國 立 交 通 大 學

電信工程學系

碩 士 論 文

高速模型演算法擺放無意義金屬用以改善化學機械研磨的平整度

Fast and Model-Based algorithm for dummy pattern insertion in layout uniformity of chemical mechanical polishing

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摘要

在超大型積體電路進入了深次微米的時代之後，晶片製造的困難度和可靠度都大幅下降，而主因就是化學機械研磨後的晶圓平整度問題。晶圓的平整度會干擾製程中的曝光，進而影響電路的效能甚至毀壞電路，這個問題在深次微米後的晶片製造影響更是明顯。由於先進的製程科技，插入無意義的金屬已經是成為主流的方法用以改進在化學機械研磨之後的晶圓平整度。在這篇論文當中，我們提出一個更快更有效率的的演算法，命名為Fast Model-based Dummy Insertion (FMDI) 演算法 去處理這個問題。 FMDI演算法使用低通濾波器的模型去有效的選擇數個最低密度的位置擺放無意義金屬。FMDI演算法可以得到比之前更快更有效率的結果。因為其中有使用到快速傅立

葉轉換所以時間複雜度限制為O(nlogn)。並且和之前的線性演算法的時間複雜度$O(n^3)$比較起來，FMDI 演算法只需要時間複雜度O(nlogn)。由實驗的結果更可以看出FMDI演算法的結果比Min-Variance method [6] 的結果更好速度更快。

Fast and Model-Based algorithm for dummy pattern insertion in layout uniformity of chemical mechanical polishing

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Abstract

After VLSI fabrication technology entered deep-submicron regimes, the increasing difficulty in fabrication leaded to decrease in manufacturability and reliability of IC. Post-CMP (Chemical Mechanical Polishing) wafer topography variation is one of the main reasons. The variation caused change of metal line shape in lithography and circuit performance related problems, especially in DSM.

Due to advanced technology manufacturing variations, dummy feature placement becomes the key process of VLSI fabrication in reducing wafer-topography variation in chemical mechanical polishing. In this thesis, we propose a faster and more effective algorithm, called Fast Model-based Dummy Insertion (FMDI) algorithm, to deal with this issue. FMDI selects panels to insert dummy feature by effective CMP low pass filter model, and obtain feasible solutions with good quality very quickly. Compared with previous linear programming approach that costs $O(n^3)$, FMDI is quite fast in $O(n\log n)$, same complexity as in [6]. The experiments on a real design show that our approach has outperformed the approach in [6], and is more efficient and effective in the smoothness of metal layers.

誌　謝

兩年的時間，讓我體驗的深刻的碩士生活，雖然沒有什麼大風大浪，但是有大家的互相扶持我才有可能完成今天碩士的學業。

這二十幾年來始終不停止關心我的父母，是我最大的動力，我深信現在他們依然在遙遠的星辰中注視著我。雖然看不見但是依舊存的鼓勵，無論是在歡樂或是失意的時候都可以陪伴的我。感謝這分秒不停的關心。

在我剛進入碩士的時候，張振壹教授給予我相當大的啟蒙與鼓勵，同時教導我相當多做人做事的道理，是我精神上的導師。而陳宏明教授適時的提攜我，讓我能有機會可以接觸到 EDA 的研究領域。不可否認的，我對這份研究相當有興趣。在這片對我而言尚是未知的領域，陳宏明教授也給予細心的指導與支持。感謝在碩士遇見的兩位恩人。

研究的時候，雖然大家研究題目互不相同，但是互相討論與教導更是增進與同學的友誼。雖然真的是短短的兩年時光，但是我相信大家的心中都已經默許了成為一輩子的好朋友。感謝兩年的夥伴們。

感謝各位

Contents

List of Figures

List of Tables

Chapter 1

Introduction

With VLSI fabrication technology entering deep submicron(DSM) regimes, the increasing difficulty in fabrication leaded to decrease in manufacturability and realiability of IC. Post-CMP (Chemical Mechanical Polishing) wafer topography variation is one of the main reasons. The variation caused change of metal line shape in lithography and circuit performance related problems, especially in DSM. Recent studies, such as [1], show post-CMP strongly depends on the features density (topography variation). Improving the density uniformity through dummy feature filling usually gets better CMP planariazation quality [2][3].

Methods for tiling can be classified into two categories: rule-based and model-based. Rule-based tiling method are from the experience that inter-layer dielectric (ILD) thickness is directly proportional to local pattern density. Compared to rule-based approach, model-based methods are based on analytical expressions, which are not simply proportional relations between local pattern density and post-CMP oxide thickness, allowing both local tile density and insertion location to vary. Obviously model-based methods provide more accurate and efficient results [1-3]. Until recently many algorithms [5-8] about dummy filling have been proposed. The linear programming method gives us optimal solutions but it is time-consuming. The greedy and Monte-Carlo methods are much faster: the Monte-Carlo method selects a panel in each step according to priority assigned by panel effective density, while the greedy method searches for the panel with the highest priority in each step and fills with the maximum possible amount of dummy features. During dummy feature placement, CMP process model is the key to efficiently solve this problem. An accurate 2-D low pass filter CMP model has been developed and tested[9-12].

In this thesis, we propose a novel algorithm to efficiently and effectively inserting dummy features to solve CMP problems, named Fast Model-based Dummy Insertion (FMDI). FMDI algorithm contains accurate CMP model, smart and efficient dummy features assignment, and dummy feature density extraction. FMDI algorithm has computational cost of O(nlogn), mainly constrained from Fast Fourier Transformation (FFT), which is the same complexity as in [6]. However, through an experiment with a real design, our approach has outperformed the approach in [6] in efficiency and performance (uniformity) of dummy feature placement. The remaining parts of the thesis are organized as follows. In Chapter II, we discuss the previous works about CMP low pass filter model, formulation of dummy feature placement, and multi-layer transfer function. In Chapter III, we present our FMDI algorithm and further improvement in efficiency. We show experimental results in Chapter IV and conclude the thesis in Chapter V.

Chapter 2

Preliminaries

In this Chapter, we discuss the previous works. First, the relation of panel density and ILD thickness tells why we change the panel density to increase the layout uniformity. Then we illustrate the 2-D low pass filter density model which is more accurate than original local pattern density model. At last, the old objective and multi-layer structure will be shown.

2.1 Panel density and ILD thickness

The inter-level dielectric (ILD) variation must be kept in control due to aggressive lithographic depth-of-field focus budget requirements and the potential impact of dielectric thickness variation on circuit performance. This problem has become especially acute as performance requirements have increased, dimensions have scaled, and larger die sizes have emerged. Also, CMP has found wider application in VLSI technology development and production serving as an enabling tool for shallow trench isolation , damescene metallization technologies, and other novel process techniques.

Attempts to control CMP ILD thickness variation include an exhaustive search and experimentation with different consumable and process choices (especially pads), but no

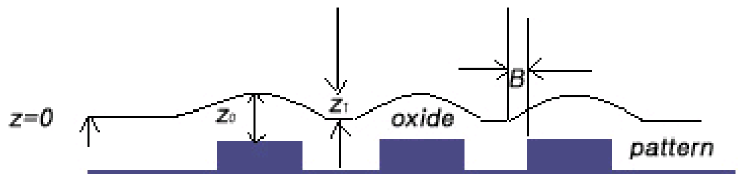

Figure 2.1: Some parameters in Chemical Mechanical Polishing(CMP).

consumable choice currently available appears to reduce appreciably pattern-dependent dielectric thickness variation; thus, the only viable choice available for reducing layout pattern dependent dielectric thickness variation is to change the layout pattern in each metal layer.

The ILD thickness Z at location (x,y) is solved from the following equation:

$$Z = \left\{ \begin{matrix} Z_0 - [K_i t/\rho_0(x,y)] & t<(\rho_0 Z_1/K_i) \\ Z_0 - Z_1 - K_i t + \rho_0(x,y) Z_1 & t<(\rho_0 Z_1/K_i) \end{matrix} \right\} \quad (1)$$

where K_i is the blanket polishing rate, Z_0 is the height of oxide deposition, Z_1 is the height of existing feature, t is the polishing time, and $\rho_0(i,j)$ is the initial pattern density (Figure 2.1).For a specific CMP process, all K_i, Z_0, Z_1, and t are constants. As a result, the final topography is determined by the pattern density $\rho_0(x,y)$.

2.2 2-D low pass filter CMP model

In chip-level CMP model, we need to predict the dielectric planarization performance for any layouts. Thus a precise density model for detecting the location to insert dummy features is significant. The effective density model proposed in [10] had excellent ability for simulating CMP process and easy to implement.

The effective pattern density across a die is determined in two steps. First, local pattern density is evaluated in small panels in a square grid across the die. The pattern density in each panel is the ratio of metal pattern density and total panel area . Second, the 2-D filter (Figure 2.2) is used to determine the effective density for each panel by weighting the influence of nearby panel density for each panel. The number of grid points is set to a power of two so that the Fast Fourier Transform (FFT) may be used. The effective discretized density, $\rho(i,j)$ is given by:

$$\rho(i,j) = IFFT(FFT(d(i,j)) \cdot FFT(f(i,j))) \qquad (2)$$

where $f(i,j)$ is discrete weighting filter, and $d(i,j)$ is local pattern density.

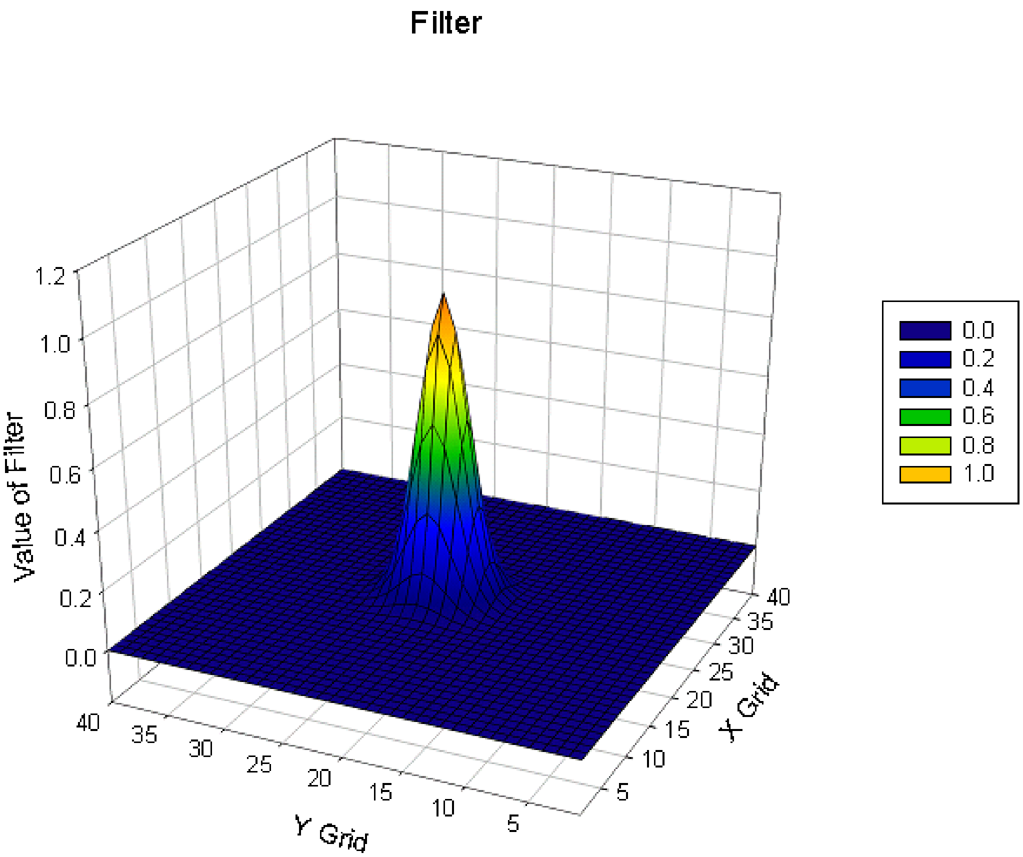

Figure 2.2: The illustration of the discrete weighting filter used by transfering local pattern density to effective density.

2.3 Previous works on dummy insertion

Table 2.1 shows many algorithms for solving dummy insertion problem. All detailed descriptions in time complexity and layout uniformity for those algorithms are listed.

Table 2.1: Algorithms performance comparison table

	Rule-based	Linear programming	Greedy	Monte-Carlo	Min-Var
Time complexity	fast	O(n^3)	O(nlogn)	O(nlogn)	O(nlogn)
Layout uniformity	worst	best	good	good	good

Rule-based method is developed according to that the ILD thickness is proportional to local layout density. Rule-based method has execellent performance in time complexity. After effective density model is proposed, we can predict the abstract level final topography. So model-based algorithms lead us to better layout uniformity. Linear programming approach [3] has best layout uniformity but worst time complexity. Greedy algorithm[7,8] choose the location to insert dummy pattern with highest priority. Monte-Carlo algorithm [7,8] selects location randomly,while min-var [6] method randomly picks n location to insert dummy pattern. Greedy, Monte-Carlo, and min-var algorithms have similar performance in time complexity and layout uniformity.

2.4 Multiple layer dummy insertion

In order to control the layout uniformity more precisely, multiple-layer structure consideration for dummy insertion is needed. Furthermore, the variation in ILD thickness is cumulative from layer to layer. Each layer except first one cannot assume a perfectly uniformity starting surface. Therefore, tiling each layer individually may not achieve yearning planarization when layers are stacked together in semiconductor manufacturing. In the model for cumulative effective density, topography variation of one layer flats through the CMP processes, each of which is modeled as a low-pass filter based on equations (1) and (2).

Mathematically

$$\underset{\rho_{0(k)}}{\sim} = \begin{cases} \left[\underset{d_k}{\sim} + \left(\frac{z_{k-1}}{z_k} \right) \underset{\rho_{0(k-1)}}{\sim} \right] \times \underset{f}{\sim} & \text{if } k > 1 \\ \underset{d_1}{\sim} \times \underset{f}{\sim} & \text{if } k < 1 \end{cases}$$

where

"$\sim$" FFT operator;

$\rho_{0(k)}$ effective local density;

Z_k step height;

d_k local density, for all layer k;

f weighing function;

For example, the effective density for layer two is the ILD thickness of post-CMP oxide of layer one passed through function (2) two times. i.e.,

$$\underset{\rho_{0(2)}}{\sim} = \underset{f}{\sim} \times \left(\underset{d_2}{\sim} + \left(\frac{z_1}{z_2} \right) \underset{f}{\sim} \times \underset{d_1}{\sim} \right)$$

2.5 Min-var problem formulation

Formula below is the the previous objective from [6].

Minimize:

$$\rho^H - \rho^L \quad (3)$$

Subject to:

$$0 \le \rho^L \le \rho_0(i,j) \le \rho^H \le 1$$

$$0 \le d_1(i,j) \le S(i,j)$$

$$d(i,j) = d_1(i,j) + d_o(i,j) \quad (4)$$

where ρ^H and ρ^L are the maximal and minimal effective density in all panels, d_0 is the original layout density at location (i,j), $d_1(i,j)$ is the dummy feature density at location (i,j), and $S(i,j)$ is the salck of panel in layout.

Chapter 3

Fast Model Based Dummy pattern Insertion algorithm

In this Chapter, we debate the core of the dummy filling problem. New objective which is more appropriate to min-variation filling problem is modified by [6]. We will show the pseudo code and flow chart of FMDI algorithm, meanwhile, the difference of FMDI algorithm will be described. Then we show a new equation which is used to improve FMDI algorithm.

3.1 Our problem formulation

Given a rule-correct design in an $n * n$ panel, we add dummy feature in low effective density panel to minimize the variation of effective density, and satisfy foundries design rule. According to (1), minimizing the variation of effecitve density in panels is the same as minimizing variation of ILD thickness. So we slightly modify the objective which is min-variation problem for single layer presented in [6].

Minimize:

$$\rho^H - \rho^L \qquad (3)$$

Subject to:

$$0 \leq \rho^L \leq \rho_0(i,j) \leq \rho^H \leq 1$$

$$0 \leq d(i,j) \leq d_{\max}$$

$$d(i,j) = d_1(i,j) + d_o(i,j) \qquad (4)$$

where ρ^H and ρ^L are the maximal and minimal effective density in all panels, $d_1(i,j)$ is the dummy feature density at location (i,j), and $d_{\max}$ is the max panel density in layout.

3.2 FMDI algorithm

In order to efficiently reduce the variation of effective density in all panels, we have developed FMDI (Fast Model-based Dummy feature Insertion) algorithm. This algorithm integrates with effective density model and the new processes we proposed. FMDI calculates the effective density in every loop, and selects the lowest ρ panel to fill dummy features. If the panel density or effective panel density exceeds constraints, we lock the panel from inserting dummy features. Fill amount is determined by the selected panel and mean effective panel density. The above steps are repeated until the maximal number of iteration is reached or uniformity of effective density cannot be further improved. FMDI algorithm(Figure 3.1) is described as follows:

Algorithm 1 *Fast and effective Model-based Dummy Insertion (FMDI)*

While(not terminated (max iteration or uniformity reached){

1. *Calculate the effective density for all panels*
2. *Find lowest ρ in $n * n$ panel*
3. *Set $panel(i,j)$ locked if $mean(\rho) - \rho(i,j)$ or $d_{max} - d(i,j) < \epsilon$*
4. *If selecting $panel(i,j)$ is locked, stop the algorithm*
5. *Calculate the fill amount: Fill amount =*
   *$coef$ * $(mean(\rho) - \rho(i,j))$+ basic*
6. *Assign dummy pattern in $panel(i,j)$*

}

where $mean(\rho)$ is the mean value for all panels, $coef$ is the weight for accurately inserting dummy feature (also shown in previous approaches), and $basic$ is the basic amount for dummy feature placement.

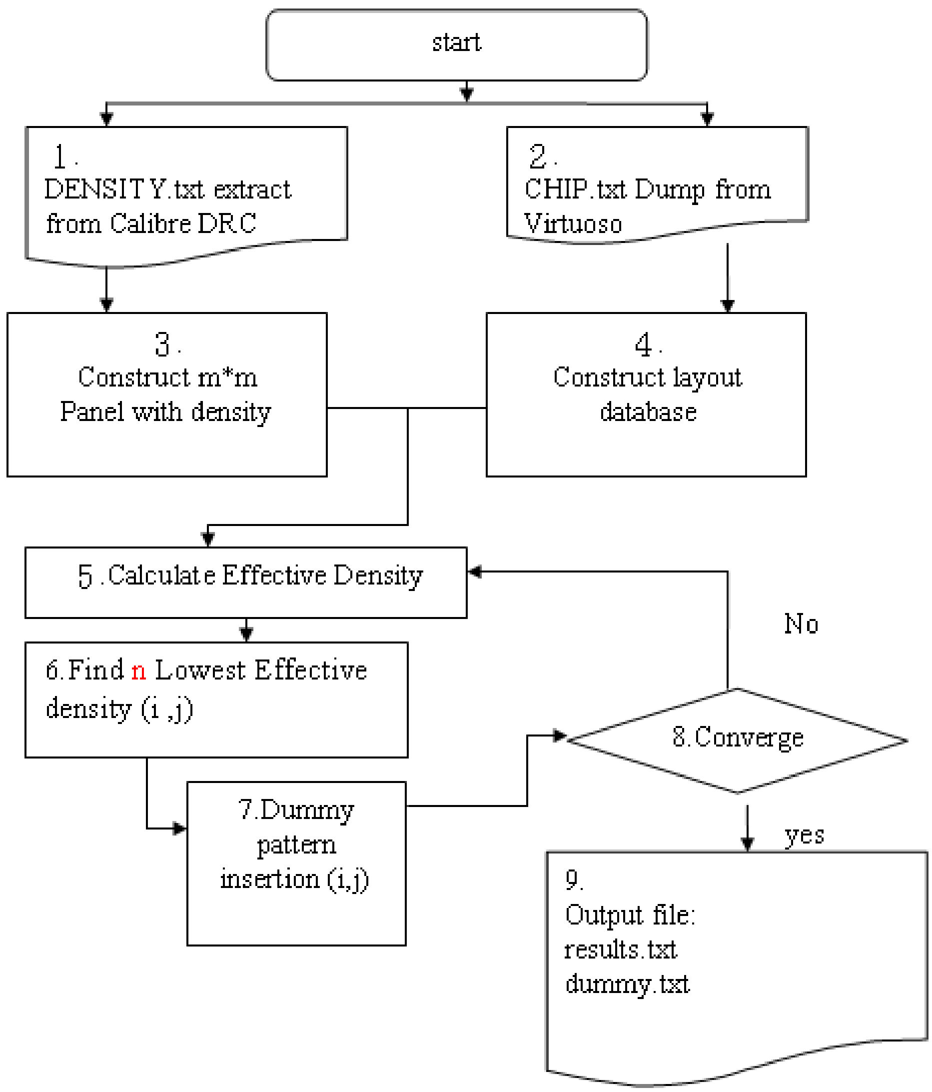

Figure 3.1: The flow chart of the FMDI algorithm.

FMDI algorithm is different from the other model-based algorithms in three parts.

1. If the panel density which is selected satisfies the max density constraints, the panel will be locked. This will prevent to insert too many dummy patterns in one panel. If the effective panel density is closed to mean value of the effective panel density, the panel is locked. This step means effective panel density will converge to better solutions. As can be seen that we do not have steps to remove excess dummy features, which makes our approach more efficient.

2. Comparing with the other model-based algorithm which approached the optimal solution like damped oscillation, FMDI algorithm approaches the optimal solution like exponential increase. That is the reason why we can set the factor $coef$ very small. Once the $coef$ is smaller, the assignment of dummy feature is more accurate. So the layout uniformity will be smoother. This part of FMDI algorithm can lead to nearly optimal solution.

3. Obviously the termination of the dummy feature insertion algorithm will be slow if we set $coef$ small. So we add a factor *basic* in our algorithm. The usage of factor *basic* will accelerate the termination of the dummy feature insertion algorithm, and *basic* must be a positive integer. Factor *basic* cannot be too large, otherwise FMDI algorithm will lose accuracy. Figure 3.2 demonstrates the improvement of algorithm speed by factor *basic*. By applying this factor, our approach can reach uniform insertion, thus obtaining accurate results, compared with other model-based approaches with non-uniform dummy feature insertion [1].

3.3 Further FMDI algorithm improvement for efficiency

In this Section, we will illustrate the improvement of FMDI algorithm. Additionally this improvement provides users a choice between execution time and layout uniformity.

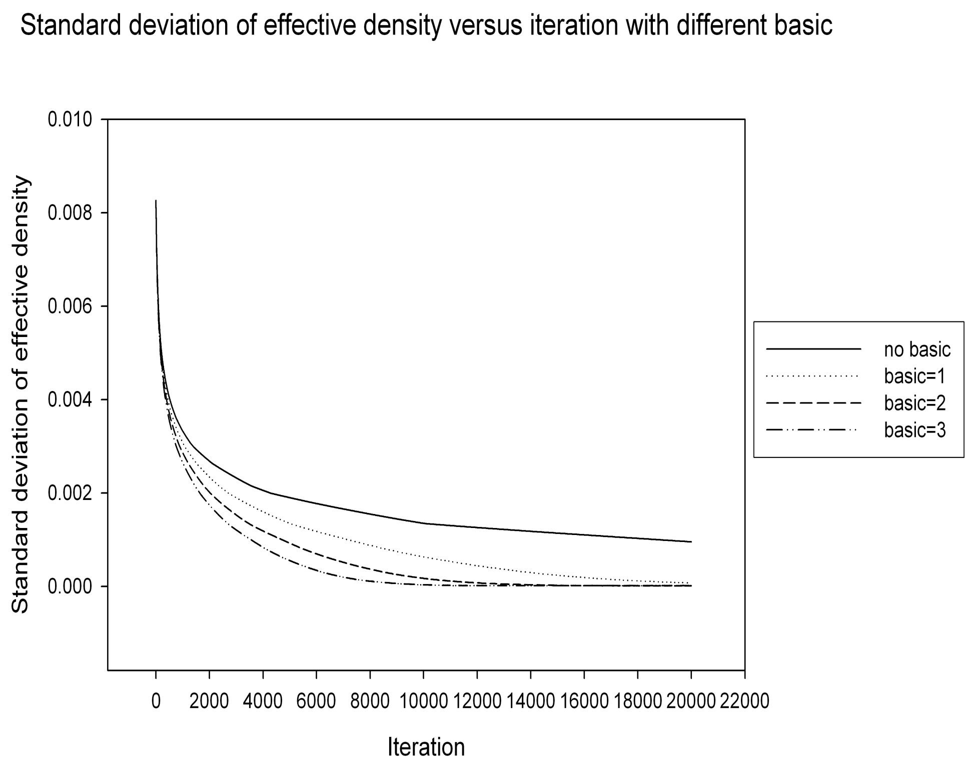

Figure 3.2: The improvement of algorithm speed by applying the factor *basic*. With appropriate *basic* value, we can reach good solutions with much less number of iterations.

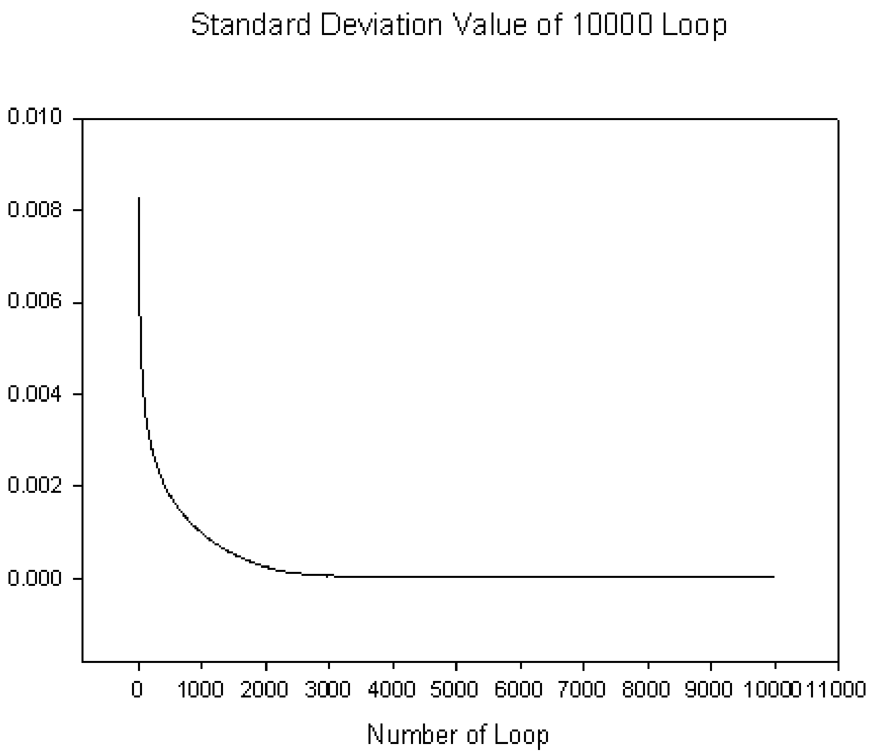

Figure 3.3: This shows that number of iteration and layout uniformity is unlinear positive corelation

Table 3.1: Effect of number of iterations to execution time and standard deviation of effective density.

Iterations	Standard-Dev	Time(s)	Dummy(num)
10000	4.6788e-05	48.93	350296
3000	6.0256e-05	18.13	126188

Table 3.2: Error rate between predicted iteration number and exact iteration number. This shows that (5) can accurately predict the total number of iterations in reaching target smoothness.

coef	pre_iter	exact_iter	error
0.05	2783	3000	0.072
0.04	3265	3600	0.093
0.03	4057	4297	0.056
0.02	5598	5729	0.023
0.01	10000	8571	0.167

Figure 3.3 shows the correlation between number of iteration and layout uniformity. Actually the number of iteration which reaches 3000 is nearly convergent (Table 3.1). The other 7000 iterations only improve 1.3 times to standard deviation of 3000 iterations, but spend more time and dummy features. This shows that users can choose high uniformity or high efficiency of the filler program.

We discover the most effective number of loop can be predicted by many factors. The predicted function is as follows:

$$pre\_iter = \frac{(Max\_ED - Min\_ED)*(Mea\_D - Min\_D)/X}{n*dum\_w*dum\_L*m*coef/(die\_w*die\_l)} \qquad (5)$$

where $X = \ln(\ln(1/coef))$, Max_ED and Min_ED are max and min effective density. Mea_D is mean value of density. Min_D is min density.And dum_w and dum_l are width and length of dummy features. Factor n means that we seperate layout into n*n panels. Obviously die_w and die_l are width and length of die. Part of X is to correct the function.

Table 3.2 shows that the predicted iteration and exact iteration with different $coef$. The data predicting through (5) can be used for improving the efficiency of FMDI algorithm. However users still can chooes efficiency and layout uniformity by their will.

[1]The factor *basic* can be a constant or a variable. The experiments we perform are applying constant *basic*. If variable *basic* is used, it can reach better results. The variable *basic* can be obtained as follows: $basic = ln(ini\_max(\rho) - ini\_min(\rho))/ln(max(\rho) - min(\rho)) * n$, where n is a constant.

Chapter 4

Experimental results

4.1 Single layer dummy pattern insertion

We test the FMDI algorithm by LDPC_1200 decoder chip with UMC 0.18um technology. Experimental results shows the layout uniformity, peak to peak value, number of dummy features, and maximum local pattern density. For comparing, we implement the data passed through min-var method and show the layout uniformity without inserting dummy features. Because the data are too large, only metal layer 1,4 will be shown ,and min-var method only demonstrate metal layer 1 results.

As shown in Figure 4.1, we experiment on Mentor Calibre DRC for design rules checking and Cadence SOC encounter for extracting layout data. Then the data passed through FMDI program and obtain the DEF format result. At last the DEF format file received from FMDI algorithm must adds to original layout DEF file.

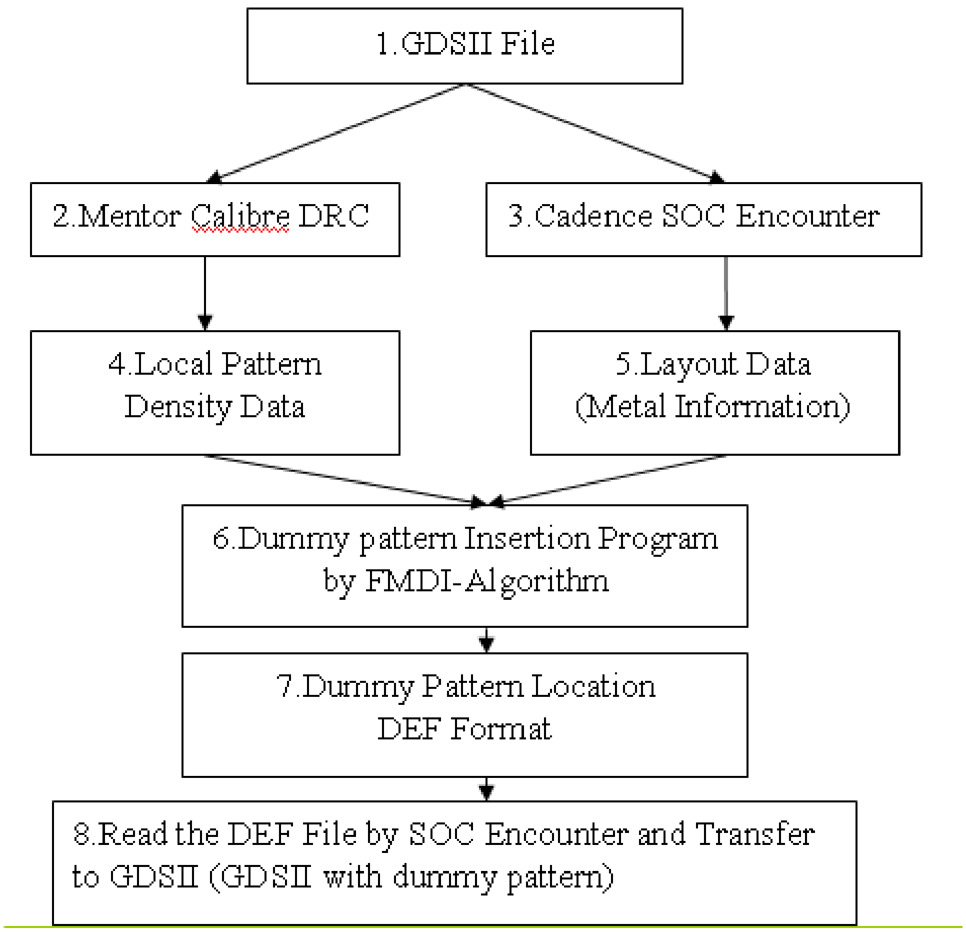

Figure 4.1: Mentor Calibre DRC for design rules check and Cadence SOC encounter for extract layout data. The data passed through FMDI program and obtain the DEF format result.

4.1.1 Effective density without inserting dummy features

Figure 4.2 demonstrates the metal 1 layer effective density without inserting dummy features. Table 4.1 shows the information of effective density.

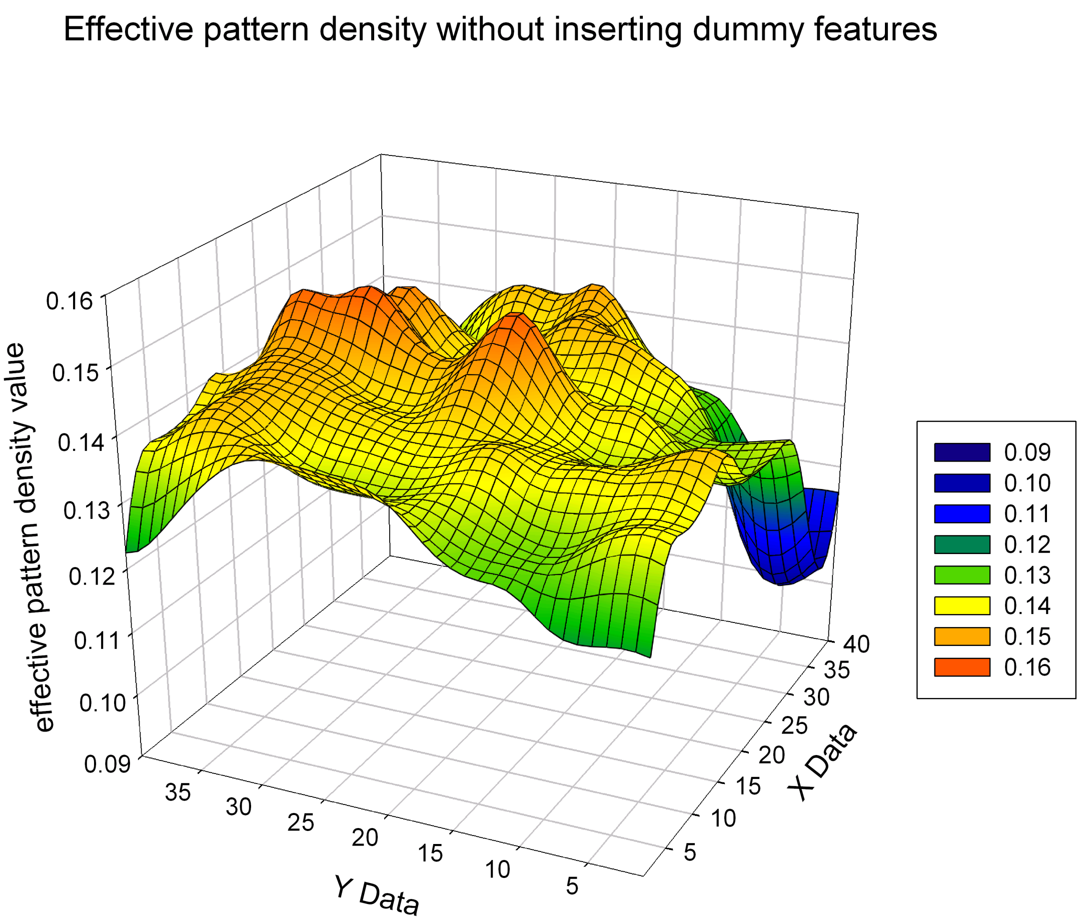

Figure 4.2: Metal 1 layer effective pattern density without inserting dummy features

4.1.2 Local pattern density without inserting dummy features

Figure 4.3 demonstrates the metal 1 layer local pattern density without inserting dummy features. Table 4.2 shows the information of local pattern density.

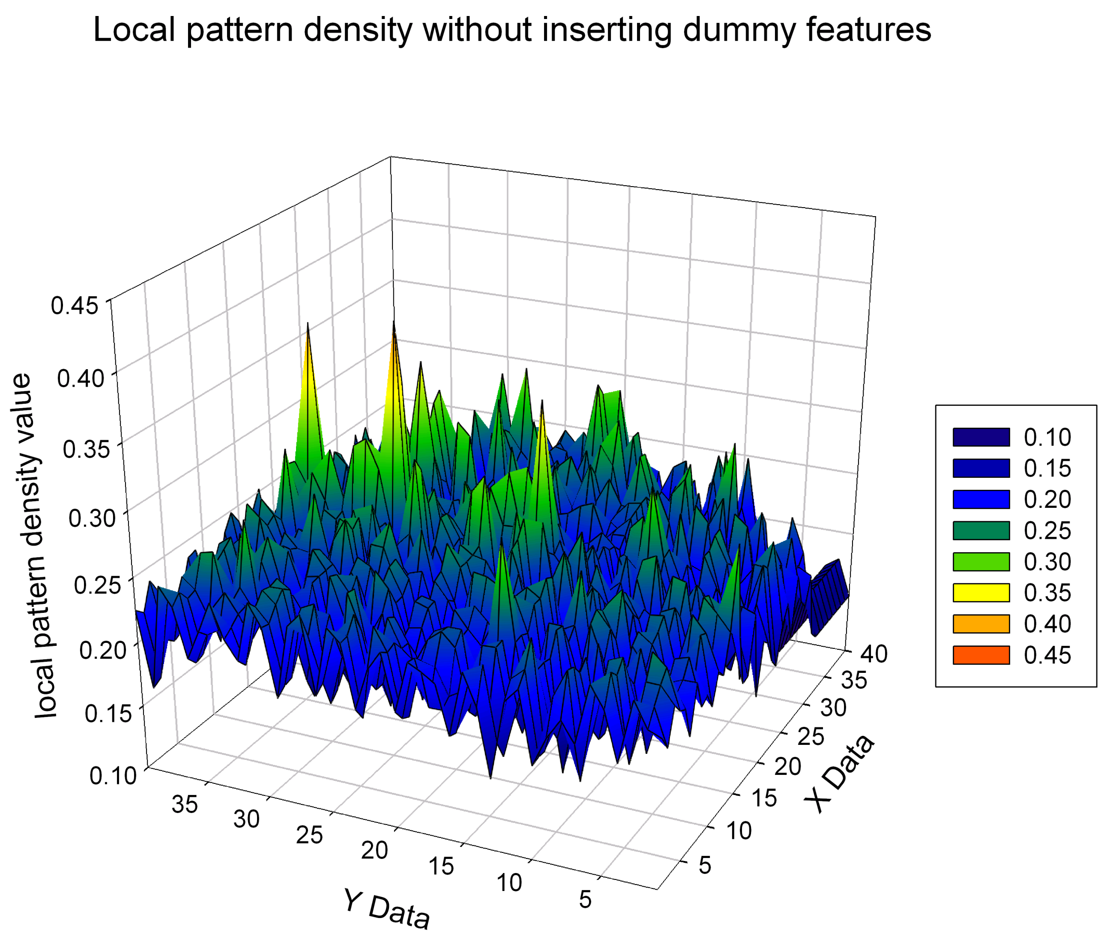

Figure 4.3: Metal 1 layer local pattern density with inserting dummy features

4.1.3 Effective density with dummy pattern insertion by FMDI algorithm

Figure 4.4 demonstrates the metal 1 layer effective density without inserting dummy features. Table 4.3 shows the information of effective density.

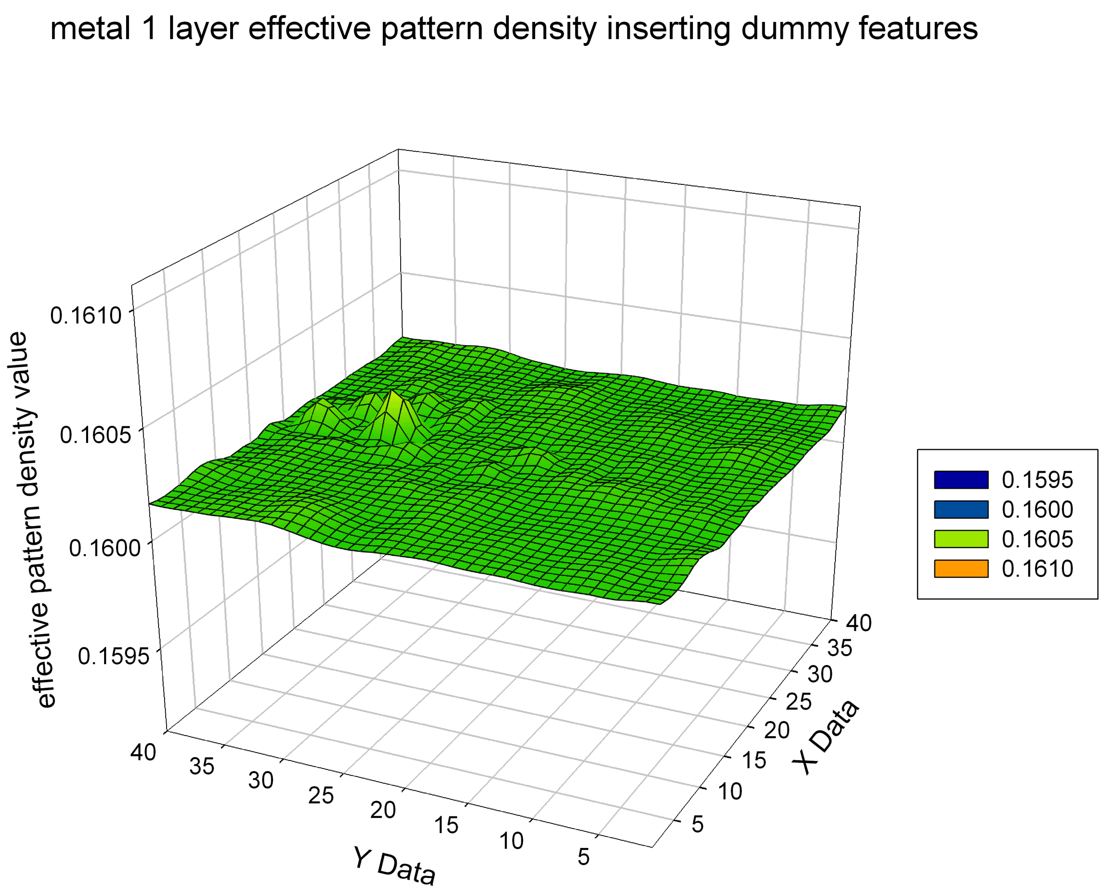

Figure 4.4: Metal 1 layer effective pattern density with inserting dummy features by FMDI algorithm

4.1.4 Effective density with dummy pattern insertion by Min-Var algorithm

Figure 4.5 demonstrates the metal 1 layer effective density without inserting dummy features. Table 4.4 shows the information of effective density.

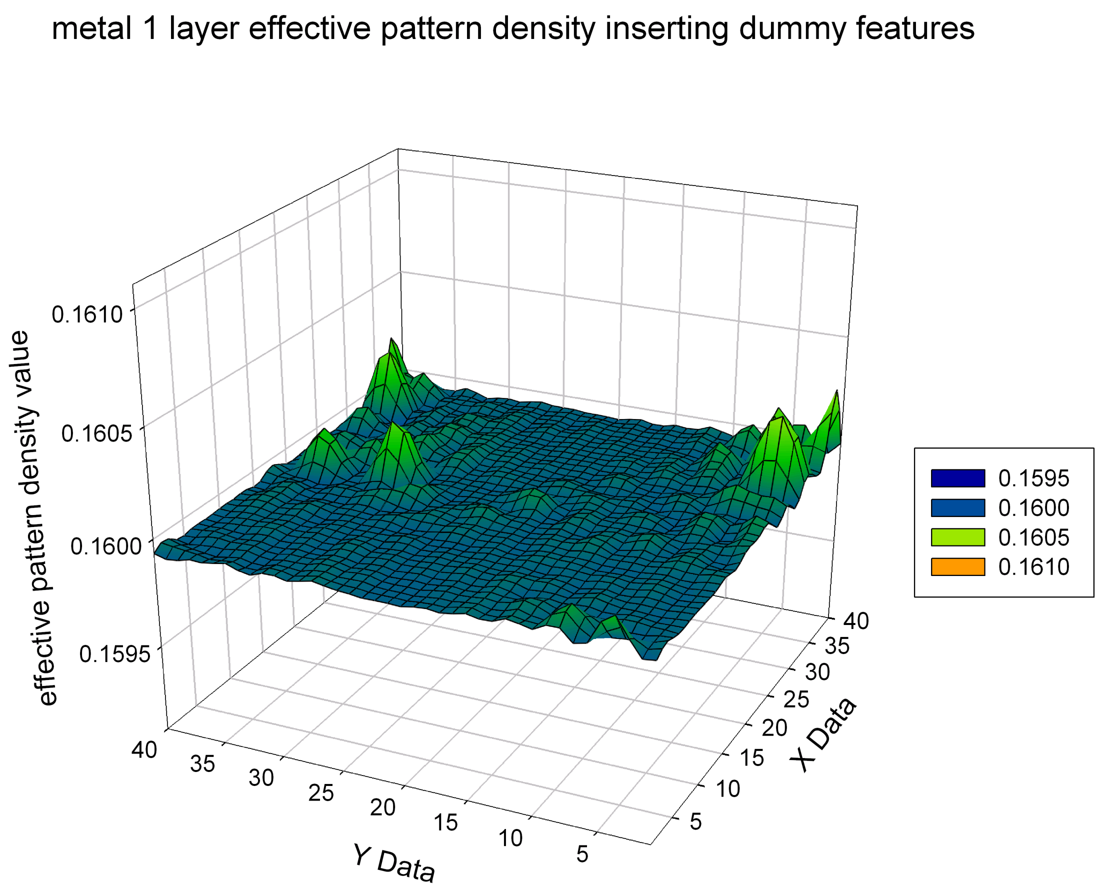

Figure 4.5: Metal 1 layer effective pattern density with inesrting dummy features by min-var method

4.1.5 Comparison of FMDI and Min-Var

Through different processes, FMDI algorithm achieves better solution whether in layout uniformity or execution speed. We will show the comparison table between FMDI algorithm and min-var method, and then discuss the improvement of FMDI algorithm.

1. Layout uniformity

FMDI algorithm reaches the nearly optimal solution with excellent precision. Low standard deviation and peak to peak value mean the high reliability and manufacturability. Furthermore, less dummy features inserted is achieved by better precision.

2. Algorithm speed

As the description in Section 3.2, parameter *basic* accelerates the speed of algorithm. Algorithms proposed before will insert more amount of dummy patterns but less at the termination. By inserting steady number of dummy features, *basic* can eliminate the drawback of algorithms proposed before and accomplish the insertion jobs more fast.

3. Side effect

RC consideration is now the major and significant affection of dummy feature insertion. Although the improvement is not purpose in this research, but it is really a good side effect.

Table 4.1: Metal 1 layer effective pattern density data without inserting dummy pattern include maximal value, minimal value, standard deviation, and peak to peak value.

Max(ρ)	Min(ρ)	Sta_Dev(ρ)	peak to peak(ρ)
0.151912	0.101997	0.00826395	0.049915

Table 4.2: Metal 1 layer local pattern density data with inserting dummy features include maximal value, minimal value, standard deviation, and peak to peak value.

Max(d)	Min(d)	Sta_Dev(d)	peak to peak(d)
0.388521	0.147992	0.0284971	0.240529

Table 4.3: Metal 1 layer effective pattern density data with inesrting dummy features by FMDI algorithm contain maximal value, minimal value, standard deviation, and peak to peak value, and number of inserted dummy features.

Max(ρ)	Min(ρ)	Sta_Dev(ρ)	peak to peak(ρ)	# of dummy
0.160358	0.160137	1.58499e-05	2.21e-04	125670

Table 4.4: Metal 1 layer effective pattern density data with inesrting dummy features by min-var method contain maximal value, minimal value, standard deviation, and peak to peak value, and number of inserted dummy features.

Max(ρ)	Min(ρ)	Sta_Dev(ρ)	peak to peak(ρ)	# of dummy
0.160291	0.159892	3.913e-05	3.99e-04	144457

Table 4.5: Compare the performance between FMDI algorithm and min-var method.

Algorithm	Max(ρ)	Min(ρ)	Sta_Dev(ρ)	peak to peak(ρ)	# of dummy	iteration
FMDI	0.160358	0.160137	1.58499e-05	2.21e-04	125670	15388
Min-var	0.160291	0.159892	3.913e-05	3.99e-04	144457	29915

Table 4.6: Compare the number of inserted dummy pattern and maximal local pattern density.

Algorithm	# of dummy	Max(d)
FMDI	125670	0.388521
Min-var	144457	0.450274

4.2 Multi-layer dummy pattern insertion

Figure 4.6 shows the metal 4 layer effective density in single layer dummy feature insertion and Table 4.7 shows the metal 4 layer effective density data. Definitely the layout uniformity of metal 4 layer is perfect, but actual situation in manufacturing won't be ideal. It means that the layout uniformity of lower level will affect the layout uniformity in high level, and ILD thickness variation accumulates through first one layer to last one. Then we simulate the actual layout uniformity in manufacturing by single-layer consideration data.

Figure 4.7 shows the real status of metal 4 layer in manufacturing. Obviously multi-layer consideration is unavoidable.

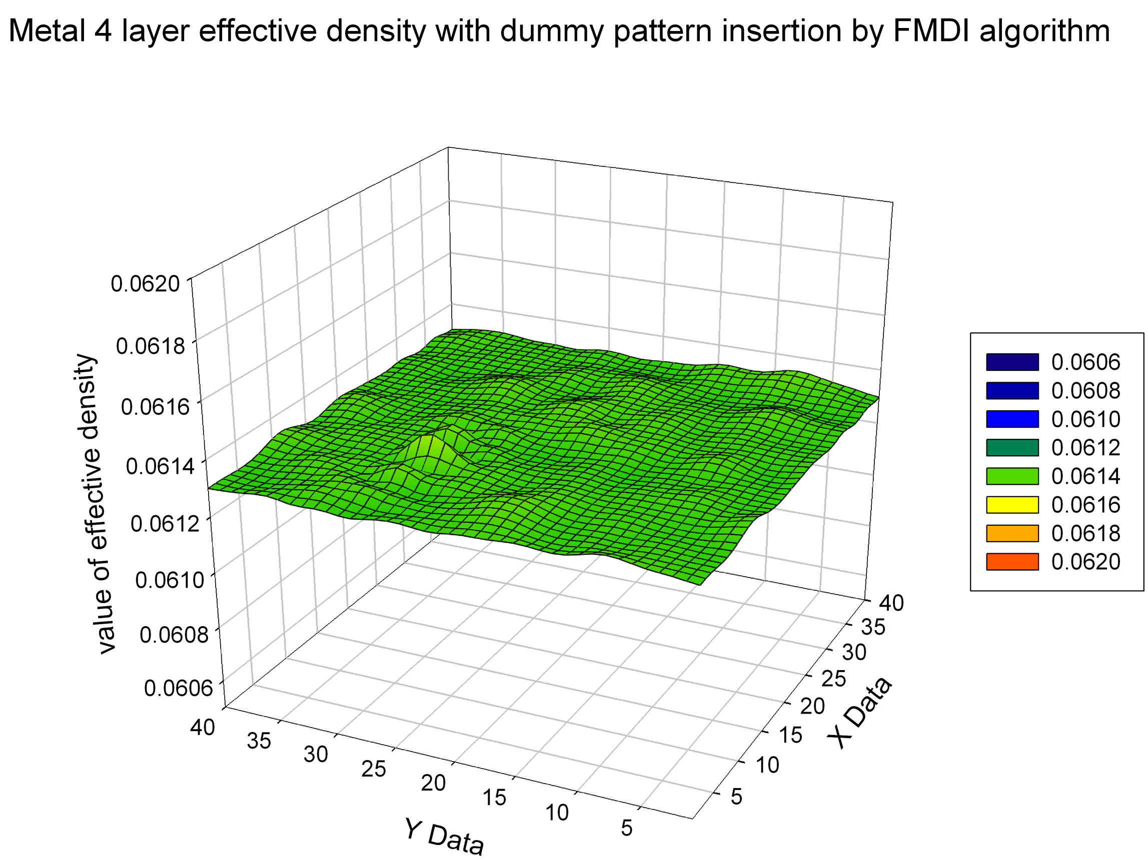

Figure 4.6: Metal 4 layer effective density with single layer dummy pattern insertion by FMDI algorithm

Table 4.7: The table contains the analysis data of metal 4 layer effective density include maximal value,minimal value, standard deviation, peak to peak value, and number of dummy pattern inserted.

Max(ρ)	Min(ρ)	Sta_Dev(ρ)	peak to peak(ρ)	# of dummy
0.0614075	0.0612909	1.15803e-05	1.166e-04	199994

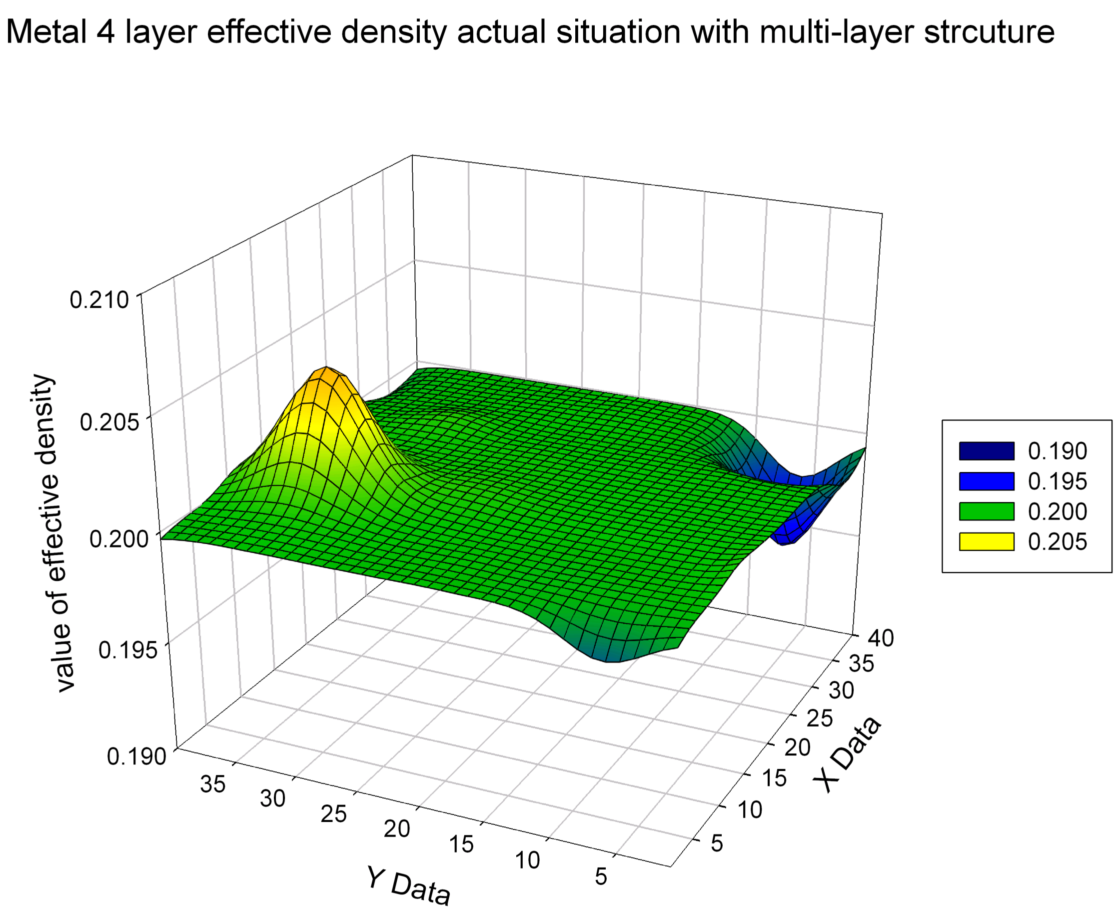

Figure 4.7: Simulate metal 4 layer actual(multi-layer) effective density with single layer data

Chapter 5

Conclusion and future works

Chemical mechanical polishing(CMP) has became an improtant process for layout uniformity in chip manufacturing. Through the development of CMP technology, layout global planarization can be accomplished more conveniently and effectively. But there are still some problems in CMP process like dishing and erosion. Since ILD thickness is proportional to local pattern density. Therefore dummy feature insertion is a useful method to avoid the defects in CMP process with control local pattern density.

From the large amount of researches[2][3][4][5][6][7][8] before which studied intensively in dummy feature insertion algorithm, we remain the best part like density model and concept of problem formulation. The 2-D low pass filter for improving the detection of low density part is preserved. According to the drawbacks of algorithm processes we improve the algorithm speed and precision by correcting filling amount calculation and reform the RC problems by deceasing the number of dummy features and keeping away from critical path. Therefore we have proposed fast model-based dummy insertion(FMDI) algorithm to resolve the problem.In experiment, FMDI algorithm performs efficient and high speed CMP dummy pattern insertion and new method has an O(nlogn) time complexity. The experimental results shows that the layout uniformity is very smooth. Additionally the precision of FMDI algorithm can decrease the number of inserted dummy features.

We will study the problem for consequent problems in capacitance increase and time issues as future works.

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Bibliography

[1] B. Stine. et al., “The physical and electrical effects of metal-fill patterning practices for oxide chemical-mechanical polishing process,” IEEE Trans. Electron Devices, vol. 45, no.3, pp.665-679, Mar. 1998

[2] A. B. Kahng, G. Robins, A. Singh, and A. Zelikovsky, “Filling algorithms and analyzes for layout density control,” IEEE Trans. CAD, vol. 18, pp. 445–462, Apr. 1999.

[3] R. Tian, D. Wong, and R. Boone, “Model-based dummy feature placement for oxide chemical–mechanical polishing manufacturability,” IEEE Trans. CAD, vol. 20, no.7, pp. 902–910, July 2001.

[4] W. Grobman, M. Thompson, R. Wang, C. Yuan, R. Tian, and E. Demircan, “Reticle enhancement technology: Implications and challenges for physical design,” in Proc. DAC, Las Vegas, NV, 2001,pp. 73–78.

[5] Y. Chen, A. B. Kahng, G. Robins, and A. Zelikovsky, “Monte Carlo methods for chemical–mechanical planarization on multi-layer and dual-material models,” in Proc. SPIE Conf. Design and Process Integration for Microelectronic Manufacturing, Santa Clara, CA, Mar. 2002

[6] XinWang, Charles C. Chiang, Jamil Kawa, Qing Su, “A Min-Variance Iterative Method for Fast Smart Dummy Feature Density Assignment in Chemical-Mechanical Polishing” Proc. of ISQED 2005

[7] Y. Chen, A. B. Kahng, G. Robins, and A. Zelikovsky, “Practical iterated fill synthesis for CMP uniformity,” in Proc. DAC, Los Angeles, CA, June 2000, pp. 671–674.

[8] Y. Chen, A.B. Kahng, G. Robins and Z. Zelikovsky, “New Monte-Carlo Algorithms for Layout Density Control”, Proc. ASPDAC, 2000, pp. 523-528.

[9] B. Stine, D. Ouma, R. Divecha, D. Boning, J. Chung, D. Hetherington, I. Ali, G. Shinn, J. Clark, O. S. Nakagawa, and S.-Y. Oh, "A closed-form analytic model for ILD thickness variation in CMP processes," in Proc. CMP-MIC Conf., Santa Clara, CA, Feb. 1997, pp. 266–273.

[10] D. Ouma, D. Boning, J. Chung, G. Shinn, L. Olsen, and J. Clark, "An integrated characterization and modeling methodology for CMP dielectric planarization," in Proc. Int. Interconnect Technology Conf., San Francisco, CA, June 1998, pp. 67–69.

[11] T. Yu, S. Cheda, J. Ko, M. Roberton, A. Dengi, and E. Travis, "A two dimensional low pass filter model for die-level topography variation resulting from chemical mechanical polishing of ILD films," in Proc. IEDM, Washington, DC, Dec. 1999.

[12] G. Nanz and L. E. Camilletti, "Modeling of chemical–mechanical polishing: A review," IEEE Trans. Semiconductor Manuf., vol. 8, pp. 382–389.

自傳

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