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Multi-gate non-volatile memories with nanowires as charge storage material

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ABSTRACT

Multi-gate non-volatile memory (NVM) cell is a promising approach in the next generation. In this work, the performance of NVMs using nanocrystals (NCs) and nanowires (NWs) as charge trapping materials were evaluated by three-dimensional simulation. It is found that the NWs located at different positions have different charge injection speeds. And the NW density will strongly affect the charge injection efficiency. The NW at channel center can result in large memory window and acceptable channel controllability. Although the total charges injected into NWs is lower than that injected into NCs under the same programming condition, using NWs as charge trapping material exhibits larger memory window and better channel controllability. It is suggested that the NW is a better choice than NC to be charge storage material from the perspective of memory performance.

1. Introduction

To further scale down the cell size of non-volatile memories and increases the memory density, flash-type memory is predicted to migrate from floating gate (FG) structure to discrete traps structure because conventional continuous floating gate will loss all of the charges even if one leakage path in tunneling oxide is formed [1,2]. It is hard to improve the P/E speed of FG memory because of the non-scalable tunneling oxide thickness. Coupling between floating gates is another issue. The SONOS type non-volatile memory which stores charges in discrete traps of the silicon nitride layer exhibits better retention characteristics so that the tunneling oxide thickness can be reduced to improve the P/E speed and operation voltage [3–5].

Nanocrystal (NC) memory is another possible solution for the future NVMs [6–10]. However, it is reported that as the NC size becomes smaller than 5 nm, the Coulomb blockade effect and the quantum confinement effect will degrade the programming and retention performance [11]. On the other hand, the number of NCs in one cell becomes fewer and fewer as the cell size continuously scales down so that the performance fluctuation due to NC number variation becomes worse and worse.

Using NW to replace NC has been proposed recently [12–14]. It has been demonstrated that carbon nano-tubes can be used as charge trapping materials although the operation mechanism is not clear at this moment. Comparing to the zero-dimensional NC, NW has higher density of states, weaker Coulomb blockade effect, and less quantum confinement effect due to its quasi one-dimensional structure. It is expected that NW NVM may have better memory performance than NC NVM. However, there is no literature discusses the performance of the NW NVM. In this work, the effects of density and spatial distribution of NWs on programming speed, memory window, and channel controllability are studied by three-dimensional simulation.

2. Device structure

Sentaurus-TCAD tool is used in this work [15]. The multi-gate silicon-on-insulator (MG SOI) MOSFET structure is used to obtain better fundamental device and memory characteristic. The schematic structure of the MG SOI memory cell with five NWs as discrete charge storage material is shown in Fig. 1. The channel region is p-type Si with a constant doping concentration of $1 \times 10^{15}\,cm^{-3}$. The channel thickness is 40 nm and the width is 30 nm to have fully-depletion and channel volume inversion states. The tunneling SiO_2 layer and blocking SiO_2 layer is 3 nm and 14 nm thick, respectively. No interface charge or oxide charge are assumed in the dielectric. The gate electrode is n^+ poly-Si with work function of 4.05 eV. The physical gate length is 50 nm. The source/drain concentration is $1 \times 10^{20}\,cm^{-3}$ with constant doping profile and the gate to source/drain (G–S/D) overlap is 5 nm at each side so that the channel length becomes 40 nm. The diameter of NWs is 3 nm in most case, which is a reasonable value for metallic CNTs or Si NWs. The memory cell may have 1, 3, or 5 NWs to evaluate the effects of NW density and the location. The NWs are labeled as NW1, NW2, NW3, NW4, and NW5 from drain side to source side in sequence. The NW1 and NW5 are located at the position 2 nm away from the drain and source junction, respectively, and the NW3 is located at the channel center. The NW2 and NW4 are located at the positions to have equal space between NWs. Therefore, the distance between NWs depends on the NW diameter. In the case of NW

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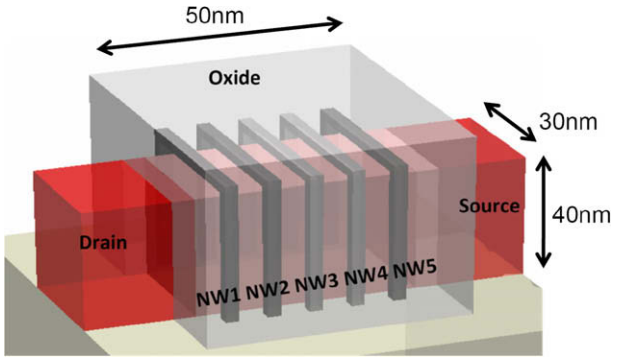

Fig. 1. Schematic structure of the multi-gate silicon-on-insulator memory cell with nano-wire as charge storage material. There are five NWs across the channel.

diameter is 3 nm, the NW space is 5.25 nm. For the memory cell with 3 NWs, the NW2 and NW4 are deleted. For the memory cell with 1 NW, only the NW3 at channel center exists. The trapping level of the NW is assumed to be 4.05 eV. The characteristics of NC NVMs are also simulated. The same MG SOI memory cell structure is used, and all of the structural parameters are the same. The only difference is using NCs to replace NWs. The diameter of NCs and NWs are both 2 nm in this comparison.

The simulation is performed in two steps. At first, the memory cells are programmed using gate bias of +16 V or +18 V to make charges in channel inject into the NWs or NCs by Fowler–Nordheim (F–N) tunneling mechanism which is dominant when relative high gate bias is applied. The drain and source are grounded. The charges injected into NWs and NCs are examined. Then the amount of charges in each NW or NC is directly assigned according to the results obtained at step one to simulate the device *I–V* characteristics.

Since this is a pure simulation work, the validity of the results is based on the validity of the used models. In this work, complete bandgap narrowing model, recombination model, quantum tunneling mechanics model, and mobility model were all considered. These models are sufficient for calculating the electrostatic performance of MOSFET. Because the tunneling layer is SiO_2 and the main carrier transport mechanism at high electric field is F–N tunneling, only the F–N model was considered in this simulation. The simulation of flash-type NVMs is a mature technique. In fact, several simulation works on the NC NVM have been reported [6,11]. Replacing NCs with NWs will not affect the validity of the simulation. Thus, it is believed that the simulation results should be reliable.

3. Results and discussions

Fig. 2 shows the charges injected into the NWs as a function of programming time at V_g = +18 V and $V_d = V_s$ = 0 V with all five NWs in the memory structure. There are more charges could be injected into the NWs at the positions near the source/drain side (e.g. NW1 and NW5) because the electric field at the gate to source/drain overlap region is higher than that at the channel region. Fig. 3 show the side-view and top-view of the electric field distributions at the same programming condition of V_g = +18 V and $V_d = V_s$ = 0 V. The strongest electric field occurs at the top corner of the rectangular shape channel because of the coupling between top gate and side gate and the field enhance due to the sharp corner. It should be noted that because the NW is across the channel, once carriers are injected into NW from the channel corner position, they redistribute immediately and change the potential of the whole NW. The threshold voltage of the memory cell would be changed effectively. This case would not occur on the NC NVM cell because the NCs are isolated from each other. The non-uniform distribution of charges in NCs will result in non-uniform channel potential and therefore poor device characteristics.

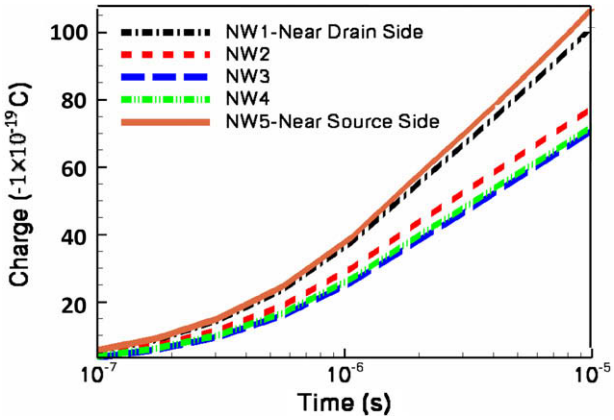

Fig. 2. Charges injected into the NWs as a function of programming time at +18 V.

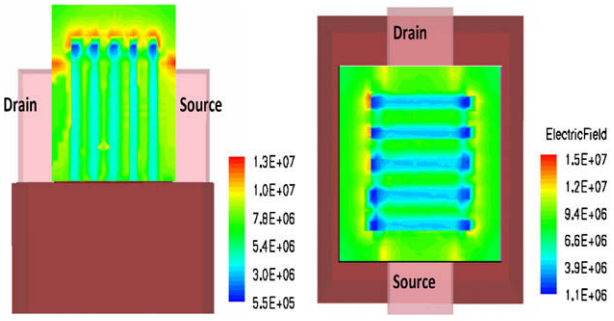

Fig. 3. Side-view and top-view of the electric field distribution during programming at +18 V.

The influence of NW density on charge injection is then evaluated. Fig. 4 shows the charges injected into the NW located at channel center (NW3) as a function of programming time with various NW densities. The programming condition is V_g = +18 V and $V_d = V_s$ = 0 V. As the NW density increases, the total charges injected into the NW3 decreases due to the Coulomb repulsion between neighboring NWs. Therefore, the memory cell with only

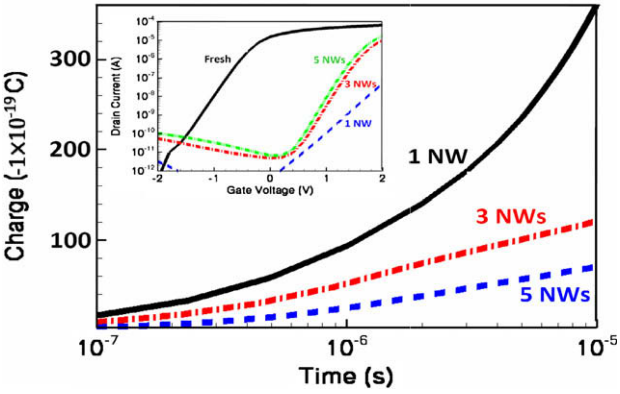

Fig. 4. Charges injected into the NW at channel center (NW3) as a function of programming time on the memory cell with various NW numbers. The programming voltage is +18 V. The inset shows the transfer characteristics of the memory cells with various NW numbers after programming at +18 V for 10 μs.

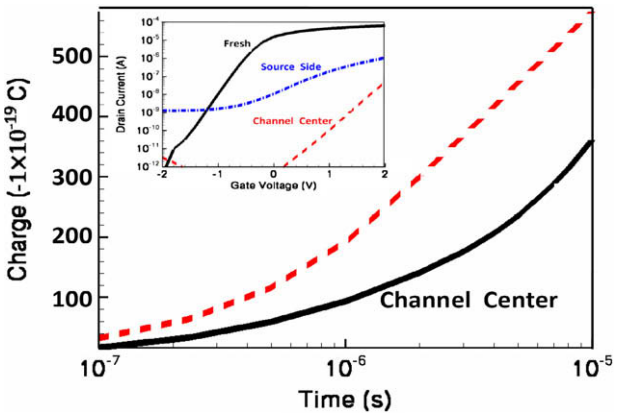

Fig. 5. Charges injected into the NW as a function of programming time if only one NW exists and the NW locates at either source side or channel center. The programming voltage is +18 V. The inset shows the transfer characteristics of the memory cells with only one NW. The NW locates at either source side or channel center. The programming condition is +18 V for 10 μs.

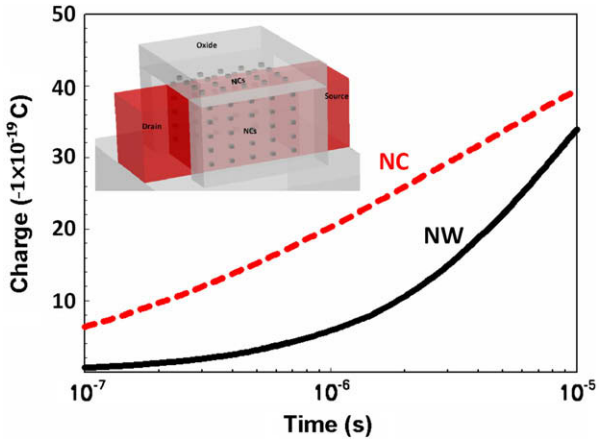

Fig. 6. Amount of the charges injected into the NW and the NCs located at channel center as a function of programming time at +16 V. The diameters of NW and NC are both 2 nm. The inset shows the memory cell with uniformly distributed NCs as charge trapping material. The diameter of the NC is 2 nm and the space between NCs is 6 nm.

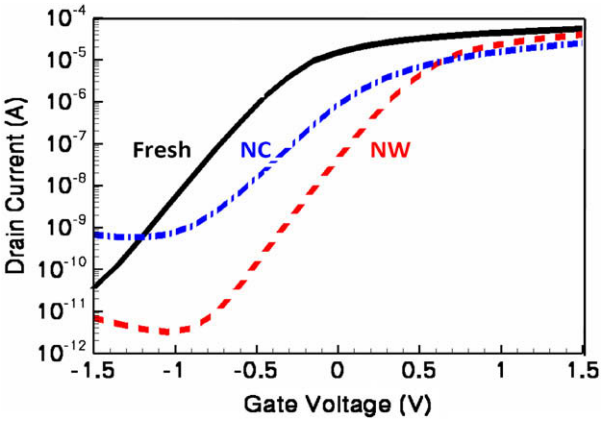

Fig. 7. Transfer characteristic of the memory cells with NWs and NCs as charge storage material after programming at +16 V for 10 μs. The diameters of NW and NC are both 2 nm.

one NW at channel center exhibits the largest memory window as the inset shown in Fig. 4. The subthreshold swing of the memory cell with only one NW at channel center (NW3) is degraded after programming. It can be explained by the mechanism similar to the drain-induced barrier lowering effect. Although the potential energy at channel center is raised by the negative charged NW, the potential energy will be lowered by the drain bias coupling as the channel length is short. The subthreshold swing degradation is not found on the memory cell with higher NW density because more NWs could screen the drain bias coupling effectively.

Fig. 5 shows the effect of the position of the NW if only one NW exists. It has been shown in Fig. 2 that the NW near source side has more charges than the NW at channel center. This phenomenon becomes more apparent as only one NW exists. Furthermore, the amount of charges injected into NW shown in Fig. 5 is much higher than that shown in Fig. 2 once the Coulomb repulsion force does not exist as only one NW exists. However, although the NW located near source side has more charges, the cell with NW at channel center exhibits larger memory window and better subthreshold swing characteristic as the inset shown in Fig. 5. The transfer characteristic of the memory cell with only one NW near source side distorts severely. Because the NW5 is only 2 nm away from the source junction edge, the high charge density results a very strong electric field near the junction edge. Band-to-band tunneling occurs at source side and results in high leakage current. The high charge density in NW5 screens the effect of the gate voltage on the electron energy barrier from source to inverted channel so that the subthreshold swing becomes poor and the driving capability becomes low. These observations indicate that the memory behavior is not only determined by the amount of injected charges, but also affected by the position where the charge stored.

To compare the memory cell performance between using NWs and using NCs as charge storage materials, memory cell with NCs at the positions of NWs is simulated. The schematic NC NVM cell structure is shown as the inset in Fig. 6. The diameters of NC and NW are both 2 nm. The distance between NCs is 6 nm. Fig. 6 shows the amount of charges injected into the NW3 and the NCs corresponding to the position of NW3 as a function of programming time at V_g = +16 V. Because the potential of each NC is determined by the charges stored in it, the total charge injected into the NCs is higher than that injected into NW because much more charges are injected into the NCs near the corner of the rectangular shape channel. However, since these NCs are discrete, each NC can affect the channel potential of a short range underneath it. Although the NCs near the channel top corner have the most charge number, these NCs cannot control the whole channel. Even with fewer total charges, the memory window of the NW cell is larger than that of the NC cell under the same programming condition as shown in Fig. 7. The NW cell also exhibits better subthreshold swing after programming. To achieve the same memory window, the NW NVM requires less charge than the NC memory cell. This characteristic implies that the NW NVM may have higher program/erase speed and better endurance.

In this work, we focused on the programming performance of the NW NVM. The read operation can be seen from the *I–V* characteristics before and after programming. The data retention is another important issue. The simulation of data retention requires more precise physical models, for example, the quantum effect in NW and NC and the transient carrier escape from different energy levels. Although it is hard to include the data retention issue in this manuscript, a short discussion can be addressed. The quantum effect in NW is weaker than that in NC. Therefore, carriers stored in NW would have lower energy than those stored in NC, which increases the energy barrier for carrier escaping. The weaker electric field due to the less stored carriers at the same memory window also benefits to the data retention performance. Therefore, it is expected that the NW NVM should have better data retention performance that the NC NVM.

4. Conclusions

In this work, the performance of multi-gate silicon-on-insulator NVM cell using NWs as charge storage material is evaluated. Evident Coulomb repulsion effect between neighboring NWs is observed. The NWs located near source and drain side have more charges but weaker channel controllability and results in poor subthreshold swing behavior than the NWs located near channel center. It is evident that where the charge stored is also an important factor to memory window and subthreshold swing behavior. Only one NW at channel center can result in large memory window and acceptable channel control ability. Although the NC NVM may have higher total injection charges, the memory window and subthreshold slope behavior are poorer than those of the NW NVM. Because less charge is required for NW NVM to obtain wide memory window, the NW NVM has the potential of high speed and heavy endurance. It is thus concluded that using the NWs across the channel is a better memory cell structure than using NC to be charge storage material.

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