行政院國家科學委員會專題研究計畫 成果報告

針對 3D 整合之電子設計自動化技術開發--總計畫(2/2)
研究成果報告(完整版)

計 畫 類 別 ： 整合型
計 畫 編 號 ： NSC 99-2220-E-009-034-
執 行 期 間 ： 99 年 08 月 01 日至 100 年 07 月 31 日
執 行 單 位 ： 國立交通大學電子工程學系及電子研究所

計 畫 主 持 人 ： 陳宏明
共 同 主 持 人 ： 周景揚、李育民、李毅郎、黃俊達、溫宏斌
計畫參與人員： 碩士班研究生-兼任助理人員：張業琦
碩士班研究生-兼任助理人員：徐欣吳
博士班研究生-兼任助理人員：蔡篤雄
博士班研究生-兼任助理人員：秦敬雨
博士班研究生-兼任助理人員：劉時穎
博士班研究生-兼任助理人員：王俊凱

中 華 民 國 100 年 10 月 31 日

中文摘要：

在過去數十年間，半導體技術尺度快速縮小，使積體電路設計發展得非常成功，這也使數以百萬計的電晶體可被整合到單一晶片中。然而在製程微縮所得到的好處愈來愈少，市場並預估摩爾定律到 16nm 時將為其極限。進一步來說，如果系統架構仍維持平面放置，在 90nm 技術結點(Technology node)平均可得到 50%-60%系統效能的改進，在 45nm 以下只能得到不到 20%的改善。因此，使電容降低、維持信號完整性、及維持高頻運作晶片的最好方式，是找到兩點間的更短的連接距離，即向上發展或立體堆疊晶片整合。3D 晶片技術是將數個晶片用矽穿孔(TSV)的方式作晶片間的連接，大大降低全域連接(global interconnect)之線長。其它好處包括了低功率、產品極小化、製造成本降低與加快上市時間。然而我們必須研發或提昇 EDA 輔助工具品質提升來克服這個新概念的設計問題。

在這個計畫裡，我們有五個研究主題來幫助目前尚未完整的 3D 整合電子設計自動化研究與設計流程/工具，包括：

(1) 三維度積體電路的隨機電熱模擬及其對功率最佳化的應用
(2) 三維電路整合之實體設計系統
(3) 針對三維規則型邏輯結構之架構探索及穩健合成系統開發
(4) 立體堆疊晶片與系統級構裝之設計最佳化研究
(5) 應用在驗證與測試 3D IC 整合過程中以計算智慧為基礎的測試向量產生方法

這個計畫提案提供在 3DIC 上之電熱模擬、實體設計、架構探索、系統構裝，與測試驗證之演算法。本計畫已累計發表 10 篇國際期刊論文及 41 篇國際研討會論文，並申請/獲得二國內專利與三件美國專利。

英文摘要：

The rapid scaling of silicon technology has enabled the dramatic success of integrated circuit (IC) design during the past few decades, allowing millions of transistors to be fully integrated onto a single chip. However, the gain from technology scaling will be less and less and the Moore’s Law is predicted to reach the limit in 16nm technology node. The 50-60% system performance improvement per technology node, historically seen through the 90nm node, will drop to under a 20% improvement per node beyond 45nm node if the system architectures remain planar. Therefore the best way to lower capacitance, maintain signal integrity, and keep chips blazing along at ever faster multi-gigahertz speeds is to find a shorter distance between two points: going vertical. A three-dimensional chip (3D IC) is a stack of multiple dies with many direct connections tunneling through them (Through-silicon-via,

TSV), dramatically reducing global interconnect lengths and increasing the number of transistors that are within one clock cycle of each other. Other advantages for 3D integration include the following: power efficiency, significant produce miniaturization, cost reduction, and modular design for improved time to market. Consequently, we need to have corresponding EDA tools to help such designs effectively.

In this project, we have proposed five research topics to resolve some core issues in 3D integration design automation to assist current incomplete EDA researches and tools, including:

1) Stochastic electro-thermal simulation and power optimization for 3D ICs
2) Physical design in 3D IC integration
3) Architecture exploration and robust synthesis framework for 3D regular logic structure
4) 3D-SIC and 3D-SIP design planning
5) Computational-intelligence-based test pattern generation for verification and test of 3D integration

This proposed project has provided a set of methodology on thermal, physical design, architecture, package design, and verification/testing for 3D integrated circuit. This project has generated 10 journal papers and 41 international conference papers. We have also filed/acquired 5 patents (2 ROC patens an 3 US patents).

行政院國家科學委員會補助專題研究計畫 ■ **成果報告**
□ **期中進度報告**

針對 3D 整合之電子設計自動化技術開發 — 總計劃(2/2)

計畫類別：□ 個別型計畫 ■ 整合型計畫
計畫編號：NSC 99-2220-E-009-034
執行期間：99年8月1日至100年7月31日

計畫主持人：陳宏明、周景揚
共同主持人：李育民、李毅郎、江蕙如、黃俊達、陳宏明、劉建男、溫宏斌

成果報告類型(依經費核定清單規定繳交)：□精簡報告 ■完整報告

總計畫: 針對 3D 整合之電子設計自動化技術開發(2/2)
計畫編號：NSC 99-2220-E-009-034

子計畫一： 三維度積體電路的隨機電熱模擬及其對功率最佳化的應用
計畫編號：NSC 99-2220-E-009-035

子計畫二： 三維電路整合之實體設計系統
計畫編號：NSC 99-2220-E-009-036

子計畫三： 針對三維規則型邏輯結構之架構探索及穩健合成系統開發
計畫編號：NSC 99-2220-E-009-037

子計畫四： 立體堆疊晶片與系統級構裝之設計最佳化研究
計畫編號：NSC 99-2220-E-009-038

子計畫五： 應用在驗證與測試 3D IC 整合過程中以計算智慧為基礎的測試向量產生方法
計畫編號：NSC 99-2220-E-009-039

執行單位：國立交通大學電子工程學系(所)、國立交通大學電信工程學系(所)、國立交通大學資訊工程學系(所)

中 華 民 國 100 年 10 月 31 日

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關鍵詞: 3D 整合、電子設計自動化、超越摩爾定律、矽穿孔

Abstract

The rapid scaling of silicon technology has enabled the dramatic success of integrated circuit (IC) design during the past few decades, allowing millions of transistors to be fully integrated onto a single chip. However, the gain from technology scaling will be less and less and the Moore's Law is predicted to reach the limit in 16nm technology node. The 50-60% system performance improvement per technology node, historically seen through the 90nm node, will drop to under a 20% improvement per node beyond 45nm node if the system architectures remain planar. Therefore the best way to lower capacitance, maintain signal integrity, and keep chips blazing along at ever faster multi-gigahertz speeds is to find a shorter distance between two points: going vertical. A three-dimensional chip (3D IC) is a stack of multiple dies with many direct connections tunneling through them (Through-silicon-via, TSV), dramatically reducing global interconnect lengths and increasing the number of transistors that are within one clock cycle of each other. Other advantages for 3D integration include the following: power efficiency, significant produce miniaturization, cost reduction, and modular design for improved time to market. Consequently, we need to have corresponding EDA tools to help such designs effectively.

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This proposed project has provided a set of methodology on thermal, physical design, architecture, package design, and verification/testing for 3D integrated circuit. This project has generated 10 journal papers and 41 international conference papers. We have also filed/acquired 5 patents (2 ROC patens an 3 US patents).

Keywords: 3D Integration, Electronic Design Automation, Beyond Moore's Law, TSV

1. 前言

由於半導體製造製程不斷演進，現今的電路設計面臨重大考驗，其中一個關鍵是被電子業奉為金科玉律的摩爾定律。但想維持摩爾定律所言的每18個月在相同單位面積內增加1倍的電晶體數，以現有的製程微縮(Technology Scaling)作法將愈來愈困難，在90nm 技術結點(Technology node)平均可得到50%-60%系統效能的改進，在45nm 以下只能得到不到20%的改善。市場並預估到16nm 時將為其極限。與摩爾定律相違背的另一發展方向於焉產生，即為向垂直或向上方向發展的立體堆疊晶片整合設計(3D Integration)。它必須讓不同功能性質，甚至不同基板的晶片，各自應用最合適的製程分別製作後，再利用矽穿孔（Through-Silicon Via，TSV）技術進行立體堆疊整合。理論上，這種做法可縮短金屬導線長度及連線電阻，並減少晶片面積，具有體積小、整合度高、效率高、耗電量及成本更低的特點，能符合數位電子輕薄短小發展趨勢要求。也因為這些特點，目前包括多核心處理器、記憶體等應用上，都被視為可從3D 晶片技術中，獲得更高價值的應用。

3D 整合技術事實上包含了非常多種技術，可粗略分成下列四種：3D system-in-Package (3D-SIP, 3D 系統級封裝）、3D Wafer-Level-Packaging (3D-WLP, 3D 晶圓級封裝）、3D Stacked-IC(3D-SIC)和3D-IC，Figure 1.為這些技術的示意圖，Figure 2. 則顯示了其中幾種3D 垂直連結技術。基本上要將晶片結構由平面轉為立體，這中間存在許多挑戰，例如在晶圓廠的矽製程上，便會出現晶圓IC 線路與實體設計、晶圓孔隙的穿透及填滿(via-first or via-last)、晶圓薄化(thinned silicon)拋光、晶粒／晶圓的連結等技術問題。其它重要問題如製程變異(process variation)、3D 散熱與功率最佳化、異質整合、構裝與晶片連動設計(codesign)及3D 晶片測試與驗證，在在顯示此整合技術亟需大量人力與深入研究，才能突破半導體微縮的瓶頸，將此立體堆疊整合技術的優點完全實現。

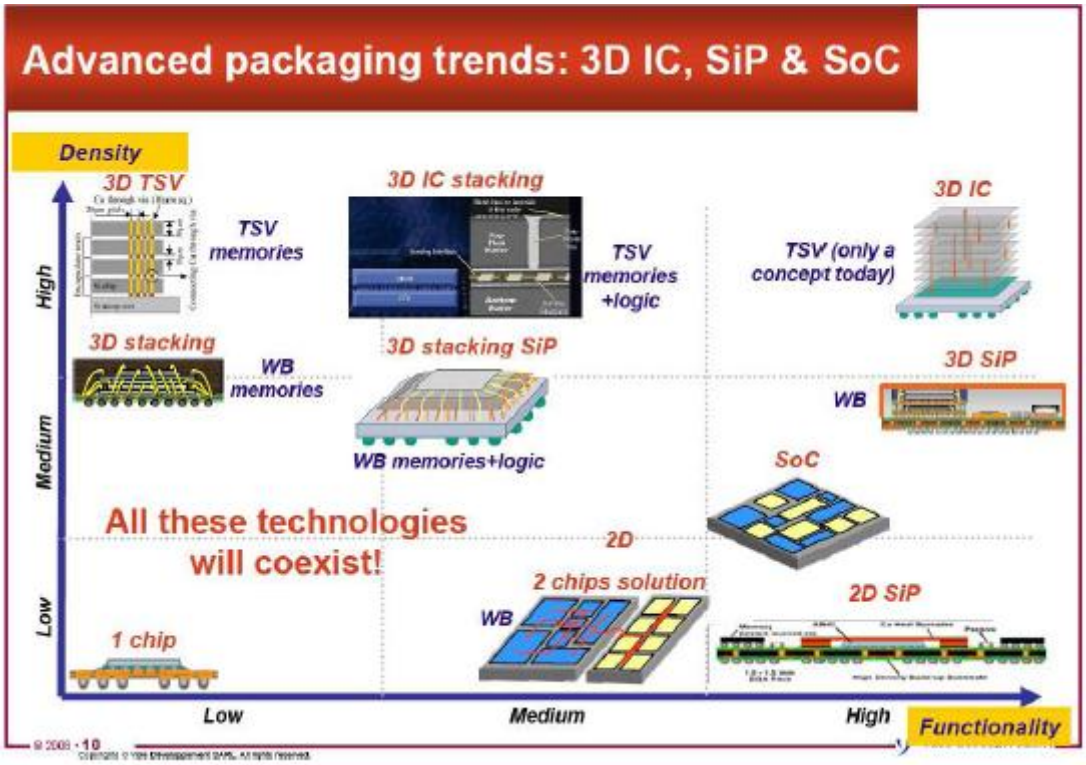

Figure 1: 3D 整合技術趨勢 (from Yole Development SARL)

Figure 3.顯示了目前發展3D 技術在設計與架構上的挑戰，EDA 工具明顯為不可或缺的重要 利器。為了能提供上述各個問題的解決途徑，並藉著自動化工具來提升效率，總計畫結合數個優秀的EDA研發團隊，規畫一個在目前被提出或使用的3D 技術設計自動化整合方案，為幾個核心的技術問題找到解決方法。子計畫一針對製程變異進行統計型電熱分析研究，並加入功率最佳化之低功率技術。子計畫二發展電路切割與擺置的自動化系統，並開發兼具考量導線長度與散熱的繞線系統。子計畫三則提出三維規則型邏輯架構，探索更佳的硬體架構，並於其上發展具有高效能及高容錯能力的合成演算法。子計畫四則對於3D 構裝技術提出效能導向的矽穿孔規畫與封裝-系統電路板之繞線系統。子計畫五則是將立體堆疊整合設計時的測試與驗證難度降低，並將其所用方法與設計流程整合，成功驗證3D晶片設計與測試矽穿孔之實現。Figure 4.展示我們子計畫與總計畫的整合，顯示各子計畫為環繞並支撐總計畫的核心元件。在各子計畫間，我們使用矽穿孔與製程之共同目標進行溝通與整合。

由於立體堆疊整合技術所帶來的廣大市場，EDA 公司也開始發展相對應的軟體，但由於目前各個晶圓廠(如TSMC)、封測廠(如日月光)、IDM(如IBM)及研究與育成機構(如IMEC 及ITRI)有各種不同的整合與矽穿孔模型與技術，使得真正的EDA 工具發展並不容易。另一方面，根據相關業者指出，以台灣晶圓製造實力，發展3D 晶片頗具優勢，因為3D 晶片技術是屬於晶圓製造的層級，且構裝占有舉足輕重的地位，而台灣的晶圓製造和封裝皆是世界第一，半導體產業聚落完整，在發展3D 晶片上已具有先天上的優勢。因此我們相信，以我們所提出的研究方向，再加上產官學界的積極合作，期在3D EDA領域得到正面回應，並有機會將我們的研究成果納入量產的設計與驗證流程。

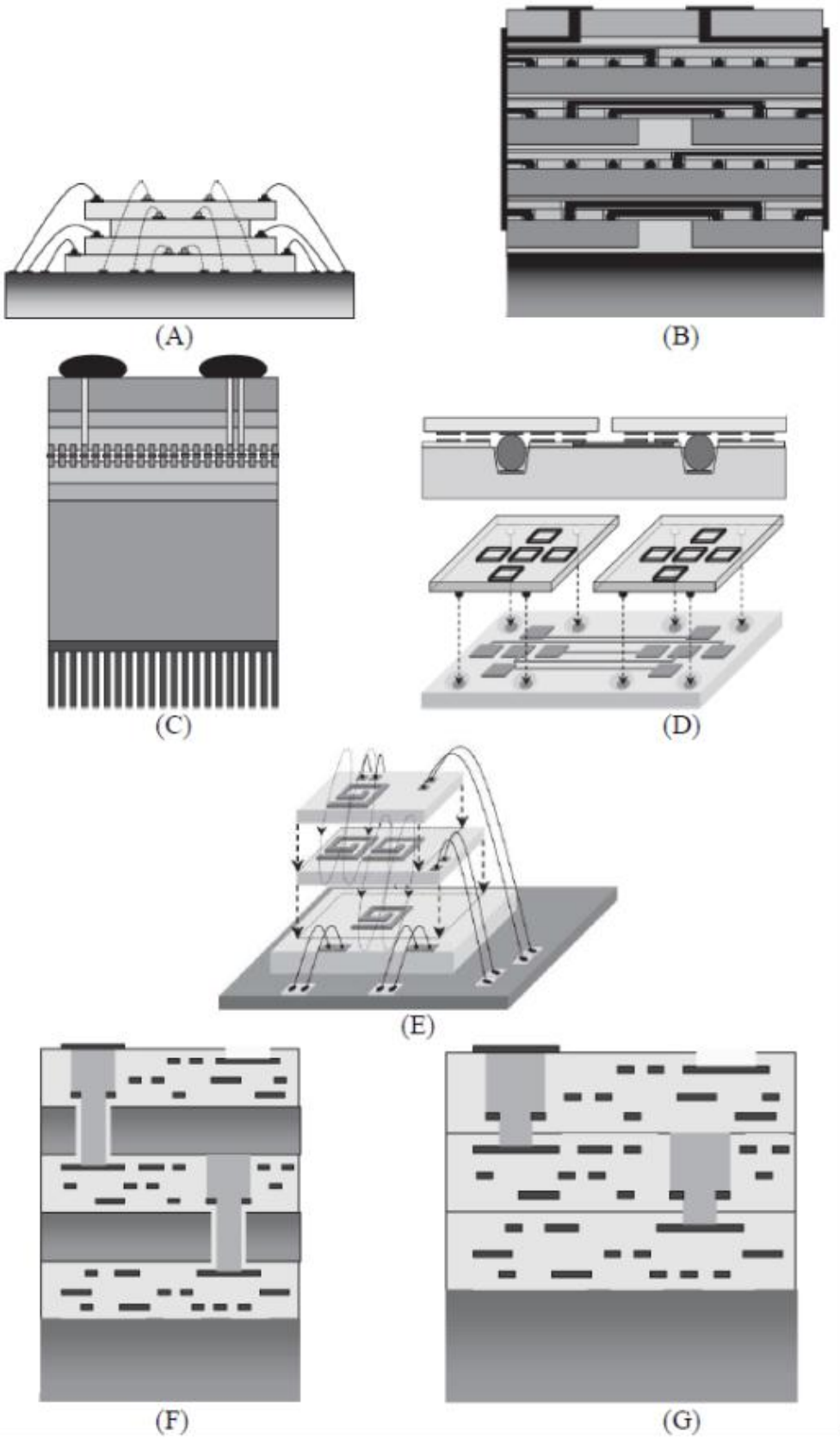

Figure 2. 垂直連結技術（A)線連接，(B)前對後微觸點連接，(C)前對後微觸點連接，(D）電容藕合無觸點連接，(E）電感藕合無觸點連接，(F）體效應技術直通矽穿孔和(G）絕緣層上覆矽技術直通矽穿孔

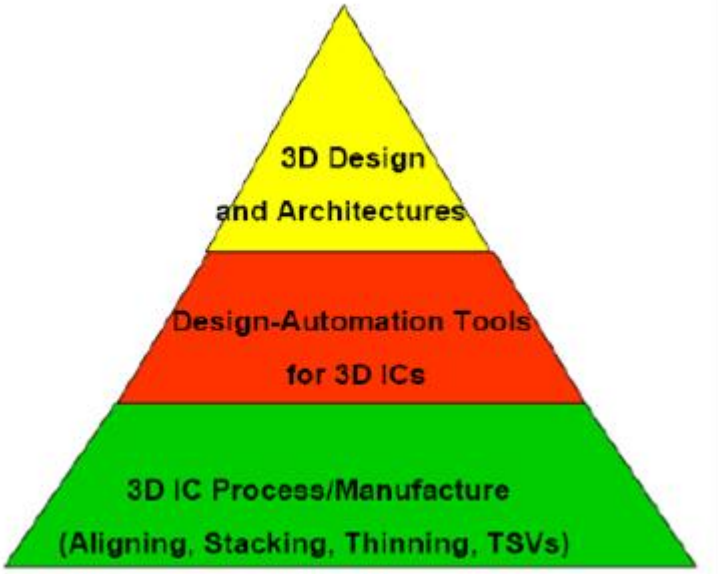

Figure 3. 3D EDA/設計/架構的挑戰，EDA 工具明顯為不可或缺之溝通橋樑圖

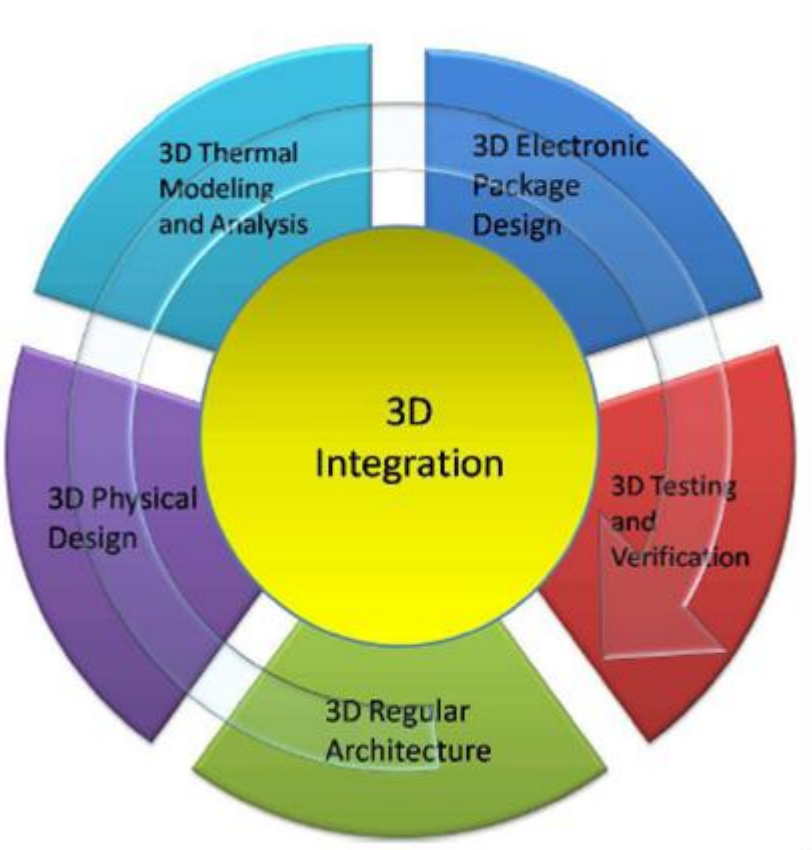

Figure 4. 3D 整合設計總計畫與子計畫的整合，各子計畫間均可連結發展，並合力支援 3D 整合總計畫之技術開發

2. 各子計畫成果報告

本總計畫包括下列五個子計畫：

總計畫: 針對 3D 整合之電子設計自動化技術開發
計畫主持人：陳宏明副教授、周景揚教授
計畫編號：NSC 99-2220-E-009-034

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計畫編號：NSC 99-2220-E-009-035

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計畫主持人：李毅郎副教授、江蕙如副教授
計畫編號：NSC 99-2220-E-009-036

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計畫主持人：黃俊達副教授
計畫編號：NSC 99-2220-E-009-037

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計畫主持人：陳宏明副教授、劉建男副教授
計畫編號：NSC 99-2220-E-009-038

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計畫主持人：溫宏斌助理教授
計畫編號：NSC 99-2220-E-009-039

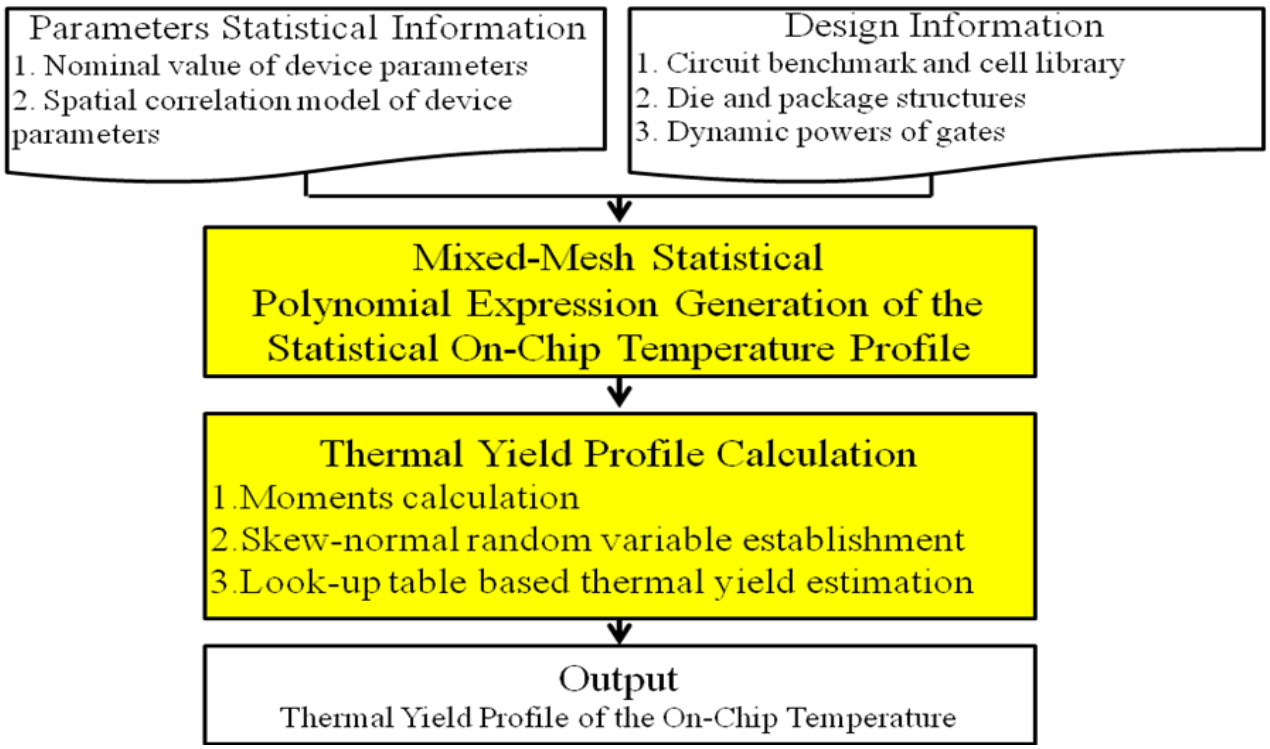
本章節對各子計畫的報告成果作摘要式描述，詳細敘述請參考各子計畫完整報告。

2.1 子計畫一：三維度積體電路的隨機電熱模擬及其對功率最佳化的應用

主要創新技術

1. 高效率之熱良率分析技術

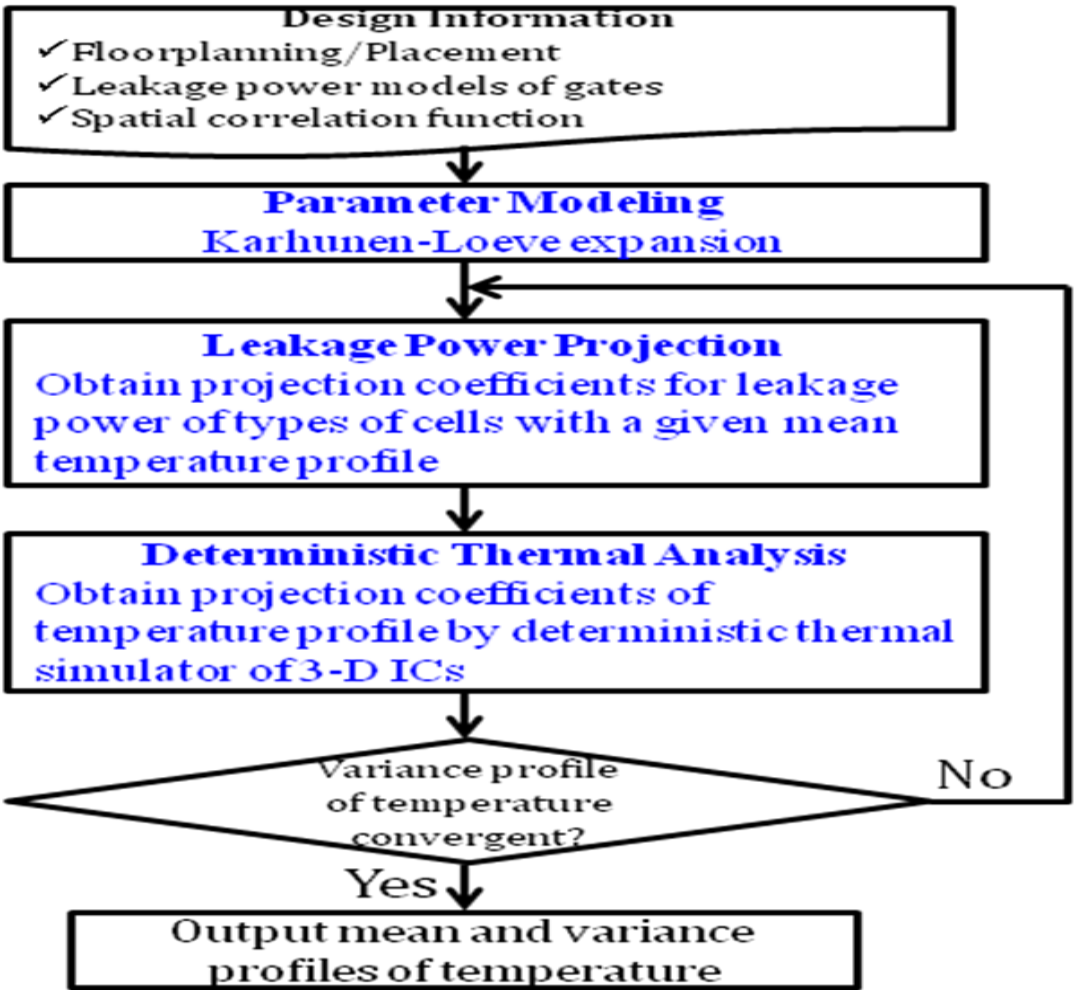
在此子計畫中，我們發展了一個利用混合網格來分析在考慮製程變異下晶片上具有隨機特性的溫度分佈。如 Figure 5 所示，當元件參數統計特性的資訊以及設計電路的資訊被給定之後，我們首先利用混合網格(mixed-size grid)來產生用來近似溫度的隨機多項式。此混合網格分析方法主要是利用一個較密的網格分析晶片上溫度分佈的期望值。由於要晶片溫度分布的二階以及三階統計特性可藉由執行許多次無隨機變異的溫度分析來近似之。因此，為了要達到效能上的提升，我們利用了較為稀疏的網格來執行分析二階以及三階統計特性所需的多次無隨機變異的溫度分析。在得到晶片溫度的期望值、標準差以及歪斜係數之後，我們將在晶片上任意點的隨機溫度近似成歪斜常態(skew-normal)的隨機變數。然後再利用此歪斜常態隨機變數的尾端機率求得晶片上的熱良率分布輪廓(thermal yield profile)。 利用此分析流程，我們能在可接受的準確率之下，使得具有製程變異之晶片溫度分析的效率達到與不考慮製程變異之溫度分析之效率相當的程度。此熱良率分析技術，可有效地提供晶片之相關熱資訊予任何熱導向之積體電路設計流程。



▲Figure 5、高效率之熱良率分析技術流程圖

2. 三維度積體電路隨機電熱模擬技術

基於我們所發展的高效率之熱良率分析技術，在此子計畫中，我們亦發展了一個適用於三維度積體電路考慮製程變異的電熱回授分析技術。如 Figure 6 所示，當設計電路的資訊給定之後，我們首先利用 KLE (Karhunen-Loeve expansion)將具有空間相關性的元件製程參數以一組無相關性的隨機變數來表示之。之後，我們計算晶片上漏電功率分布相對於赫米特多項式(Hermite polynomial)所投影之分布。當以上之漏電功率分布被計算之後，我們對於每個投影之漏電功率分布所產生的溫度分佈效應以命定的熱分析器(deterministic thermal simulator)計算之。之後，晶片上溫度變異數之分佈可以被近似之。由於漏電功率與溫度具有相依性，因此以上分析流程將會重複的執行直到晶片上溫度變異數分佈收斂為止。此隨機電熱模擬技術，可提供三維度晶片上溫度分佈的期望值分佈圖及變異數分布圖予任何熱導向之三維度積體電路設計流程。

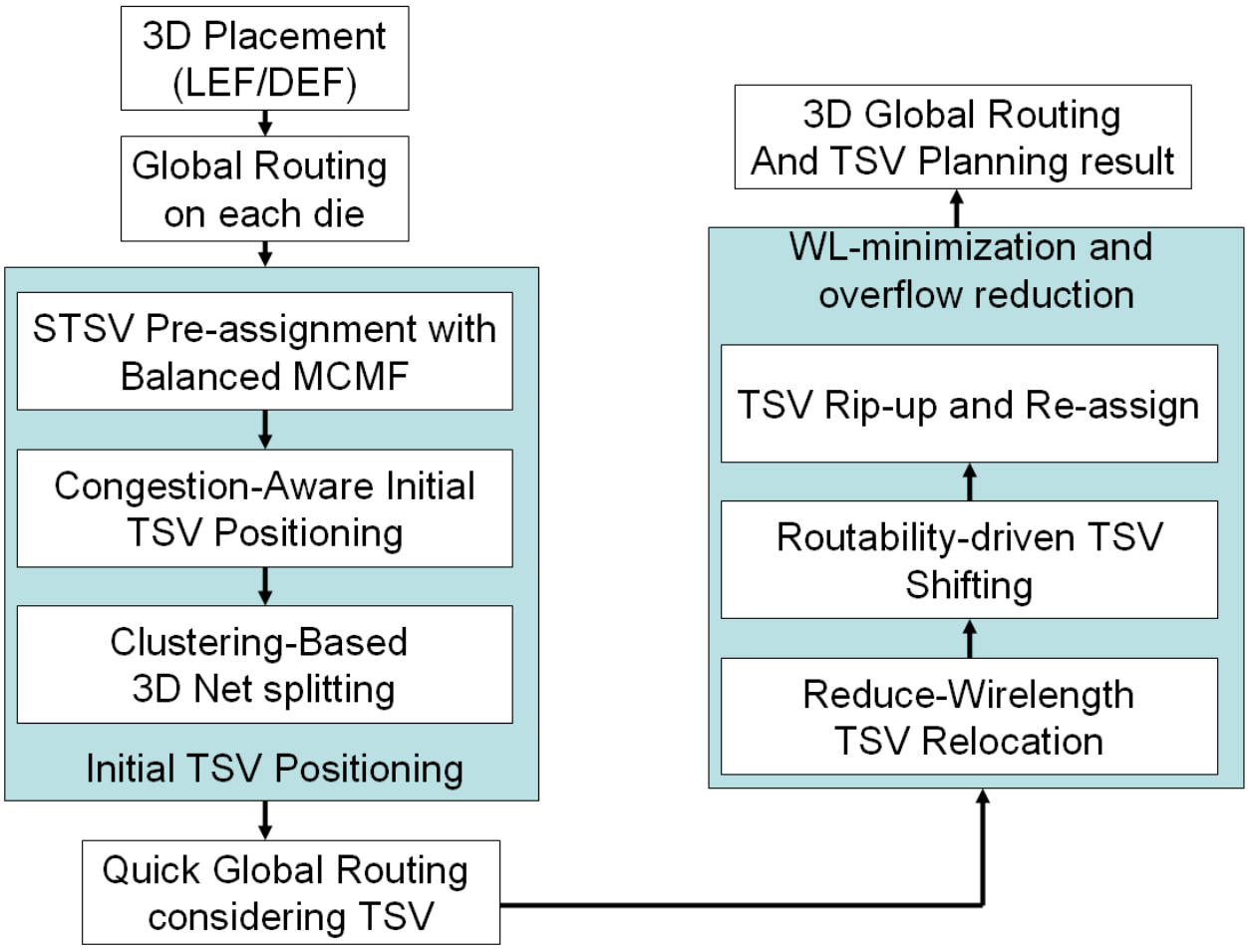


▲Figure 6、三維度積體電路隨機電熱模擬技術流程圖

2.2 子計畫二：三維電路整合之實體設計系統

主要創新技術

在此我們提出了一個可以完成三維積體電路繞線的方法，透過在擺放訊號矽穿孔(signal TSV) 時，考慮實際繞線的擁擠程度狀況以及訊號的線長，我們可以將訊號矽穿孔擺放在較好的位置。更重要的，我們也整合了目前現有的電子設計自動化軟體，完成了整個三維積體電路的繞線。實驗結果顯示我們的三維積體電路繞線系統可以比前人的研究有更短的繞線長度，並且有更少的 Design Rule Checking (DRC) 錯誤。



▲ Figure 7. 三維積體電路繞線系統流程

Comparison of routing result with via-first TSV

	Cong [1]	Zhang [2]	Kim [3]	Ours
NCTU-gr	1.08	1.03	1.03	1
SOC Encounter	1.05	1.04	1.02	1

Comparison of routing result with via-last TSV

	Cong [1]	Zhang [2]	Kim [3]	Ours
NCTU-gr	1.17	1.04	1.06	1
SOC Encounter	1.10	1.03	1.03	1

▲ Figure 8. 三維積體電路繞線結果

2.3 子計畫三：針對三維規則型邏輯結構之架構探索及穩健合成系統開發

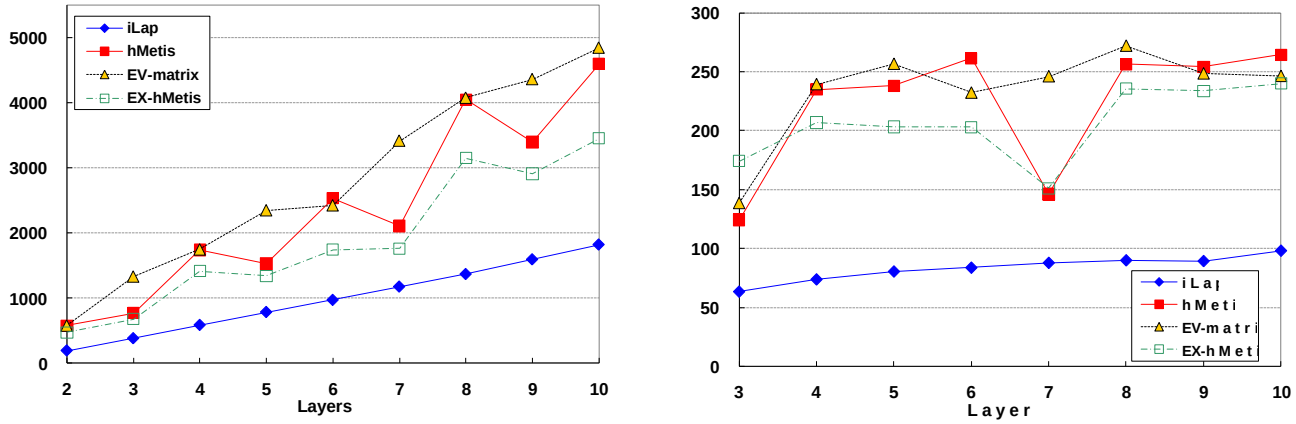
主要創新技術

1. Layer-aware design partitioning for through-silicon via minimization

Three-dimensional (3D) design technology, which has potential to significantly improve design performance and ease heterogeneous system integration, has been extensively discussed in recent years. This emerging technology allows stacking multiple layers of dies and typically resolves the vertical inter-layer connection issue by through-silicon vias (TSVs). However, TSVs also occupy significant silicon estate as well as incur reliability problems. Therefore, the deployment of TSVs must be very judicious in 3D designs.

We propose an iterative layer-aware partitioning algorithm, named iLap, for TSV minimization in 3D structures. iLap iteratively applies multi-way min-cut partitioning to gradually divide a given design layer by layer in the bottom-up fashion. iLap applies layer-aware partitioning at each iteration utilizing hMetis as the kernel of its partitioning engine. Meanwhile, iLap also properly fulfills a specific I/O pad constraint incurred by 3D structures to further improve its outcome. Moreover, our proposed framework can obviously co-work with any multiway min-cut partitioning engines. It implies that a better engine (if any) may be adopted for better 3D partitioning results in the future.

Next, Fig. 9(a) depicts the average TSV count over 14 test cases as a function of the number of layers; and three points are worth pointing out. Firstly, the more layers a design gets partitioned into, the more TSVs it generally requires. Secondly, iLap is the all-time winner from 2 layers to 10 layers among four methods. Thirdly, unlike the other three methods, the number of TSVs required by iLap raises very smoothly as the number of layers increases. From Fig. 9(b), it is evident that the standard deviation of TSV count associated with iLap is far better than those of the other three. As previously mentioned, a TSV occupies significant silicon estate so that high standard deviation of TSV count potentially worsens area imbalance among individual layers and even lowers the yield of a design. We believe a good TSV-minimized 3D partitioning solution can serve as a good starting point for further tradeoff operations between TSV count and wirelength.



(a)TSV count (b) Standard deviation of TSV count

Figure 9. Experimental results of our proposed framework.

2. Architectural exploration of 3D regular structures

The emerging 3D technology, which stacks multiple dies within a single chip and utilizes through-silicon vias (TSVs) as vertical connections, is considered a promising solution for achieving better performance and easy integration. Similarly, a generic 2D FPGA architecture can evolve into a 3D one by extending its signal switching scheme from 2D to 3D by means of TSVs. However, replacing all 2D switch boxes (SBs) by 3D ones with full vertical connectivity is found both area-consuming and resource-squandering. Therefore, it is possible to greatly reduce the footprint with only minor delay increase by properly tailoring the structure and deployment strategy of 3D SB. We perform a comprehensive architectural exploration of 3D FPGAs. Various architectural alternatives are proposed and then evaluated thoroughly to pick out the most appropriate ones with a better area/delay balance. In the baseline BSL, as shown in Fig. 10(a), all SBs are fully connected 3D-SBs. An IS architecture adopts the same type of partially connected 3D-SBs for all SBs instead, as in Fig. 10(b). In an ES architecture as shown in Fig. 10(c), fully connected 3D-SBs are partially distributed in a regular fashion.

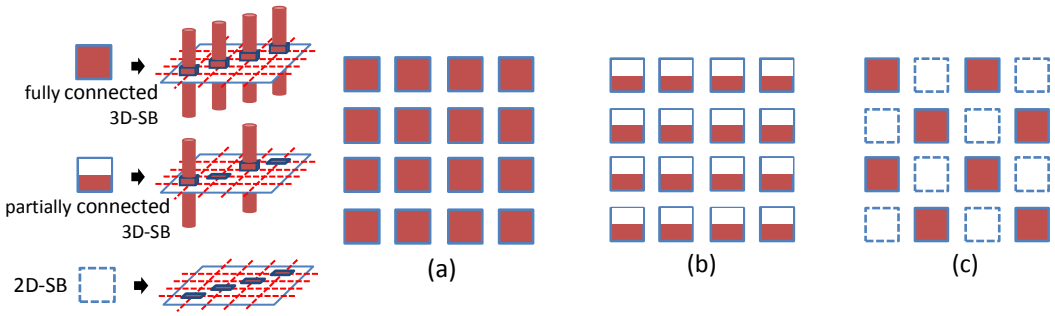


Figure 10. Different proposed 3D regular structures.

Fig. 11 reports the area and delay of different IS architectures, in which all values are normalized to that of the BSL. It shows that both the sizes of an SB and a tile basically decrease linearly as the number of TSVs in a 3D-SB decrease. However, though reducing the number of TSVs in an 3D-SB can save area, it is very likely to harm delay at the same time. To realize what the exact impact on delay is, the benchmark circuits are mapped onto different IS architectures and the BSL through the reference synthesis framework.

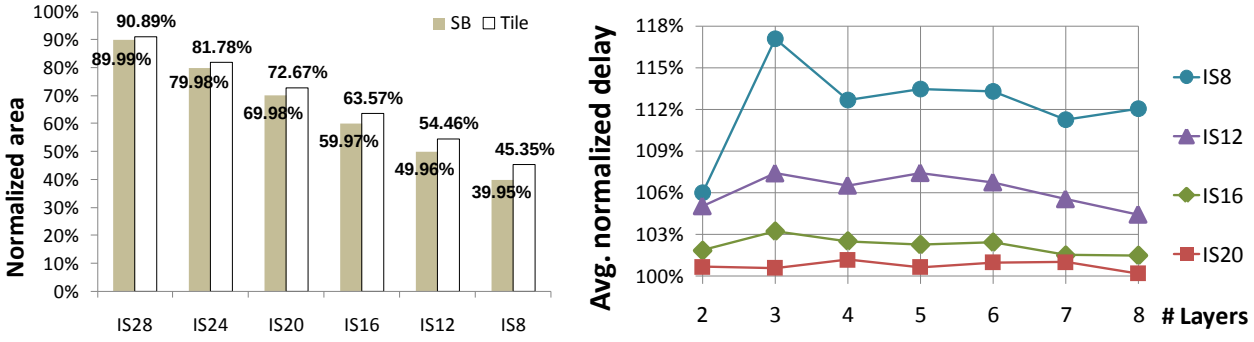


Figure 11. Area and delay trade-off among different architectures.

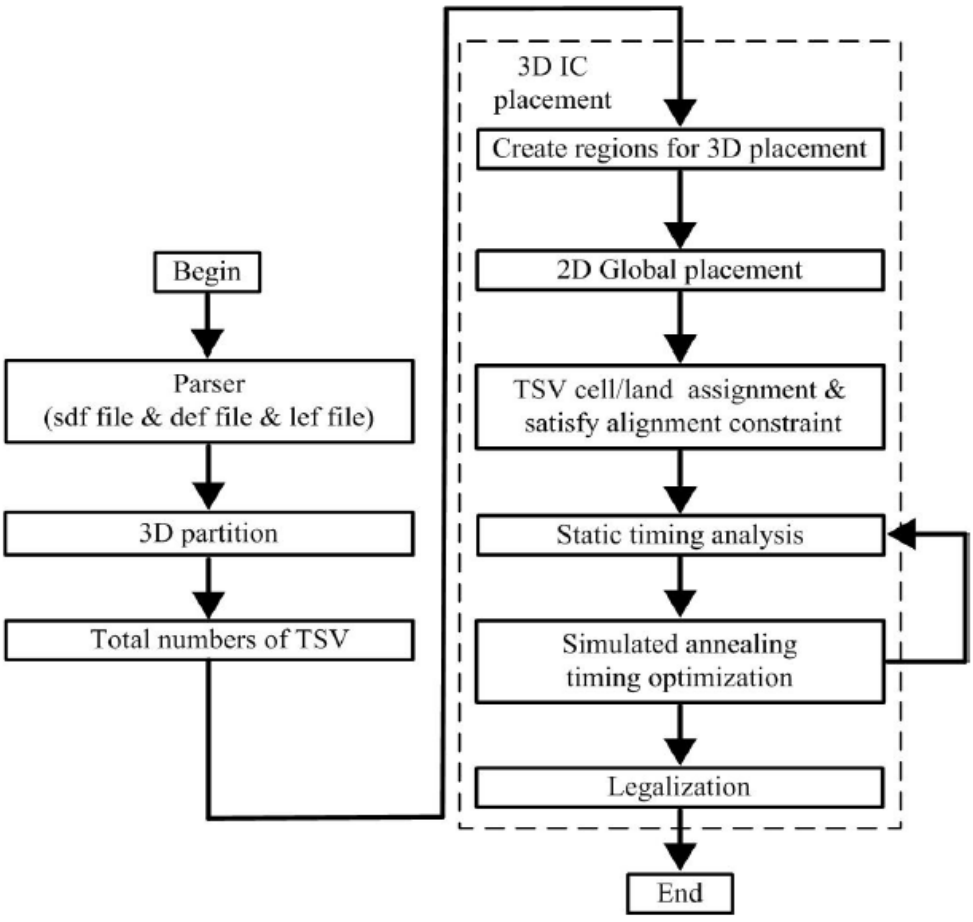
Moreover, the hybrid methods, including sparse architecture (SP) and sunny egg (SE), are also proposed to further minimize the area of 3D FPGAs by using the techniques of IS and ES at the same time. Those architectures are explored thoroughly and evaluated objectively. After comparing all these architectures, two generic 3D FPGA architectures are suggested, which save the most area with acceptable delay penalty.

2.4 子計畫四：立體堆疊晶片與系統及構裝之設計最佳化研究

主要創新技術

1. 3D IC Timing Driven Placement (3D 晶片之時序導向佈局)

在此子計畫中，我們發展了一套在 3D 晶片上自動佈局的技術。此方法在全域佈局(global placement)中利用 partition-based placement 與 greedy 演算法(Figure 12)，考量 cell 之間的連線關係，並同時確保 through silicon via (TSV) 的 alignment constraint 不會被違反。在 detailed 佈局中並在流程中利用靜態時序分析與 simulated annealing 來調整 cell 與 TSV 的位置，縮短 critical path 的線長，使佈局結果符合 timing rule 的要求，而可工作在最佳時脈頻率(clock frequency)上。

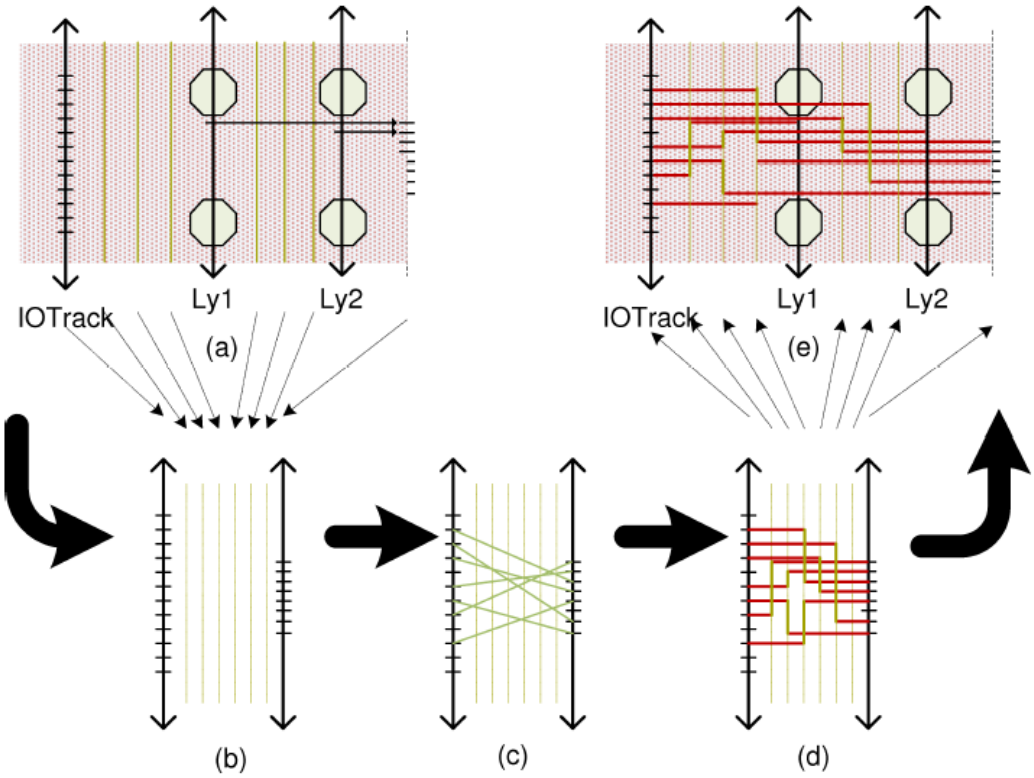


▲Figure 12、3DIC 之時序導向佈局流程

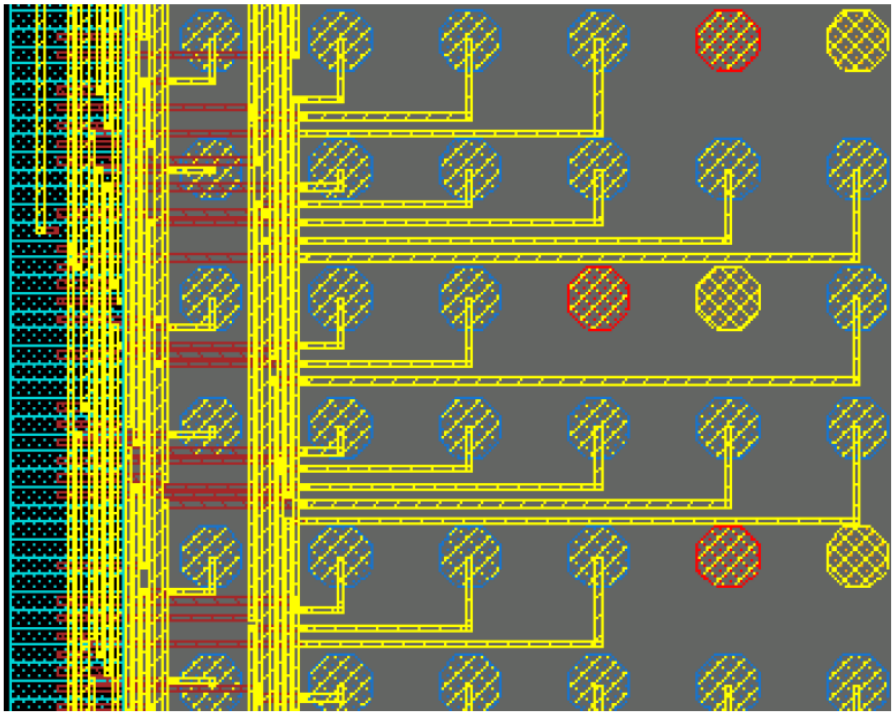
2. Effective Flip-Chip Routing Methodology via Pseudo Single Redistribution Layer

我們提出了一個在 flip-chip 上有效率的 redistribution layer (RDL) 繞線方法。RDL 繞線是為解決 RDL Bump 到 peripheral IO 的連線問題。由於繞線資源稀少，很多情況下 RDL 繞線即使以人工處理也無法在一層 metal layer 中完成。我們提出了一個啟發式演算法，利用 pseudo layer 的概念，將 RDL 繞線問

題轉換成 channel route problem，使用 Left-Edge 演算法在兩層 metal layer 上繞線來解決這個問題(Figure 13, 14)。此方法可充分利用僅有的繞線資源，在連線相當擁擠的狀況下完成 Bump 到 IO 的接線，並符合 design constraint 的要求。



▲Figure 13、RDL 繞線規劃步驟圖



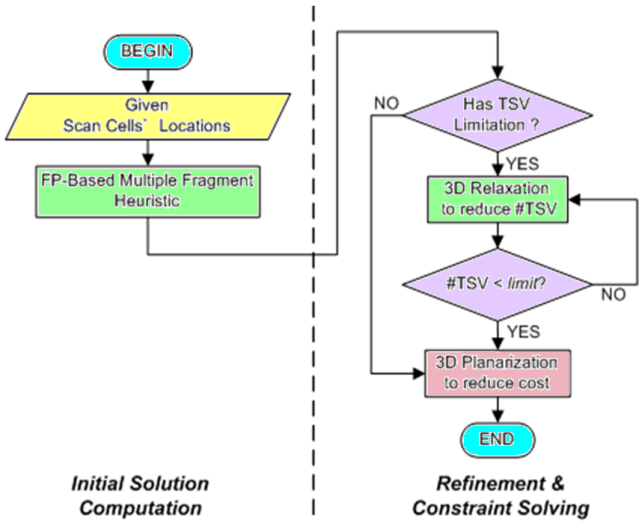
▲Figure 14、自動化 RDL 繞線結果

2.5 子計畫五：應用在驗證與測試 3D IC 整合過程中以計算智慧為基礎的測試向量產生方法

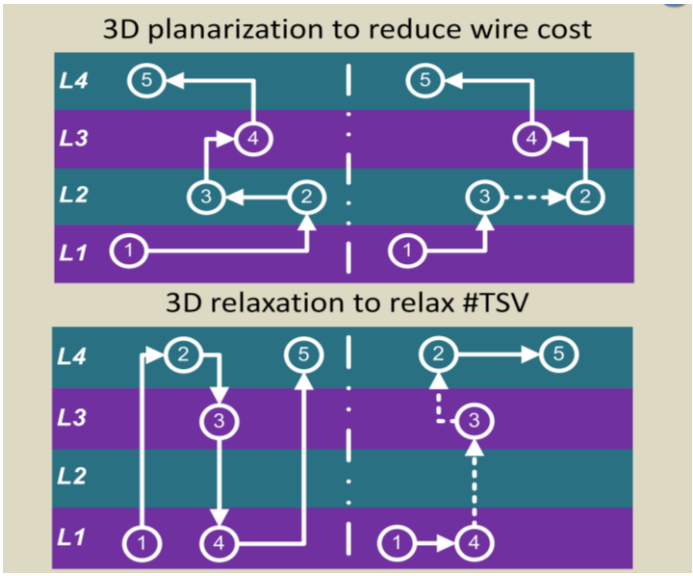
主要創新技術

1. Through-Silicon-Via (TSV)-constrained Scan Chain Reordering for Three-dimensional (3D) Integrated Circuits

良率問題在三維積體電路中極為重要，良率與製造成本息息相關，因此 Design for Testability 在三積體電路中更是不可或缺的一項技術，scan-chain based 的測試是 DFT 中常見的方法，我們提出了快速的演算法(3D-Multi-Fragment-Heuristic, 3D 平坦化與 3D 鬆弛化)來幫助我們決定 scan-chain 的順序，用來降低繞線長度以及功能消耗。



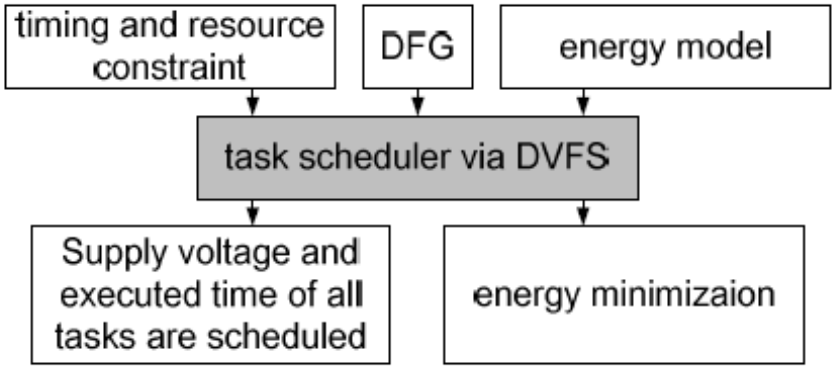
▲Figure 15. 演算法設計流程



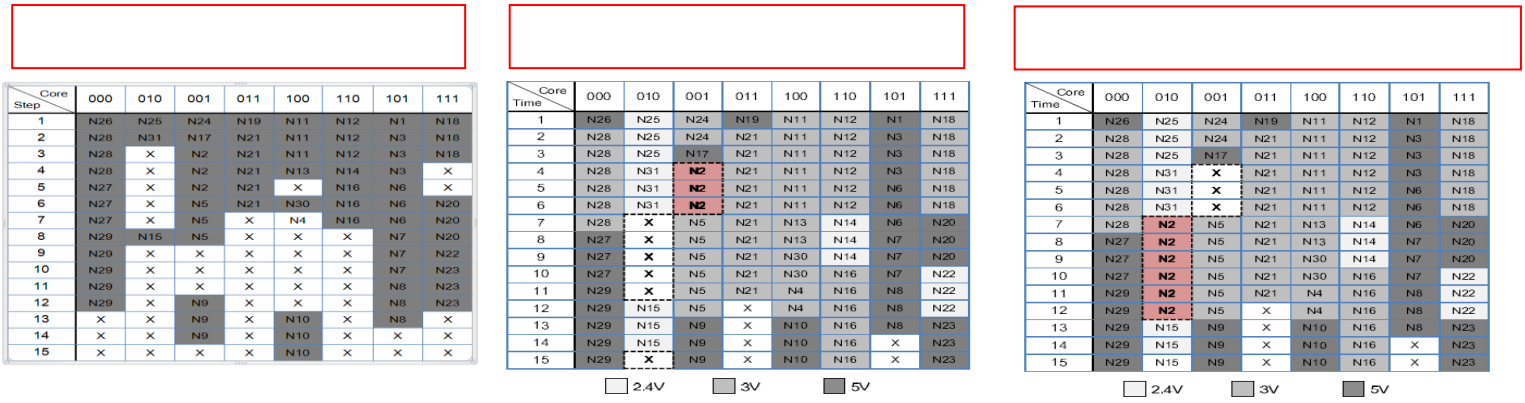
▲Figure 16. 三維平坦化與鬆弛化範例

2. Enhancing Energy-Efficient Task Scheduling on 3D Multi-Core Processors by Dynamic Remapping

三維積體電路比傳統的二維積體電路有著許多顯著的優勢，但三維積體電路比二維積體電路面臨了更嚴重的熱問題，因此我們提出了 task scheduling 的演算法並配合 DVFS(動態電壓頻率規劃)的技術，調整每個 task 執行的電壓頻率，進而平衡三維積體電路中每一層的溫度分佈。



▲Figure 17. 演算流程



▲Figure 18. 演算法主要步驟

3. 本計畫執行成果之論文

子計畫一:

I. 期刊論文

1. Yu-Min Lee and Po-Yi Chiang, “Effective Sleep Transistor Sizing Algorithm for Leakage Power Reduction”, *International Journal of Electrical Engineering* (*IJEE*), vol. 16, no. 5, pp. 421-431, October 2009.
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3. Huai-Chung Chang, Pei-Yu Huang, Ting-Jung Li and Yu-Min Lee, “Statistical Electro-Thermal Analysis with High Compatibility of Leakage Power Models”, *International SOC Conference* (*SOCC*) 2010.
4. Ting-Jung Li, Shu-Han Whi, Chi-Wen Pan and Yu-Min Lee, “Efficiently Adaptive Thermal Simulator for 3D-ICs”, *in preparation*.
5. Shu-Han Whi and Yu-Min Lee, “Dual Supply Voltage Assignment in 3D ICs Considering Thermal Effects,” *The 16th Workshop on Synthesis And System Integration of Mixed Information Technologies (SASIMI)*, 2010.
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3. Yih-Lang Li, Yu-Ning Chang, and Wen-Nai Cheng, “A Gridless Routing System with Non-Slicing Floorplanning-Based Crosstalk Reduction on Gridless Track Assignment”, *ACM Trans. on Design Automation of Electronic Systems, Vol 16, No. 2, Article 19 (1-25),* March 2011.

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1. Jiang, I.H.-R, “Generic integer linear programming formulation for 3D IC partitioning”, *22nd IEEE International SOC Conference (SOCC-2009),* Belfast, UK, Sep. 2009.
2. Wan-Yu Lee and Iris Hui-Ru Jiang, “Variability tolerance on throughput and power for 3D chip-multiprocessor”, 1*8th International Workshop on Logic & Synthesis (IWLS-2009),* Berkeley, CA, Jul. 2009.
3. Wen-Hao Liu, Yih-Lang Li and Kai-Yuan Chao, “High-Quality Global Routing for Multiple Dynamic Supply Voltage Designs,” *to appear in International Conference on Computer-Aided Design (ICCAD 2011),* San Jose, California, 2011.
4. Yen-Hung Lin, Yong-Chan Ban, David Z. Pan and Yih-Lang Li, “DOPPLER: DPL-aware and OPC-friendly Gridless Detailed Routing with Mask Density Balancing,” *to appear in International Conference on Computer-Aided Design (ICCAD 2011),* San Jose, California, 2011.
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10. Wen-Hao Liu, Wei-Chun Kao, Yih-Lang Li, and Kai-Yuan Chao, “Multi-Threaded Collision-Aware Global Routing with Bounded-Length Maze Routing”, *in Proceedings of ACM/IEEE Design Automation Conference (DAC-2010),* Anaheim, CA, June 2010.
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8. Ya-Shih Huang, Yang-Hsiang Liu and Juinn-Dar Huang, "Layer-Aware Design Partitioning for Vertical Interconnect Minimization," *Proc. of IEEE Computer Society Annual Symposium on VLSI*, pp. 144–149, Jul. 2011. (Best Paper Award)

子計畫四:

I. 期刊論文

1. C.-Y. Lin, H.-C. Lin and H.-M. Chen, “On Reducing Test Power and Test Volume by Selective Pattern Compression Schemes,” *IEEE Transactions on Very Large Scale Integration Systems(TVLSI)* 2010.
2. R.-J. Lee and H.-M. Chen, "Fast Flip-Chip Pin-Out Designation Respin for Package-Board Codesign," *IEEE Transactions on Very Large Scale Integration Systems*, v.17, no.8, pp.1087-1098, August 2009 (TVLSI-Aug-09)
3. M.-C. Wu, M.-C. Lu, H.-M. Chen, and J.-Y. Jou, "Performance-Constrained Voltage Assignment in Multiple Supply Voltage SoC Floorplanning," , *ACM Transactions on Design Automation of Electronic Systems* (TODAES) 2009
4. C.-Y. Lin, L.-C. Hsu, and H.-M. Chen, "On Reducing Test Power, Volume and Routing Cost by Chain Reordering and Test Compression Techniques," in *IEICE Transactions*, 2010

II. 會議論文

1. C.-C. Hsiao and H.-M. Chen, "On Distinguishing Process Corners for Yield Enhancement in Memory Compiler Generated SRAM," *Proc. of IEEE International Workshop on Memory Technology, Design, and Test (MTDT-09),* August 2009
2. F.-Y. Fan, H.-M. Chen, and I-M. Liu, "Technology Mapping with Crosstalk Noise Avoidance," *ACM/IEEE ASP-DAC-10*, January 2010.
3. C.-Y. Lin and H.-M. Chen, "A Novel Two-Dimensional Scan-Control Scheme for Test-Cost Reduction," *Proceedings of the 20th VLSI Design/CAD Symposium, Hualien, Taiwan*, August 2009.
4. R.-J. Lee and H.-M. Chen, "Row-Based Area-Array I/O Design Planning in Concurrent Chip-Package Design Flow," *Proc. of IEEE Asia and South Pacific Design Automation Conference*, January 2011 (ASP-DAC-11)
5. T.-Y. Tsai, R.-J. Lee, C.-Y. Chin, C.-Y. Kuan, H.-M. Chen, and Y. Kajitani, "On Routing Fixed Escaped Boundary Pins for High Speed Boards," *Proc. of IEEE Design, Automation and Test in Europe*, March 2011 (DATE-11)
6. C.-Y. Lin, H.-M. Chen, and W.-C. Fang, "A Low Noise and Robust 3D System-in-Package Test Scheme for Optical Biosensor," *IEEE/NIH Life Science Systems and Applications Workshop,* April 2011 (LiSSA-11)
7. Y.-R. Chen, H.-M. Chen, and S.-Y. Liu, "TSV-Based 3D-IC Placement for Timing Optimization," *Proc. of IEEE International System on Chip Conference*, September 2011 (SOCC-11)
8. H.-W. Hsu, R.-J. Lee, and H.-M. Chen, “On Effective Flip-Chip Routing via Pseudo Single Redistribution Layer,” *submit to Proc. of IEEE Design, Automation and Test in Europe*, March 2012 (DATE-12)

子計畫五:

I. 期刊論文

1. Huan-Kai (Pumbaa) Peng, Yu-Hsin (Phoebe) Kuo, and Charles H.-P. Wen, *"Statistical Soft*

Error Rate (SSER) Analysis Considering Uncertainty Due to Process Variation," in submission to *IEEE Transactions on Computers (TC)* 2009.

2. Chien-Hui Liao, Yu-Ze Lin and H.-P. Wen, "Enhancing Energy-Efficient Task Scheduling on 3D Multi-Core Processors by Dynamic Remapping", *submit to IET Computers & Digital Techniques*, 2011.(under review)
3. Chien-Hui Liao, Wei-Ting Chen, Yu-Ze Lin and H.-P. Wen, "Fast Scan-Chain Ordering for 3D-IC Designs under Through-Silicon-Via (TSV) Constraints"*submit to IEEE Transaction on Very Large Scale Integration Systems*, 2011.(under review)

II. 會議論文

1. Pumbaa H.-K. Peng., Charles H.-P. Wen and Jayanta Bhadra, "On Soft Error Rate Analysis Beyond Deep Submicron - A Statistical Perspective", *Proceedings of the International Conference on Computer-Aided Design*, 2009.
2. Yu-Hsin (Phoebe) Kuo, Charles H.-P. Wen and Pumbaa H.-K. Peng, "Accurate Statistical Soft Error Rate (SSER) Analysis Using A Quasi-Monte Carlo Framework With Quality Cell Models", *Proceedings of the ISQED*, 2010
3. Chen-Yuan (Ben) Gao, Chien-Hui (Christina) Liao and Charles H.-P. Wen, "An ILP-based Diagnosis Framework For Multiple Open-Segment Defects, " to appear in *IEEE Workshop on Microprocessor Test and Verification (MTV'09),*December 2009.
4. Lynn C.-L. Chang, Charles H.-P. Wen and Jayanta Bhadra, "Paper 16.1: Speeding up Bounded Sequential Equivalence Checking with Cross-Timeframe State-Pair Constraints from Data Learning, *" Proc. Int'l Test Conference, (ITC'09),* November 2009.
5. *Francisco Torres,* Rohit Srivastava, Javier Ruiz, Charles H.-P. Wen, Mrinal Bose and Jayanta Bhadra, "Poster #16: Portable simulation/emulation stimulus on an industrial-strength SoC," *Proc. Int'l Test Conference, (ITC'09),* November 2009.
6. Wei-Ting Chen, Chia-Chin Chang and H.-P Wen, "Through-Silicon-Via(TSV)-constrained Scan Chain Reordering for Three-dimensional(3D) Integrated Circuits", *SASIMI Workshop*, Oct 2010.
7. Wei-Ting Chen, Chia-Chin Chang and H.-P Wen, "Through-Silicon-Via (TSV)-constrained Scan Chain Reordering for Three-dimensional(3D) Integrated Circuits" *VLSI Design / CAD Symposium*, April 2010.
8. Christina C.-H. Liao and Charles H.-P. Wen, "Performance Validation of Dynamic-Remapping-Based Task Scheduling on 3D Multi-Core Processors", submit to *International Symposium on VLSI Design, Automation and Test (VLSI-DAT),* April 2012. (under review)

4. 專利

年度	所屬計畫名稱	專利名稱	發明人	申請案號	專利申請國別
99	子計畫三: 針對三維規則型邏輯結構之架構探索及穩健合成系統開發	Fine-grained bandwidth control arbiter and the method thereof	黃俊達、林步青、李耿維、周景揚	US 7577780	美國
100	子計畫三: 針對三維規則型邏輯結構之架構探索及穩健合成系統開發	精細頻寬調控的仲裁器及其仲裁方法	黃俊達、林步青、李耿維、周景揚	I332615	中華民國
100	子計畫三: 針對三維規則型邏輯結構之架構探索及穩健合成系統開發	Dynamical sequentially-controlled low-power multiplexer device	陳嘉怡 黃俊達	US 7881241 B2	美國
100	子計畫三: 針對三維規則型邏輯結構之架構探索及穩健合成系統開發	低功率動態序向控制多工器	陳嘉怡 黃俊達	I342670	中華民國
100	子計畫四: 立體堆疊晶片與系統級構裝之設計最佳化研究	Orientation Optimization Method of 2-Pin Logic Cell	施盈安、陳宏明	US 7913219	美國

國科會補助計畫衍生研發成果推廣資料表

日期:2011/10/31

國科會補助計畫	計畫名稱: 總計畫(2/2)	
	計畫主持人: 陳宏明	
	計畫編號: 99-2220-E-009-034-	學門領域: 晶片科技計畫--整合型學術研究計畫

無研發成果推廣資料

99 年度專題研究計畫研究成果彙整表

計畫主持人：陳宏明	計畫編號：99-2220-E-009-034-
計畫名稱：針對 3D 整合之電子設計自動化技術開發--總計畫(2/2)	

成果項目			量化			單位	備註（質化說明：如數個計畫共同成果、成果列為該期刊之封面故事...等）
			實際已達成數（被接受或已發表）	預期總達成數(含實際已達成數)	本計畫實際貢獻百分比		
國內	論文著作	期刊論文	0	0	100%	篇	
		研究報告/技術報告	0	0	100%		
		研討會論文	0	0	100%		
		專書	0	0	100%		
	專利	申請中件數	2	2	100%	件	
		已獲得件數	0	0	100%		
	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（本國籍）	碩士生	2	2	100%	人次	
		博士生	4	4	100%		
		博士後研究員	0	0	100%		
		專任助理	0	0	100%		
國外	論文著作	期刊論文	10	10	100%	篇	
		研究報告/技術報告	0	0	100%		
		研討會論文	41	41	100%		
		專書	0	0	100%	章/本	
	專利	申請中件數	2	2	100%	件	
		已獲得件數	1	1	0%		
	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（外國籍）	碩士生	0	0	100%	人次	
		博士生	0	0	100%		
		博士後研究員	0	0	100%		
		專任助理	0	0	100%		

其他成果 (無法以量化表達之成果如辦理學術活動、獲得獎項、重要國際合作、研究成果國際影響力及其他協助產業技術發展之具體效益事項等，請以文字敘述填列。)	子計畫一: 大學院校奈米元件電腦輔助模擬與設計軟體製作競賽奈米 CMOS 元件組 佳作 子計畫三: IEEE International Symposium on VLSI Design, Automation, and Test 2011 Best Paper Candidate 子計畫三: 九十九學年度大學校院積體電路電腦輔助設計(CAD)軟體製作競賽 定題組 佳作 子計畫三: IEEE Computer Society Annual Symposium on VLSI 2011 Best Paper Award 子計畫四: 九十八學年度大學院校積體電路電腦輔助設計競賽 馬拉松組 佳作

	成果項目	量化	名稱或內容性質簡述
科教處計畫加填項目	測驗工具(含質性與量性)	0	
	課程/模組	0	
	電腦及網路系統或工具	0	
	教材	0	
	舉辦之活動/競賽	0	
	研討會/工作坊	0	
	電子報、網站	0	
	計畫成果推廣之參與（閱聽）人數	0	

國科會補助專題研究計畫成果報告自評表

請就研究內容與原計畫相符程度、達成預期目標情況、研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）、是否適合在學術期刊發表或申請專利、主要發現或其他有關價值等，作一綜合評估。

1. 請就研究內容與原計畫相符程度、達成預期目標情況作一綜合評估

■達成目標

□未達成目標（請說明，以 100 字為限）

□實驗失敗

□因故實驗中斷

□其他原因

說明：

2. 研究成果在學術期刊發表或申請專利等情形：

論文：■已發表 □未發表之文稿 □撰寫中 □無

專利：■已獲得 □申請中 □無

技轉：□已技轉 □洽談中 ■無

其他：(以 100 字為限)

3. 請依學術成就、技術創新、社會影響等方面，評估研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）(以 500 字為限)

在過去數十年間，半導體技術尺度快速縮小，使積體電路設計發展得非常成功，這也使數以百萬計的電晶體可被整合到單一晶片中。然而在製程微縮所得到的好處愈來愈少，市場並預估摩爾定律到 16nm 時將為其極限。進一步來說，如果系統架構仍維持平面放置，在 90nm 技術結點(Technology node)平均可得到 50%-60%系統效能的改進，在 45nm 以下只能得到不到 20%的改善。因此，使電容降低、維持信號完整性、及維持高頻運作晶片的最好方式，是找到兩點間的更短的連接距離，即向上發展或立體堆疊晶片整合。3D 晶片技術是將數個晶片用矽穿孔(TSV)的方式作晶片間的連接，大大降低全域連接(global interconnect)之線長。其它好處包括了低功率、產品極小化、製造成本降低與加快上市時間。然而我們必須研發或提昇 EDA 輔助工具品質提升來克服這個新概念的設計問題。

在這個計畫裡，我們有五個研究主題來幫助目前尚未完整的 3D 整合電子設計自動化研究與設計流程/工具，包括：

(1) 三維度積體電路的隨機電熱模擬及其對功率最佳化的應用

(2) 三維電路整合之實體設計系統

(3) 針對三維規則型邏輯結構之架構探索及穩健合成系統開發

(4) 立體堆疊晶片與系統級構裝之設計最佳化研究

(5) 應用在驗證與測試 3D IC 整合過程中以計算智慧為基礎的測試向量產生方法

這個計畫提案提供在 3DIC 上之電熱模擬、實體設計、架構探索、系統構裝，與測試驗證之演算法。本計畫已累計發表 10 篇國際期刊論文及 41 篇國際研討會論文，並申請/獲得二國內專利與三件美國專利。