A 1-V 50-MHz Pseudodifferential OTA With Compensation of the Mobility Reduction

Tien-Yu Lo, *Student Member, IEEE*, and Chung-Chih Hung, *Senior Member, IEEE*

***Abstract*—This brief presents a high-linearity operational transconductance amplifier (OTA) based on pseudodifferential structures. The linearity is improved by mobility compensation techniques as the device size is scaled down to achieve high speed operation. Transconductance tuning could be achieved by a MOS operating in the linear region. The OTA fabricated in the 0.18-μm CMOS process occupies a small area of 4.5×10^{-3} mm^2. The measured third-order intermodulation (IM3) distortion with a 400 mV$_{pp}$ differential input under 1-V power supply voltage remains below -52 dB for frequency up to 50 MHz. The static power consumption is 2.5 mW. Experimental results demonstrate the agreement with theoretical analyses.**

***Index Terms*—Low supply voltage, operational transconductance amplifier (OTA), strong inversion region, subthreshold region, transconductance tuning.**

I. Introduction

THE CIRCUIT that converts the voltage applied to the input terminals into current at output nodes is generally referred as a V–I converter or an Operational Transconductance Amplifier (OTA). The OTA is a basic building block in analog VLSI applications, including continuous-time filters [1]–[3] and four-quadrant multipliers [4]. The precision of the data signal processing is limited by the performance of the linearity and noise. There are numerous previous works to improve the OTA linearity [6]. On one hand, with the reduction of power supply voltage, the operating range is decreased. On the other hand, linearity based on the MOS transconductance or saturated square-law behavior becomes worse in the sub-micron process owing to the appearance of short-channel effects. The combination of linearization techniques has been used recently [7]–[9], but the potential of getting higher power consumption makes the combined linearity mechanism less practical. Therefore, maintaining high linearity while also achieving high speed becomes very challenging under the conditions of low power supply voltage and limited power consumption.

This brief presents a highly linear OTA in 1-V power supply voltage and is organized as follows. The design issues and circuit details are discussed in Section II. Compensation of the nonlinearity is also analyzed in this section. The experimental results are presented in Section III. Finally, Section IV concludes the brief.

Manuscript received December 19, 2006; revised April 14, 2007. This work was supported by National Science Council of Taiwan. This paper was recommended by Associate Editor P. P. Sotiriadis.

The authors are with the Department of Communication Engineering, National Chiao Tung University, Hsinchu, 30050 Taiwan, R.O.C. (e-mail: cchung@mail.nctu.edu.tw).

Digital Object Identifier 10.1109/TCSII.2007.907559

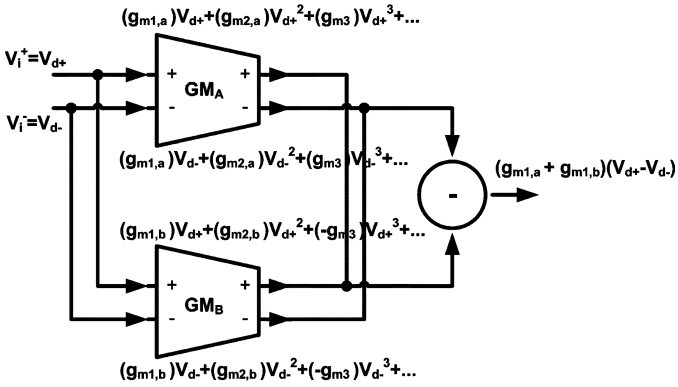

Fig. 1. Nolinearity cancellation mechanism.

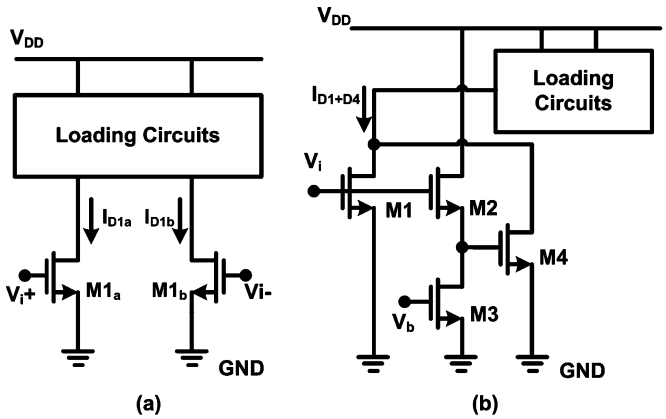

Fig. 2. (a) Basic pseudodifferential CMOS pair. (b)Mobility compensation in the pseudodifferential structure.

II. Proposed Transconductor Cell

Fig. 1 shows the block diagram of the proposed approach. It is known that under the differential architecture, the third-order distortion of the OTA will be the dominant term of its nonlinearity performance. Two voltage-to-current converters with the same first-order sign and opposite third-order sign are provided in the OTA. Therefore, the nonlinearity term of the OTA can be reduced with the addition of the two transconductance.

A. Mobility Compensation

The circuit implementation of the block diagram is based on the fact that transistors working in the saturation and subthreshold regions have opposite signs of the third-order harmonic distortion. Fig. 2(a) shows the basic pseudodifferential CMOS pair. When transistors M1a and M1b operate in the saturation region, the effective carrier mobility would be the func-

tion of longitudinal and transversal electric fields due to short-channel effects. The drain current can be approximated as

$$I_{D,\mathrm{sat}} = \frac{\mu_n C_{\mathrm{ox}} \left(\frac{W_S}{L_S}\right) (V_{\mathrm{GS}} - V_{\mathrm{thn}})^2}{2\left[1 + \theta\left(V_{\mathrm{GS}} - V_{\mathrm{thn}}\right)\right]} (1 + \lambda V_{\mathrm{DS}}) \quad (1)$$

where W_s and L_s are the width and length of the device, respectively, C_{ox} is the oxide capacitance per unit channel area, μ_n is the low-field mobility, θ is the mobility reduction coefficient, V_{thn} is the nMOS threshold voltage (a typical value of 0.43 V in the adopted process), and λ is the output impedance constant. By taking nonlinear effects into accounts of the saturated device, the differential output current can be expanded by Taylor series and obtained as follows:

$$I_O = I_{D1} - I_{D2} = a_1 V_{\mathrm{in}} + a_3 V_{\mathrm{in}}^3 + a_5 V_{\mathrm{in}}^5 + a_7 V_{\mathrm{in}}^7 + \cdots \quad (2)$$

where V_{in} equals to $(V_i + -V_i-)$ and the even-order harmonic distortion terms are cancelled out due to the topology of the differential structure. The third-order harmonic distortion term of the saturated transistors can be calculated as

$$a_{3,\mathrm{sat}} = -\frac{\mu_n C_{\mathrm{ox}} \left(\frac{W_s}{L_s}\right) \theta}{32\left[1 + \theta\left(V_{\mathrm{cm}} - V_{\mathrm{thn}}\right)\right]^4} \quad (3)$$

where V_{cm} is the input common-mode voltage. The above equation is inversely proportional to the input common-mode voltage, so the third-order harmonic distortion term increases rapidly for low power supply voltage. On the other hand, the drain current of the subthreshold transistors can be expressed as

$$I_{D,\mathrm{sub}} = I_0 \left(\frac{W_w}{L_w}\right) e^{(V_{\mathrm{GS}}/\xi V_T)} \left(1 - e^{(-V_{\mathrm{DS}}/V_T)}\right) \quad (4)$$

where W_w and L_w are the width and length of the device, respectively, I_0 is the process-dependent parameter, ξ is the subthreshold slope factor, and V_T is the thermal voltage. When transistors M1a and M1b work in the subthreshold region, the coefficient of the third-order harmonic distortion term of the differential output current would be given by

$$a_{3,\mathrm{sub}} = \frac{I_0}{24\left(\xi V_T\right)^3} \left(\frac{W_w}{L_w}\right) e^{(V_{\mathrm{cm}}/\xi V_T)}. \quad (5)$$

The third-order harmonic distortion term would be decreased by smaller device width and smaller input common-mode voltage. As the current of the saturated transistor is combined with that of the subthreshold transistor, the nonlinearity term can be reduced by choosing proper aspect ratios such that

$$a_{3,\mathrm{sat}} + a_{3,\mathrm{sub}} = 0. \quad (6)$$

Fig. 2(b) shows the implementation of the concept. Transistors M1, M2, and M3 are working in the saturation region. The source follower composed by M2 and M3 is used to force M4 to enter the subthreshold region. Thus, the third-order nonlinear term could be reduced by given

$$a_{3,\mathrm{sat}} + \frac{1}{\alpha} a_{3,\mathrm{sub}} = 0 \quad (7)$$

where α is inversely proportional to the gain of the source follower. Therefore, the third-order harmonic distortion term would be cancelled out by adding drain current of M1 and M4 together. Since transistor M4 needs to work in the subthreshold region in order to reduce the harmonic distortion, the source follower plays an important role in the approach. For large bias current, the gate–source voltage of the source follower will become larger. In this case, the minimum input swing range and the aspect ratio of transistor M4 should be increased in order for M4 to stay in the subthreshold region and for effective nonlinearity compensation. If a smaller source follower gain is maintained, the source follower would work as a voltage attenuator and the input swing range can be increased. However, under this condition, the compensation ability of the third-order harmonic distortion provided by the subthreshold transistor M4 will become weaker due to a higher attenuation ratio. Therefore, the aspect ratios of transistors M2, M3, and bias current, set by voltage V_b, should be optimized. In order to maintain proper circuit operation, the minimum input swing range is set by the condition that transistors M1 and M4 work in their respectively specified regions, which is given by $V_{\mathrm{in,min}} = V_{gs,sf} + V_{ds,m3}$, where $V_{gs,sf}$ is the gate–source voltage of the transistor M2 and $V_{ds,m3}$ is the drain-source voltage of the transistor M3. We should note that owing to transistor M4 working in the subthreshold region, the input swing limit is caused by the correct operation of the source follower, and the V_{ds} of transistor M3 should be taken into consideration. On the other hand, when the operation region of transistor M4 is maintained, the maximum input voltage $V_{\mathrm{in,max}}$ is limited due to the low power supply voltage, which is given by $V_{\mathrm{in,max}} = V_{\mathrm{thn}} + V_{\mathrm{DD}} - V_{\mathrm{Load}}$, where V_{Load} is the voltage drop at loading transistors.

The linearity performance of the input signal will also be degraded by the non-ideal effect of the source follower. The nonlinearity term of nMOS source followers is dominated by the body effect [10]. The 0.18-μm mixed-signal CMOS process is a deep n-well process, so the body of the nMOS source follower can be connected to the source in a p-well to eliminate the body effect. However, mobility degradation and channel length modulation can also degrade the linearity performance of the source follower. The second-order distortion term of the source follower will be the dominant factor to affect the third-order harmonic distortion term in the drain current of subthreshold transistors. In addition, such a level shifter adds a high frequency pole of little influence.

B. Proposed OTA Implementation

Fig. 3 shows the proposed OTA circuit. The optimal ratios between the two voltage-to-current converters have been established to achieve minimal harmonic distortion. In the circuit, the transistor MR connected between two current mirrors would be working in the linear region as a resistor. Therefore, the continuous tuning of the transconductance can be employed by adjusting the gate voltage, V_{tune}. The MOS resistor which acts as the attenuator actually promotes the linearity performance. In addition, it not only improves the linearity performance, but also adds a tuning strategy. Besides, the current mirror would introduce another high frequency pole, which is located at lower frequency than that caused by the source follower. The non-dominant poles would only slightly influence the excess phase in this approach. Fortunately, the speed limitation caused by current

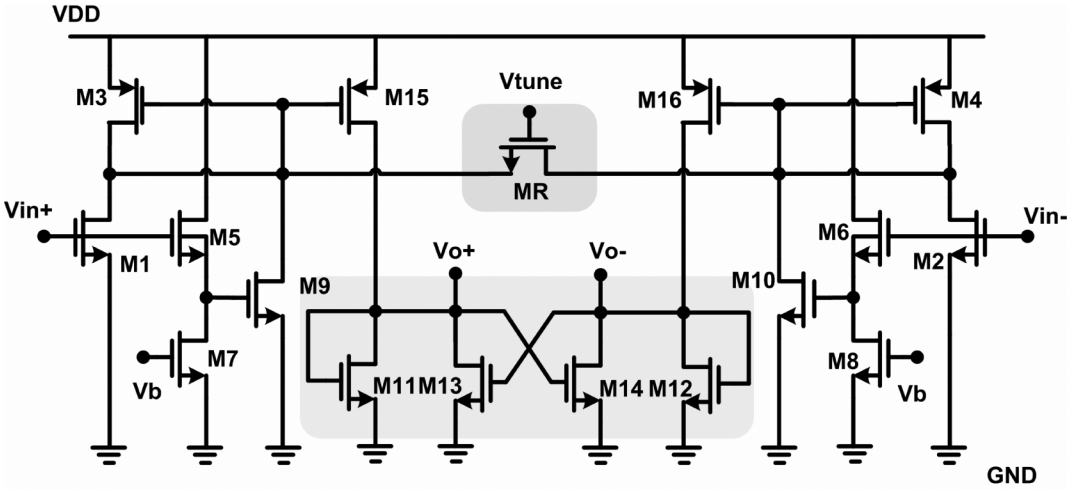

Fig. 3. Proposed OTA circuit.

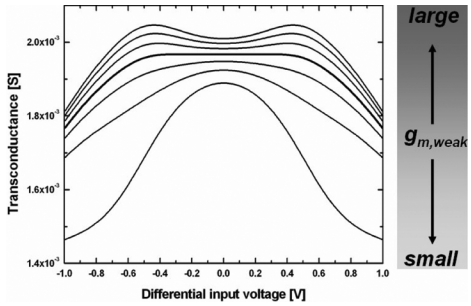

Fig. 4. Large-signal simulation of the proposed circuit.

mirror circuit would be relaxed by the addition of the small MOS resistor MR.

Fig. 4 illustrates the large-signal simulation of the proposed circuit. We can find that if no subthreshold transistors are used, the linearity performance is limited. When we increase the transconductance value of subthreshold transistors, high linearity performance can be obtained. However, if an even larger transconductance value of subthreshold transistors is used, the third-order harmonic distortion term would be dominated by the subthreshold transistors. Besides, simulation also indicates the unity-gain bandwidth of 200 MHz with a 2-pF loading and the phase margin of 89° are obtained.

In the pseudodifferential structure, in order to maintain low voltage operation, the use of stacked devices, such as the cascode structure, is prohibited. Therefore, to maintain the high output resistance in the pseudodifferential structure under the sub-micron process, increasing channel length could be one solution. However, a very long-channel transistor will increase the parasitic capacitance associated with the output node, and thereby reduce the OTA bandwidth. In Fig. 3, as the aspect ratio of transistor M11 equals to that of M12 and M13 equals to M14, the saturated transistors give the following expressions for both the differential-mode resistance and common-mode resistance

$$\begin{aligned}\text{Common-mode resistance} &= (g_{m_{11}} + g_{m_{13}})^{-1} \\ \text{Differential-mode resistance} &= \left(g_{m_{11}} - g_{m_{13}} + \frac{1}{r_{o,\text{all}}}\right)^{-1}\end{aligned} \tag{8}$$

where gm_{11} and gm_{13} are the small-signal transconductance of M11 and M13, respectively, and $r_{o,\text{all}}$ is the output resistance paralleled by the drain-source resistance of M11, M12, M13, M14, M15, and M16. By designing a little larger aspect value of M13 than M11, the negative conductance formed by gm_{11}–gm_{13} would be close to the value of $1/r_{o,\text{all}}$ so as to increase the overall differential output resistance. The differential gain can be designed to a large value which will be suitable for most of applications. Moreover, as we can obtain the common-mode resistance from (8), the common-mode stability would be guaranteed by providing larger aspect ratios of transistors M11 and M13 than those of input transistors.

C. Nonidealities in the Proposed OTA

Mismatch between the input transistors of the OTA will cause an imbalance in the drain current of the current mirrors, and thus generate even-order harmonics in voltage-to-current conversion. A significant increase of the device size will reduce offset caused by random mismatch. Besides, the small MOS resistor helps to reduce the even-order harmonics by balancing the voltage at both terminals, and thus minimize the drain current mismatch caused by current mirrors. Therefore, with the MOS resistor, the dc offset caused by the device mismatch is reduced by allowing the load resistance seen from input transistors to be different. For the output stage, mismatch between transistors would limit the differential mode gain. Careful layout was taken where the device match is required.

The output noise current of the OTA is the combination of saturated and subthreshold input transistors, current mirrors, and the MOS resistor. In high speed circuit design, the most significant noise source of a single transistor is the thermal noise generated in the channel. The channel noise can be modeled by a current source connected between the drain and source with a spectral density [11]

$$\overline{I_n^2} = 4kT\delta g_{ms} \tag{9}$$

where k is the Boltzmann constant, g_{ms} is the source conductance, and the device noise parameter δ depends on the bias condition [11]. For the proposed circuit of the differential structure,

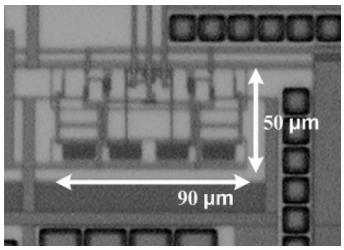

Fig. 5. Die microphotograph.

we have defined $g_{m(n)} = g_{m(n+1)}$, where n equals to the odd number (ex: $g_{m1} = g_{m2}$, $g_{m3} = g_{m4}, \ldots$). Thus, the thermal noise density evaluated at the output node is derived as

$$\begin{aligned}\overline{I_{n,\text{out}}^2} = 8kT\Bigg\{&\Bigg[\delta_1\left(g_{m5}+g_{m7}\right)\left(\frac{g_{m9}}{g_{m5}}\right)^2 \\ &+\delta_1\left(g_{m1}+g_{m3}\right)+\delta_2 g_{m9}\Bigg] \\ &\times\left(\frac{g_{m3}R_{mr}}{2+g_{m3}R_{mr}}\right)^2+\frac{\delta_3}{2R_{mr}} \\ &\times\left(\frac{2}{2+g_{m3}R_{mr}}\right)^2\Bigg\}\left(\frac{g_{m15}}{g_{m3}}\right)^2 \\ &+8kT\delta_1 g_{m15} \end{aligned} \tag{10}$$

where δ_1, δ_2, and δ_3 would be the noise parameter at saturation, subthreshold, and linear regions, respectively. Besides, R_{mr} is the resistance of linear region transistor MR. From noise analysis, the source follower adds the input-referred noise while providing a voltage gain less than unity. Also, to reduce the thermal noise, the transconductance of input transistors should be maximized, which implies that an increasing overdrive input common-mode voltage $V_{ov} = V_{gs} - V_{\text{thn}}$ would result in a higher signal-to-noise ratio (SNR).

III. Experimental Results

The chip was fabricated in 0.18-μm deep n-well CMOS process. The micrograph of the chip is shown in Fig. 5 where the active area is 4.5×10^{-3} mm^2. The device size of saturated transistors M1 and M2 is 6 μm/0.18 μm, the subthreshold transistors M9 and M10 is 1 μm/0.18 μm, the linear transistor MR is 15 μm/0.18 μm, and the bias voltage of V_b is 0.6 V. A supply voltage of 1 V was employed in the measurements and the nominal static power consumption of the OTA is 2.5 mW. The output current versus input voltage over the tuning range is shown in Fig. 6. The measured harmonic distortion for a 400 mV$_{pp}$ differential input signal at 1 MHz is -70 dB, and the third-order harmonic distortion of the output currents dominates the nonlinearity performance. The second-order harmonic distortion is due to the mismatch in the off-chip single-ended to differential input and differential output to single-ended conversion setup. The limitation of the input swing range is due to the departure of correct working regions under low power supply voltage as predicted theoretically. The third-order intermodulation (IM3) distortion measured with two sinusoidal tones of 400 mV$_{pp}$ amplitude

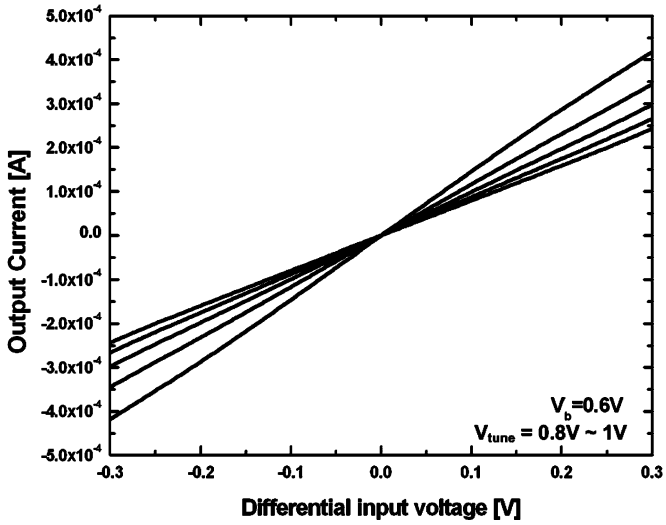

Fig. 6. Output current versus input voltage over the tuning range.

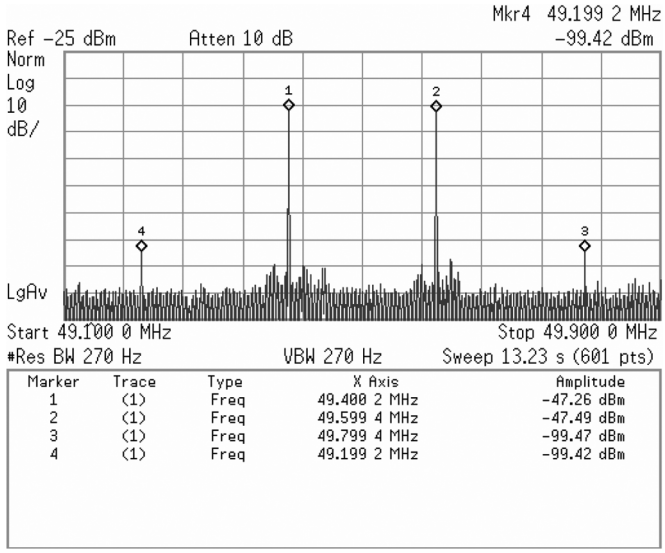

Fig. 7. Measured two tone intermodulation distortion.

is shown in Fig. 7. The IM3 is shown to be less than -52 dB at the speed of 50 MHz and drops to -50 dB at 56 MHz. The measured input referred noise spectral density at 50 MHz is 13 nV/$\sqrt{\text{Hz}}$. Table I summarizes the performance of this work with recently reported OTAs.

IV. Conclusion

A novel pseudodifferential OTA based on a mobility compensation technique has been fabricated and measured. It is based on the principle that the third-order harmonic distortion term could be cancelled by the addition of the two drain current, one in the saturation region and the other in the subthreshold region, applying small extra power consumption by adding the linearity enhancement stage. The technique employed leads to a significant increase of linearity performance in the voltage-to-current conversion. The measurement results show less than -52 dB IM3 at 50-MHz input signal under 1-V power supply voltage. We can conclude that the low-voltage OTA could be provided as

TABLE I
COMPARISON OF PREVIOUSLY REPORTED WORKS

Reference	[7]	[9]	[12]	[13]	[14]	This work
Technology	0.35-μm CMOS (Measurement)	0.5-μm CMOS (Measurement)	0.6-μm CMOS (Measurement)	0.18-μm CMOS (Simulation)	0.35-μm CMOS (Simulation)	0.18-μm CMOS (Measurement)
HD3/IM3	-65dB IM3 at 20MHz	-43dB HD3 at 30MHz	-40dB HD3 at 5MHz	-65dB HD3 at 1MHz	-41.8dB HD3 at 1MHz	-55dB HD3 and -52dB IM3 at 50MHz
Input swing range	1.3Vpp	0.9Vpp	2.5Vpp	0.6Vpp	1 Vpp	0.4Vpp
Transconductance value	100 μS	1065 μS	105 μS	20 μS	30 μS	1000 μS
Supply	3.3V	3.3V	5V	1.8V	2.5V	1V
Power consumption	10.5mW	10.7mW	5.7mW	145 μW	150.8 μW	2.5mW
Normalized power efficiency (g_m/power)	0.024	0.25	0.04	0.34	0.5	1
Input referred noise	75 nV/$\sqrt{}$Hz	9.8 nV/$\sqrt{}$Hz	38 nV/$\sqrt{}$Hz	-	-	13 nV/$\sqrt{}$Hz

a high linearity and high speed building block in analog VLSI applications.

ACKNOWLEDGMENT

The authors would like to thank the National Chip Implementation Center of Taiwan for supporting the chip fabrication.

REFERENCES

[1] M. Ismail and T. Fiez, *Analog VLSI Signal and Information Processing*. New York: McGraw-Hill, 1994.

[2] C. C. Hung, M. Ismail, K. Halonen, and V. Porra, "A low-voltage rail-to-rail CMOS $V-I$ converter," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 46, pp. 816–820, Jun. 1999.

[3] T. Y. Lo and C. C. Hung, "A wide tuning range G_m-C continuous time analog filter," *IEEE Trans. Circuits Syst. I, Reg. Papers*, to be published.

[4] S. R. Zarabadi, M. Ismail, and C. C. Hung, "High performance analog VLSI computational circuits," *IEEE J. Solid-State Circuits*, vol. 33, no. 4, pp. 644–649, Apr. 1998.

[5] E. Sánchez-Sinencio and J. Silva-Martínez, "CMOS transconductance amplifiers, architectures and active filters: A tutorial," in *Proc. IEE Circuits Devices Syst.*, Feb. 2000, vol. 147, pp. 3–12.

[6] A. Lewinski and J. Silva-Martinez, "OTA linearity enhancement technique for high frequency applications with IM3 below -65 dB," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 51, no. 10, pp. 542–548, Oct. 2004.

[7] Y. S. Youn, J. H. Chang, K. J. Koh, Y. J. Lee, and H. K. Yu, "A 2 GHz 16-dBm IIP3 low noise amplifier in 0.25 μm CMOS technology," in *Dig. Tech. Papers IEEE Int. Solid-State Circuits Conf.*, Feb. 2003, pp. 452–453.

[8] C. Fager, J. C. Pedro, N. B. Carvalho, H. Zirath, F. Fortes, and M. J. Rosário, "A comprehensive analysis of IMD behavior in RF CMOS power amplifiers," *IEEE J. Solid-State Circuits*, vol. 39, pp. 24–34, Jan. 2004.

[9] S. H. Tang, K. H. Kim, Y. H. Kim, Y. You, and K. R. Cho, "A novel CMOS operational transconductance amplifier based on a mobility compensation technique," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 52, no. 1, pp. 37–42, Jun. 2005.

[10] X. Fan and P. K. Chan, "Analysis and design of low-distortion CMOS source followers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, pp. 1489–1501, Aug. 2005.

[11] U. Yodprasit and C. C. Enz, "A 1.5-V 75-dB dyamic range third-order G_m-C filter integrated in a 0.18-μm standard digital CMOS process," *IEEE J. Solid-State Circuits*, vol. 38, pp. 1189–1197, Jul. 2003.

[12] F. Behbahani, T. Weeguan, A. Karimi-Sanjaani, A. Roithmeier, and A. A. Abidi, "A broadband tunable CMOS channel-select filter for a low-IF wireless receiver," *IEEE J. Solid-State Circuits*, vol. 35, no. 4, pp. 476–489, Apr. 2000.

[13] I. S. Han, "A novel tunable transconductance amplifier based on voltage-controlled resistance by MOS transistors," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 8, pp. 662–666, Aug. 2006.

[14] F. A. P. Baruqui and A. Petraglia, "Linearly tunable CMOS OTA with constant dynamic range using source-degenerated current mirrors," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 9, pp. 797–801, Sep. 2006.