Voltage-Polarity-Independent and High-Speed Resistive Switching Properties of V-Doped $SrZrO_3$ Thin Films

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***Abstract*—In this paper, nonpolar resistive switching behavior is reported for the first time in a SZO-based memory device. The electrode materials used which have different conductivities affect the resistive switching properties of the device. The Al/V:SZO-LNO/Pt device shows nonpolar switching behavior, whereas the Al/V:SZO/LNO device has bipolar switching property. The resistance ratios of these two devices are quite distinct owing to the difference between the resistance of low resistance states. The Al/V:SZO-LNO/Pt device with lower resistive switching voltages (±7 V turn on and ±2 V turn off) and higher resistance ratio (10^7) is more suitable for practical applications compared to the Al/V:SZO/LNO device. The switching speed of the Al/V:SZO-LNO/Pt device is 10 ns, which is the fastest speed that has ever been reported. The conduction mechanisms, nondestructive readout property, retention time, and endurance of this device are also reported in this paper.**

***Index Terms*—Conduction mechanism, nonvolatile memory (NVM), resistive random access memory (RRAM), resistive switching, $SrZrO_3$, switching polarity.**

I. Introduction

NONVOLATILE memory (NVM) has played an important role in the semiconductor industry as a result of the prevalent usage of portable equipment. The advantage of NVM is that the stored data can be kept for a long time without power supply. Requirements for a perfect NVM include the properties of nondestructive readout, low operation voltage, low power consumption, high operation speed, long retention time, high endurance, simple structure, and small size [1]. However, flash memory, the mainstream of NVM nowadays, has some drawbacks such as high operation voltage, low operation speed, and poor retention time owing to a high leakage current with device scaling [2]. Therefore, various new types of NVMs have been enthusiastically studied for possibly replacing flash memory. Among various new types of NVMs, resistive random access memory (RRAM) is one of the promising candidates due to its superior properties including simple structure, small size, long retention time, high operation speed, and multistate switching [3]–[5]. Based on the materials of resistive layers, researches of RRAM can be classified into four groups: 1) $PrCaMnO_3$ (PCMO) and $LaSrMnO_3$ [1], [6]–[8]; 2) doped $SrZrO_3$ (SZO) and $SrTiO_3$ [9]–[14]; 3) transition metal oxides [2]–[4], [15]–[18]; and 4) polymer materials [19], [20]. However, the switching voltage, nonpolar or bipolar switching, and polarity of bipolar switching of these devices are quite different from each other. For instance, Fujimoto *et al.* [15] reported that the Pt/TiO_2/TiN device was bipolar switching, while Choi *et al.* [16] reported that the Pt/TiO_2/Ru device was nonpolar switching. Further, the resistive switching of SZO-based memory devices in the earlier studies is reported to be bipolar switching, and hence, bipolar switching was considered as an intrinsic property of SZO-based memory devices [9]–[13]. Nevertheless, in this paper, the nonpolar switching of SZO-based memory devices is proposed for the first time, achieved by using Pt and Al for bottom electrode (BE) and top electrode (TE), respectively. The switching voltage, nonpolar or bipolar switching, and polarity of bipolar switching are found to be determined by the electrode materials with different conductivities used in the devices. The resistive switching time of the device reported in this paper is 10 ns, which is the fastest speed compared with the earlier mentioned reports. In addition, the conduction mechanisms, nondestructive readout property, retention time, and endurance of the Al/V:SZO-LNO/Pt device are also demonstrated. Consequently, this paper may lead to a better understanding of RRAM devices for NVM applications.

II. Experiment

First, a 200-nm-thick SiO_2 isolation layer was thermally grown on RCA-cleaned (100) silicon wafer in an oxidation furnace. Second, a 10-nm-thick Ti adhesion layer and a 100-nm-thick Pt conducting layer were sequentially deposited on the SiO_2/Si substrate using an electron beam evaporator to form the BE. Then, a 150-nm-thick $LaNiO_3$ (LNO) buffer layer was deposited on the Pt BE at 250 °C by a radio frequency (RF) magnetron sputtering. The LNO film was heat treated using a rapid thermal annealing furnace in O_2 ambient at 600 °C for 1 min. After that, a 45-nm-thick 0.3 mol% V-doped SZO (V:SZO) resistive film was deposited on the LNO buffer layer at 500 °C by RF magnetron sputtering. Finally, a 300-nm-thick Al TE was deposited on the V:SZO film using a thermal

Manuscript received April 5, 2007; revised August 3, 2007. This work was supported in part by the Winbond Electronics Corporation and by the National Science Council of Taiwan under Project NSC 95-2221-E009-278. The review of this paper was arranged by Editor M. J. Kumar.

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Digital Object Identifier 10.1109/TED.2007.908867

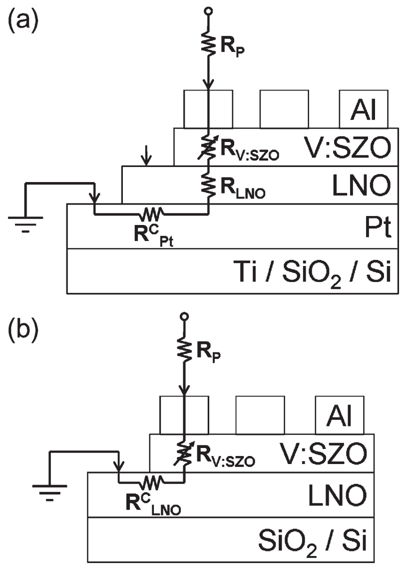

Fig. 1. Device structures and equivalent circuits of (a) Al/V:SZO-LNO/Pt device, and (b) Al/V:SZO/LNO device.

evaporator to form an Al/V:SZO-LNO/Pt (metal/resistor/metal, MRM) sandwich structure. The area of the TE defined by a shadow mask was 4.9×10^{-4} cm^2. The MRM structure of the device is shown in Fig. 1(a).

In a separate study, an LNO film was directly deposited on the SiO_2/Si substrate to form a BE. Besides, all the fabricating processes of this device were the same with the aforementioned device except the Pt/Ti deposition, and then, the Al/V:SZO/LNO MRM sandwich structure was also formed [Fig. 1(b)]. This device configuration is similar to that proposed earlier [13].

The crystal structure of LNO films deposited on Pt BE and SiO_2 layer was determined by X-ray diffraction (XRD) analysis. The electrical properties of these two devices were recorded by an Agilent 4155C semiconductor parameter analyzer and Agilent 81110A pulse pattern generator. During the electrical measurements, electrical signals including a sweep voltage and a voltage pulse were applied on TE, while the BE was grounded.

III. Results and Discussion

Fig. 2 shows the XRD patterns of LNO films deposited on Pt BE and SiO_2 layer. Two LNO films exhibit (100)-preferred orientation. It has been reported that SZO film deposited on (100)-orientated LNO film had (100)-preferred orientation and good resistive switching characteristics [12].

Fig. 3(a) depicts the current–voltage (I–V) curve of the Al/V:SZO-LNO/Pt device. When a sweep voltage is applied from 0 to +7 or −7 V, the current of the device increases rapidly, and the device is switched from high resistance state (HRS) to low resistance state (LRS), which is defined as the “turn on” process. On the other hand, when a sweep voltage is applied from 0 to +2 or −2 V, the current decreases suddenly and the device is switched from LRS to HRS, defined as the “turn off” process. A current compliance is set at 1 mA during the turn on process to prevent degradation of the device, but

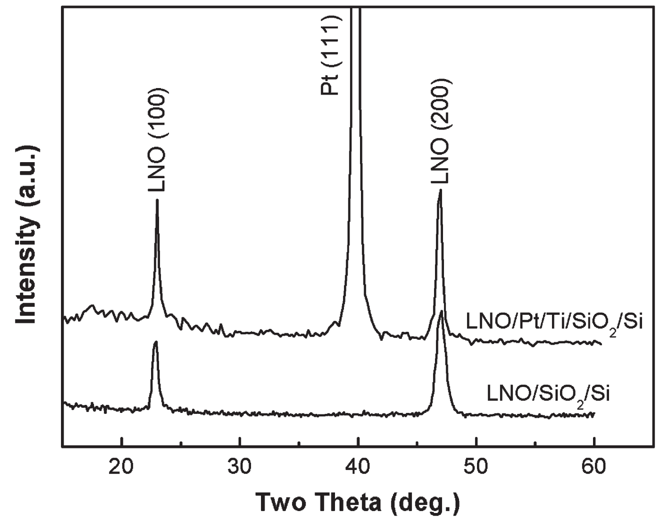

Fig. 2. XRD patterns of LNO films deposited on Pt BE and SiO_2 layer.

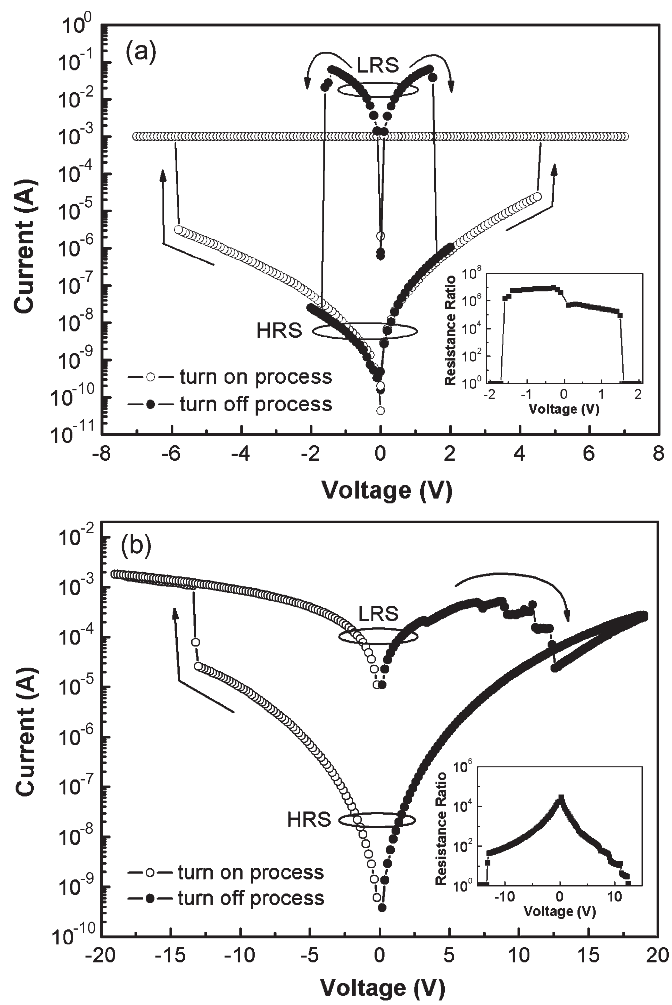

Fig. 3. I–V curves of (a) Al/V:SZO-LNO/Pt device, and (b) Al/V:SZO/LNO device. The inset is the resistance ratio between two states of each device.

no current compliance is used for the turn off process. The voltage window between turn on and turn off processes is clear enough for accurate switching of the device. The polarity independence on turn on and turn off voltages as shown here is called "nonpolar" switching. Nonpolar switching behavior is proposed in the SZO-based memory device for the first time. The LRS resistance of the device is about 15 Ω, and an equivalent circuit of this device is shown in Fig. 1(a), where the parasitic capacitance is assumed to be ignored. Equation (1) is the series resistance of this device

$$R_{\mathrm{V:SZO}} + R_{\mathrm{LNO}} + R^{\mathrm{C}}_{\mathrm{Pt}} + \mathrm{R}_P = 15\ \Omega \qquad (1)$$

where $R_{\mathrm{V:SZO}}$, R_{LNO}, $R^{\mathrm{C}}_{\mathrm{Pt}}$, and R_P are the sum of the thin film resistance of V:SZO film and contact resistance of Al/V:SZO and V:SZO/LNO interfaces, the sum of the LNO thin film resistance and LNO/Pt contact resistance, the crabwise resistance of Pt BE, and other parasitic resistance, respectively. Resistance value of each item shown in (1) is lower than 15 Ω, and the resistivity of platinum is $1.06 \times 10^{-5}\ \Omega \cdot \mathrm{cm}$ [21].

The resistance ratio between two states in this device is higher than 10^7, which is shown in the inset of Fig. 3(a). In addition, a little asymmetric of the I–V curve of the device may be due to the different materials used for BE and TE, which have different work functions and contact resistance with LNO and V:SZO films, respectively.

Fig. 3(b) shows the I–V curve of the Al/V:SZO/LNO device. When a sweep voltage is applied from 0 to −19 V, the device is turned on at about −13 V; when a sweep voltage is applied from 0 to +19 V, the device is turned off after passing through a transition region [13]. The polarity dependence on applying voltages as shown here is called "bipolar" switching. The LRS resistance of the device is about 15 kΩ, and an equivalent circuit of the device is shown in Fig. 1(b) (parasitic capacitance assumed to be ignored). Equation (2) is the series resistance of this device

$$R_{\mathrm{V:SZO}} + R^{\mathrm{C}}_{\mathrm{LNO}} + R_P = 15\ \mathrm{k}\Omega \qquad (2)$$

where $R_{\mathrm{V:SZO}}$, $R^{\mathrm{C}}_{\mathrm{LNO}}$, and R_P are the sum of the thin film resistance of V:SZO film and contact resistance of Al/V:SZO and V:SZO/LNO interfaces, the crabwise resistance of LNO BE, and other parasitic resistance, respectively. The resistance ratio between the two states in this device is higher than 10^4, shown in the inset of Fig. 3(b). However, the resistance ratio of this device is three orders of magnitude lower than that of the Al/V:SZO-LNO/Pt device owing to the difference between the LRS resistance of two devices. From (1) and (2), it can be easily understood that the crabwise resistance of LNO BE of the Al/V:SZO/LNO device mainly contributes to the LRS resistance, which is similar to a compliance effect although the resistance of V:SZO films and parasitic resistance of two devices may have some differences under the distinct turn on processes. Consequently, the device structure of Al/V:SZO-LNO/Pt with lower resistive switching voltage and higher resistance ratio is more suitable for practical NVM applications. However, if the SZO film is directly deposited on Pt or other metals, such as Al, Ti, Ta, Zr, Ni, and Nb, no (100)-preferred orientation film can be obtained, and no good resistive switching behavior can be observed [12]. Therefore, the LNO buffer layer is needed for a SZO-based device with good switching properties. Besides, to prove that the resistive switching does not occur in the LNO film, the resistive switching property was determined between

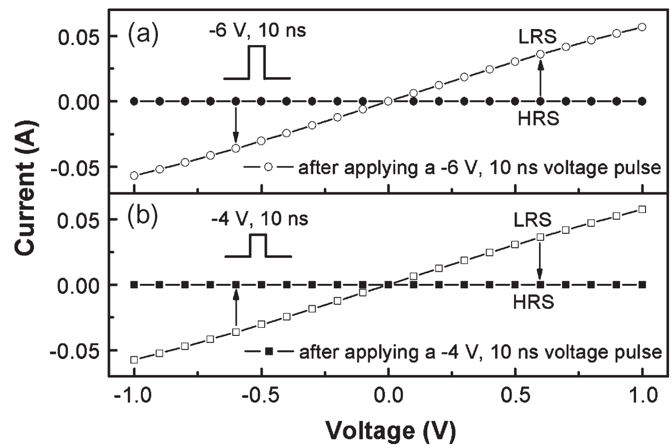

Fig. 4. Resistive switching speed of the Al/V:SZO-LNO/Pt device.

Pt BE and LNO film [Fig. 1(a)], and no resistive switching behavior was observed. Hence, the resistive switching occurring in the LNO film can be eliminated. In addition, it was indicated in Fig. 2 that the LNO film quality on Pt is better than that on SiO_2, which may be one of the minor reasons for the aforementioned distinct resistive switching behavior. The voltage polarity of resistive switching will be further discussed in the last paragraph of this section.

Fig. 4 indicates the resistive switching speed of the Al/V:SZO-LNO/Pt device. Fig. 4(a) shows the I–V curves of the device before and after applying a −6 V, 10 ns voltage pulse, and the device is switched from HRS to LRS. On the other hand, this device is switched back to HRS after applying a −4 V, 10 ns voltage pulse shown in Fig. 4(b). The switching speed of turn on and turn off processes is 10 ns. Liu *et al.* [11] have reported that the device with Al/Cr-doped SZO (Cr:SZO)/LNO structure can be turned on and turned off by applying −20 V, 5 ns and +20 V, 500 μs voltage pulses, respectively. Obviously, the switching speeds between turn on and turn off processes have a difference of five orders of magnitude. The asymmetry of switching speed can be explained by the LNO compliance effect. In the turn off process, electrons are injected from BE to resistive layer, so the conductivity of BE will determine the switching speed of the device. Therefore, the SZO-based memory device using Pt BE can significantly improve the switching speed. In this paper, the Al/V:SZO-LNO/Pt device with high-speed resistive switching of 10 ns is proposed. It is the fastest speed in comparison with those reported in the earlier studies [9], [11], [12].

Fig. 5(a) depicts the plots of $\mathrm{Ln}(|I|)$ versus $\mathrm{Ln}(|V|)$ of both LRS and HRS currents for the Al/V:SZO-LNO/Pt device. The slopes of LRS curves are close to unity, indicating that the LRS currents are dominated by Ohmic conduction, which is related to thermally excited electrons hopping from one isolated state to the next [22]. On the other hand, the HRS curves are not straight lines, implying that the HRS currents are dominated by other conduction mechanisms. Fig. 5(b) shows the plots of $\mathrm{Ln}(|I/V|)$ as a function of $|V|^{1/2}$ of both HRS and LRS currents for this device. The linear fittings of the device indicate that the HRS currents follow the Frenkel–Poole (F–P) emission, which is corresponding to field-enhanced thermal excitation of trapped electrons into the conduction band [22]. These

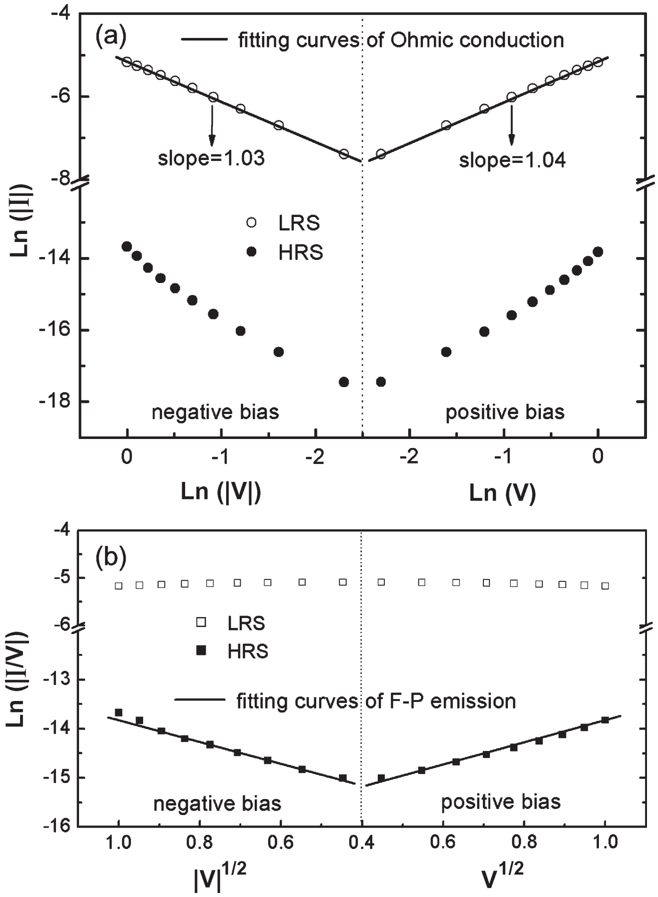

Fig. 5. Fitting curves of LRS and HRS currents of the Al/V:SZO-LNO/Pt device by (a) Ohmic conduction, and (b) F–P emission.

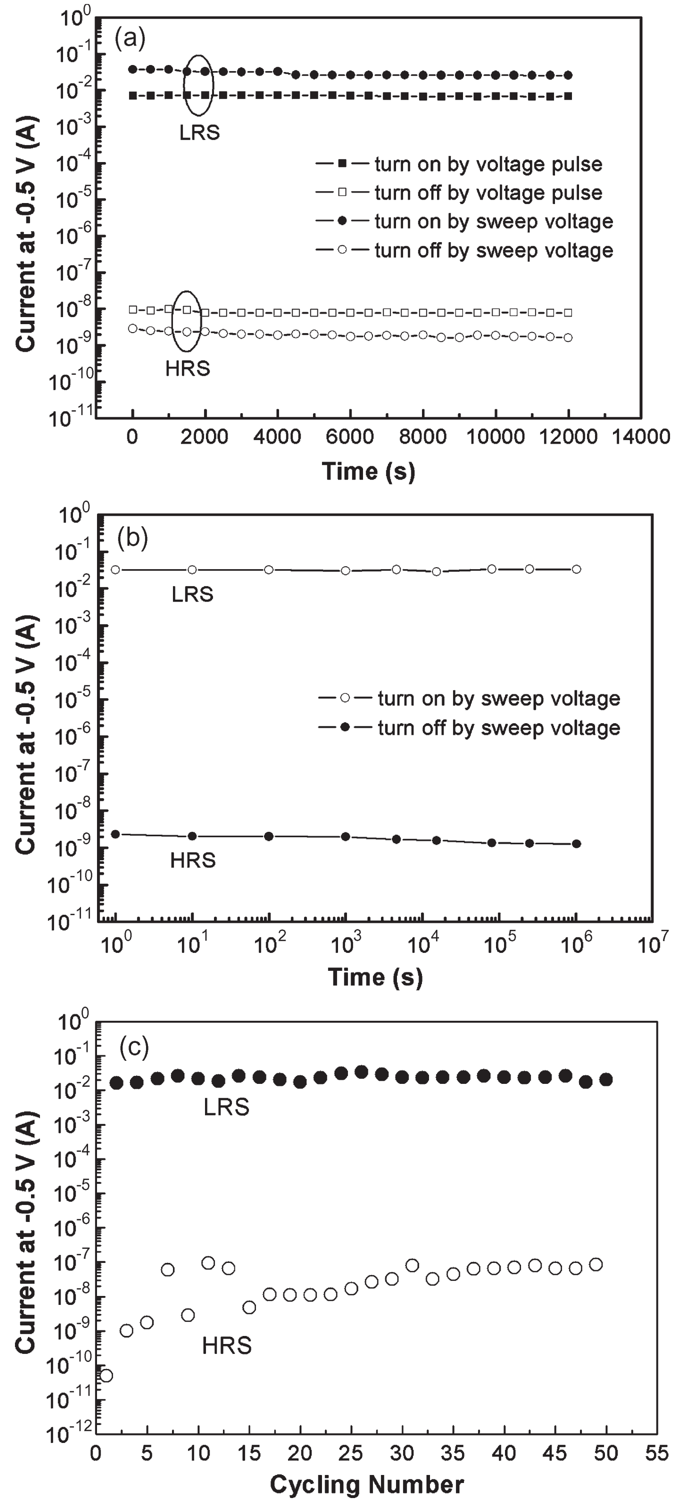

Fig. 6. (a) Nondestructive readout property, (b) Retention time, and (c) Endurance of the Al/V:SZO-LNO/Pt device measured at room temperature.

results conform to that proposed earlier [13], which implies that the resistive switching mechanisms can be considered as formation and disruption of local conducting paths. Besides, both Ohmic behavior and F–P emission are bulk conduction so that the resistive switching occurring at the interface can be eliminated.

Fig. 6(a) indicates the nondestructive readout property of the Al/V:SZO-LNO/Pt device. The currents of LRSs and HRSs switched by both sweep voltages and voltage pulses remain almost constant after applying -0.5 V, ongoing bias voltages for more than 10^4 s, which indicates that two resistance states will not be varied after performing 10^{12} of read pulses (assuming that a read pulse is -0.5 V, 10 ns). Because a sweep voltage can be looked on as a voltage pulse with infinite duration [8], the LRS/HRS current switched by a sweep voltage is higher/lower than that by a voltage pulse, and hence, the resistance ratio between two states switched by sweep voltages is higher than that by voltage pulses. Fig. 6(b) shows the retention time of the Al/V:SZO-LNO/Pt device measured at -0.5 V, indicating that the retention time is longer than 10^6 s and the resistance ratio between two states remains higher than 10^7. Fig. 6(c) indicates the endurance of the Al/V:SZO-LNO/Pt device measured at -0.5 V, showing that the device can be switched between HRS and LRS for more than 50 times. In summary, the Al/V: SZO-LNO/Pt device with superior resistive switching properties, such as low operating voltage, high operating speed, and long retention time, is a possible candidate for next-generation NVM applications.

Table I shows the resistive switching properties of SZO-, TiO_2-, and PCMO-based memory devices reported by several well-known research groups. Based on the experimental results shown in Fig. 3(a), the SZO-based memory device is nonpolar switching, which is different from bipolar switching results

TABLE I
DEVICE STRUCTURES, DEPOSITION METHOD OF RESISTIVE LAYER, RESISTIVE SWITCHING POLARITIES, AND SWITCHING VOLTAGES OF SZO-, TiO_2-, AND PCMO-BASED MEMORY DEVICES PROPOSED BY SEVERAL WELL-KNOWN RESEARCH GROUPS

Material	Device structure *	Deposition method	Switching polarity	Turn on	Turn off	Reference
V:SZO	Al/V:SZO-LNO/Pt	Sputtering	Nonpolar	Sweep ±7 V Pulse ±6 V, 10 ns	Sweep ±2 V Pulse ±4 V, 10 ns	This work
Cr:SZO	Au/Cr:SZO/SRO	Pulsed laser deposition	Bipolar	Sweep -0.5 V	Sweep +0.5 V	[9]
Cr:SZO	Pt/Cr:SZO/SRO	Sputtering	Bipolar	Sweep +2 V	Sweep -1.5 V	[10]
TiO_2	Pt/TiO_2/TiN	Oxidation	Bipolar	Pulse -2 V, 20 ns	Pulse +2.2 V, 30 ns	[15]
TiO_2	Pt/TiO_2/Ru	Atomic layer deposition	Nonpolar	Sweep ± 2 V	Sweep ±1 V	[16]
PCMO	Ti/PCMO/SRO	Pulsed laser deposition	Bipolar	Sweep -5 V	Sweep +2 V	[6]
PCMO	Pt/PCMO/Pt	Excimer laser	Nonpolar	Pulse ±3 V, 10 μs	Pulse ±5 V, 100 μs	[7]

* TE/Resistive layer/BE.

reported in the earlier studies [9], [10]. Besides, in those studies, the polarities of turn on and turn off voltages are entirely opposite; Beck *et al.* [9] proposed that their device with Au/Cr : SZO/$SrRuO_3$ (SRO) structure could be turned on/off by applying a negative/positive voltage; nevertheless, Park *et al.* [10] reported that Pt/Cr:SZO/SRO device could be turned on/off by applying a positive/negative voltage. The different switching properties between these two studies might be due to their different TEs used. Therefore, these results indicate that the electrode materials employed in the device determine its bipolar or nonpolar switching, and the polarity of bipolar switching. In Fig. 3(b), for instance, when the device is turned on, electrons are injected from Al TE into the V:SZO film; whereas in the turn off process, electrons flow from LNO BE into the V:SZO film slowly and trapped by defects uniformly [13]. However, the device cannot be turned on by applying a positive voltage because electrons injected from LNO BE are trapped by defects existing in the V:SZO film and cannot flow to Al TE. Therefore, the distinct resistive switching properties of two devices shown in Fig. 3(a) and (b) are due to different BEs used, that is, the distinct switching is attributed to different conductivities between Pt and LNO BEs. Similar results are also observed in TiO_2- and PCMO-based memory devices. In TiO_2-based memory devices, Fujimoto *et al.* [15] proposed bipolar switching of the $Pt/TiO_2/TiN$ device; however, Choi *et al.* [16] reported nonpolar switching of the $Pt/TiO_2/Ru$ device. In PCMO-based memory devices, Sawa *et al.* [6] reported bipolar switching of the Ti/PCMO/SRO device, while Fujimoto *et al.* [7] reported nonpolar switching of the Pt/PCMO/Pt device. Consequently, nonpolar switching is considered as an intrinsic property of SZO-, TiO_2-, and PCMO-based memory devices; however, the electrode materials employed, which have different conductivities, would dominate their bipolar or nonpolar switching behavior and the polarity of bipolar switching. Therefore, appropriate electrode materials chosen are indeed important for obtaining an RRAM device with excellent properties. However, other factors, such as work function of electrodes, contact resistance between two films, microstructure of resistive layer, and work function difference and property of each interface, still need further detailed studies for developing an excellent RRAM device.

IV. CONCLUSION

The experimental results reported in this paper indicate that the electrode materials with different conductivities significantly affect the resistive switching properties of the devices. The device with Al/V:SZO-LNO/Pt structure shows nonpolar switching property, whereas the Al/V:SZO/LNO device depicts bipolar switching behavior. The resistance ratios between two states are 10^7 and 10^4 for Al/V:SZO-LNO/Pt and Al/V:SZO/LNO devices, respectively, which is due to the resistance difference between the LRS of two devices. The device with Pt BE has lower switching voltages and higher resistance ratio, while the device with LNO BE possesses higher switching voltages and lower resistance ratio. Such a different behavior is attributed to a high resistance of LNO BE in comparison with a low resistance of Pt BE. The switching speed of the Al/V:SZO-LNO/Pt device is 10 ns, which is the fastest speed in comparison with those of the earlier mentioned reports. The conduction mechanisms of LRS and HRS currents are Ohmic and F–P behavior, respectively, which is considered as formation and disruption of local conducting paths in the resistive layer. The nondestructive readout property of the Al/V:SZO-LNO/Pt device is demonstrated, and the retention time of the device longer than 10^6 s is also performed in this paper. Therefore, the Al/V:SZO-LNO/Pt memory device, having good switching properties, is a possible candidate for next-generation NVM applications.

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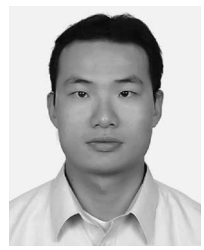

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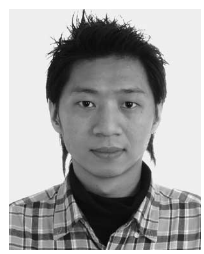

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