Performance Improvement and Scalability of Nonoverlapped Implantation nMOSFETs With Charge-Trapping Spacers as Nonvolatile Memories

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***Abstract*—This paper explores gate-to-source/drain nonoverlapped implantation (NOI) devices that function as nonvolatile memories (NVMs) by trapping charges in the silicon nitride spacers. These NOI nMOSFET devices with improved NVM characteristics were simulated and demonstrated. For a 0.8 V shift in the threshold voltage, the programming and erasing speeds of NOI devices are as fast as 40 and 60 μs, respectively. Improvements of other related NVM characteristics, including charge retention and cycling endurance, are reported. Finally, the scalability of NOI devices is simulated and discussed.**

***Index Terms*—Charge trapping, nonoverlapped implantation (NOI), nonvolatile memory (NVM).**

I. Introduction

WITH THE critical dimension of conventional floating gate memories approaching its limit in tunneling oxide [1], novel SONOS-based nonvolatile memory (NVM) devices that use silicon nitride (SiN) dielectrics as their charge trapping or storing media are being introduced [2]–[4]. Commercially available SONOS memories have been developed as two-bit-per-cell applications for high-density NVM memories [5]–[8]. Novel operating schemes such as PHINES offer improved performance [9]. Nevertheless, such SONOS devices are facing difficulties in two-bit separation, oxide–nitride–oxide downscaling, and reduction of processing complexity, as they proceed into the deep-submicrometer regime. Recently, the use of SiN spacers as the charge trapping media has provided another means of resolving these issues [10]. Fukuda *et al.* [11] reported similar SiN sidewall devices for NVM applications. However, their performance in terms of such factors as program/erase (P/E) speed does not compete with that of currently available SONOS memories. The operating speed of these SiN-spacer-trapping NVM devices seems unsatisfactory as their SiN spacer length is reduced to only 20 nm, and they suffer from poor cycling endurance and charge retention [12].

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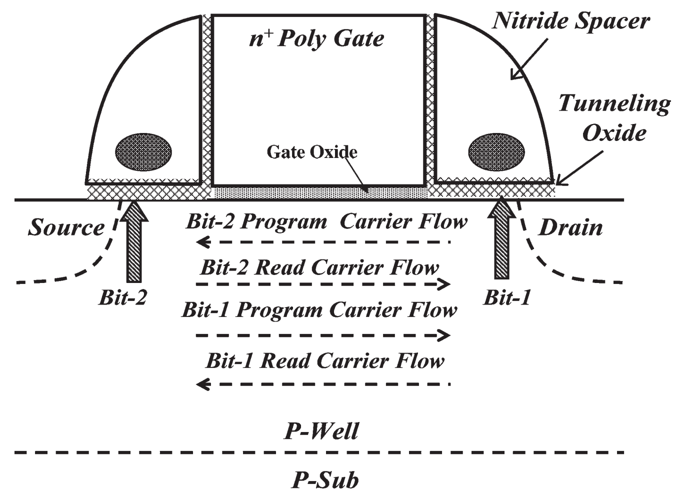

Fig. 1. Operation and structure of a two-bit-per-transistor NOI nMOSFET. These two bits can be programmed and erased by CHEI and HHEI, respectively. "Reverse Read" is used to access the stored bit in each SiN spacer.

A newly developed SiN spacer-trapping nMOSFET with gate-to-source/drain (S/D) nonoverlapped implantation (NOI) was simulated to elucidate its device structure and electrical properties. This single transistor with multibit-per-cell NVM capability is very promising, since its compact structure provides a high-density memory array. The NOI devices can be manufactured without additional masks and complex processes such as multiple polysilicon layers and ONO gate dielectrics. These advantages make NOI devices extremely attractive for embedded NVM applications in standard logic CMOS technologies. Unlike that of the other SONOS-based NVM devices, the scaling risk of two-bit charge merging can be avoided in NOI devices, because the two bits in an NOI device are stored in two SiN spacers, which are physically separated by the gate electrode and gate oxide. NOI devices can independently adjust the gate oxide and tunneling oxide thickness, making them simpler and more robust than other SONOS-type NVM devices. The processing of the new NOI nMOSFET device studied herein is first simulated. After its doping profile is obtained, the operating schemes are prescreened by simulating its potential and electrical fields under various P/E conditions. The NOI devices are then fabricated by a foundry process and later characterized to verify their electrical performance.

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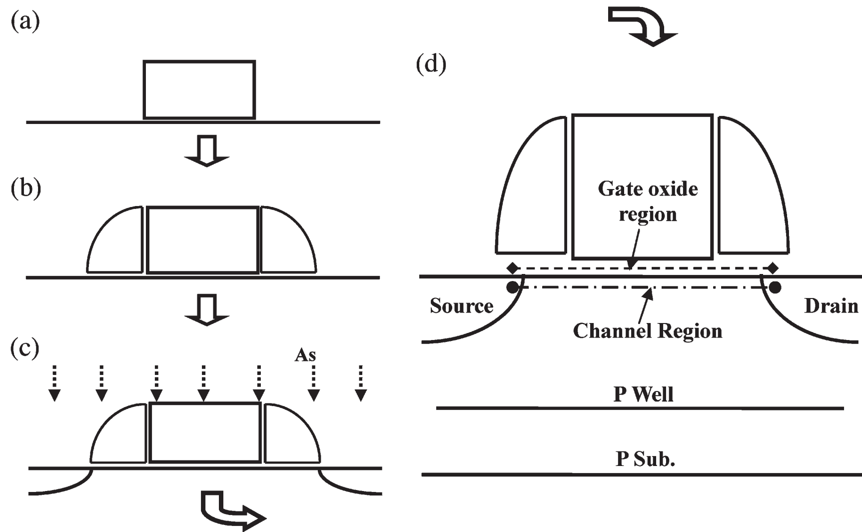

Fig. 2. Brief process flow of an NOI nMOSFET. It is fabricated by omitting the LDD implantation using a 0.25 μm CMOS process. The NOI device's channel and gate oxide regions to be simulated are also indicated in the process step (d). (a) Gate oxide and gate formation. (b) Spacer formation. (c) S/D implantation. (d) S/D annealing.

II. Device Design

A. Operating Principle

Fig. 1 schematically depicts the structure and operations of NOI NVM devices. The programming operation is based on the channel hot electron injection (CHEI) in an NOI channel region under the SiN spacer. The injection of electrons into the SiN spacer results in an increased threshold voltage $(V_{\rm th})$ as a programmed state. The erasing operation is based on hot-hole enhanced injection (HHEI) from a P-well into the SiN spacer. These injected holes cause a decreased threshold voltage as an erased state. A "reverse read" scheme is implemented by interchanging the source and drain electrodes to reverse the original programming current direction, since the channel current is more sensitive to charges trapped near the source/channel barrier [8]. As also shown in Fig. 1, the gate electrode in the NOI nMOSFET acts as a select gate between two separated SiN spacers and a control gate that manipulates carrier injection via its fringing field in each SiN spacer.

B. Device Fabrication

Fig. 2 depicts the process flow of NOI nMOSFETs. Compared to the process of typical logic devices, NOI devices are fabricated simply by omitting the lightly doped drain (LDD) implantation in the 0.25 μm CMOS technology. A 7-nm-thick gate oxide is chosen for high-voltage operations and for reasons of reliability. After the polysilicon gate is formed, a thin oxide layer is regrown to a thickness of about 6.5 nm. This oxide layer is designed for carrier tunneling and leakage blocking of stored charges during P/E operations. An SiN layer is deposited by LPCVD process and etched back to form side-wall LDD spacers after the tunneling/blocking oxide is grown. The final spacer length is measured to be 125 nm. The N-type S/D implantation is performed after the SiN spacers are formed. According to the simulated doping profile, the lateral diffusion length under the SiN spacer is about 50 nm following thermal activation. Accordingly, the gate-to-S/D nonoverlapped channel length under the spacer, which is the lateral gap between the diffusion junction of the N-type S/D and the side-wall edge of the gate electrode, is about 75 nm. Two nonoverlapped channels of an NOI device are simultaneously formed under the SiN spacers, and their spacer length significantly exceeds those reported elsewhere [10]–[12].

C. Simulation of Potential and E-Field

Commercially available TCAD tools [13], including process and device simulators, are utilized to determine the proper operating conditions before electrical characterization.

First, the device reliability has to be considered to tune its operating conditions since NVM devices are stressed in strong fields. Before the P/E operation of NOI devices can be optimized, several fundamental device limitations, including gate oxide reliability, source-to-drain punchthrough and S/D junction breakdown need to be taken into account. The gate oxide reliability limits the applied gate voltage (V_G) while the punchthrough and junction breakdown constrain the drain voltage (V_D). For typical 0.25 μm technology, the LDD nMOSFETs with 7 nm gate oxide are constantly operated at only 3.3 V to ensure long-term reliability. Their drain junction typically reaches breakdown at about 8 V and subchannel punchthrough takes place at about 7 V. The punchthrough voltage of the new NOI device is 8 V, which is higher than those of LDD devices and previously reported NOI devices whose SiN spacer length is only 80 nm [10], because they have longer SiN spacers. The total effective channel length of this new NOI device is estimated to be about 0.4 μm, which results in an increased punchthrough voltage.

The NOI's potential along the channel and the electric field in the gate oxide, as indicated in Fig. 2(d), are compared by

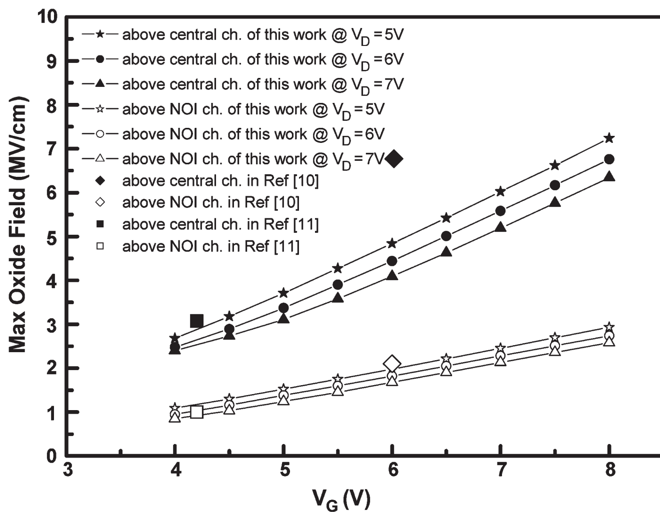

Fig. 3. Maximum programmed oxide fields above the NOI and central channels of the simulated NOI devices are compared among different V_G and V_D. The maximum oxide field increases as V_G increases and declines as V_D increases.

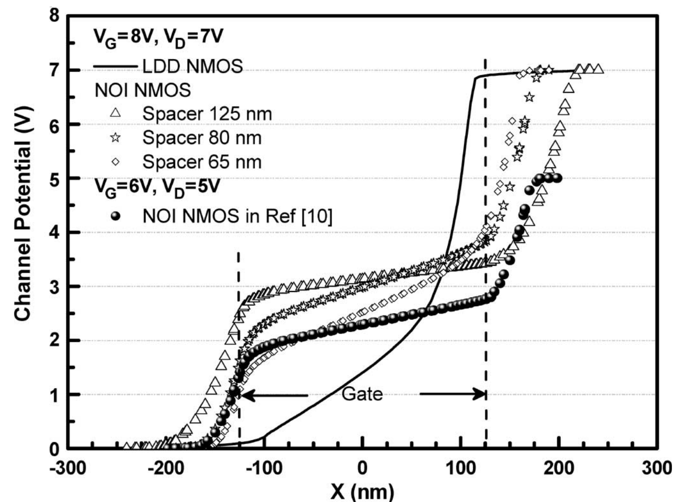

Fig. 4. Channel potential distributions of the current and previous NOI devices having different SiN spacer lengths are simulated under programming conditions. The potential distribution is divided into three segments, corresponding to two NOI channels under SiN spacers and the central channel region under the polygate.

the simulation. Various devices with different NOI channel lengths are examined by adjusting the lengths of their SiN spacers. Their identical S/D doping profiles result in a constant lateral diffusion length of 50 nm throughout this paper. Fig. 3 compares the maximum programmed oxide fields above the NOI and the central channels of the simulated NOI devices among different V_G and V_D for an SiN spacer length of 125 nm. The oxide fields of NOI devices with 65 and 80 nm SiN spacers are also simulated for benchmarking, and are highlighted in Fig. 3. These 80 nm-SiN and 65 nm-SiN NOI devices are emulated based on devices and P/E conditions in other works [10], [11], respectively. A key consideration to improve the NOI's programming speed is the increase in the oxide field above the NOI channel and the maintenance of a low oxide field above the central channel at the same time. The oxide field above the central channel of a 125 nm-SiN NOI device was weaker than that of an 80 nm-SiN NOI device under the same drain bias, and was even weaker under higher drain voltages. For $V_G > 6$ V, the 125 nm-SiN NOI device had higher oxide fields above the NOI channels than those of an 80 nm-SiN NOI device. This increased oxide field above the NOI channel is expected to enhance hot electron injection during programming. Upon consideration of the drain junction breakdown and punchthrough, the NOI maximum operating V_D value is limited to 7 V. As indicated in Fig. 3, the maximum oxide field of this paper biased at $V_D = 7$ V and $V_G = 8$ V is less than that reported elsewhere at biases of $V_D = 5$ V and $V_G = 6$ V [10]. Fig. 4 plots the simulated channel potential distributions in current and previous NOI devices. Fig. 4 also indicates that the potential distribution is divided into three distinct segments, corresponding to two NOI channels under the SiN spacer regions and the central channel region under the polygate. Since the average fringing capacitance between the gate and the NOI channel is much less than the normal gate oxide capacitance, a relatively high turn-on channel resistance and large voltage drop are expected in the NOI channels, such that the central channel potential exceeds the source potential, 0 V. Under programming, the gate oxide field is formed between the gate $(V_G = 8\text{ V})$ and central channel potentials, ranging from about 3 V at the source-side gate edge to 3.5 V at the drain-side gate edge. Consequently, the condition $V_G = 8$ V and $V_D = 7$ V for programming the new NOI device introduces an oxide potential, which is much less than that of a normal LDD nMOSFET. Fig. 5 plots the simulated oxide fields of these two NOI devices under programming. The high voltage drop is formed in the source-side NOI channel region such that the maximum programmed oxide field in the central channel region is only about 6.25 MV/cm, which is still lower than the NOI's field in the cited work [10].

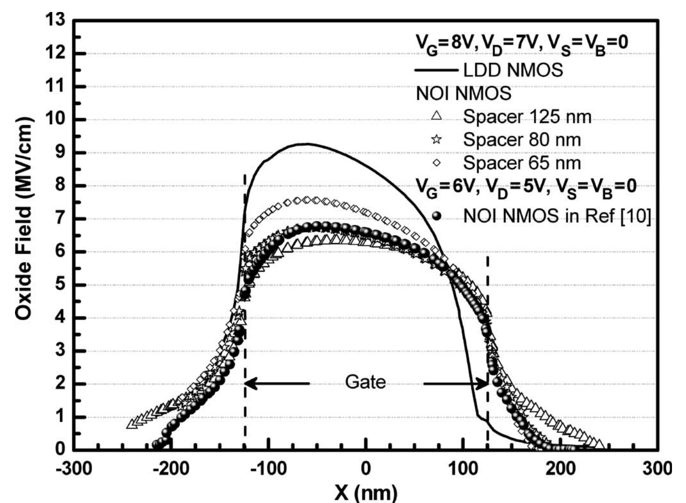

Fig. 5. Oxide field distributions of the current and previous NOI devices having different SiN spacer lengths are simulated under programming conditions. The maximum programmed oxide field in the central channel region is only about 6.25 MV/cm, which is still lower than the NOI's field in the cited work [10].

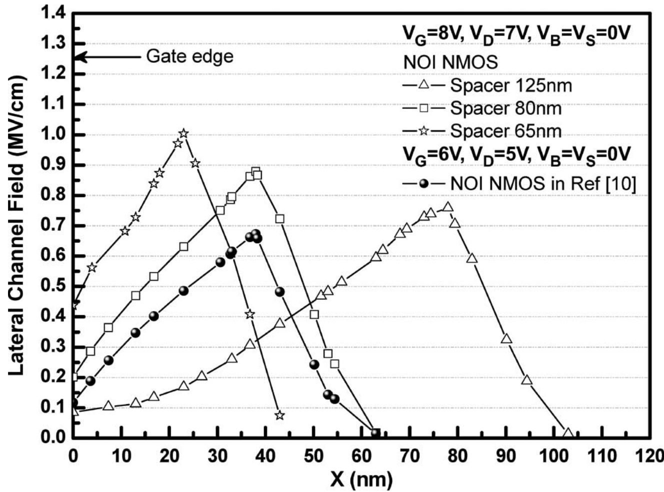

Fig. 6. Lateral channel field distribution under a SiN spacer with different SiN spacer lengths are simulated under specified programming conditions. Compared to the NOI devices with 65 and 80 nm SiN spacers, the NOI device with 125 nm SiN spacers shows the decreased maximum lateral electrical field near its drain junction.

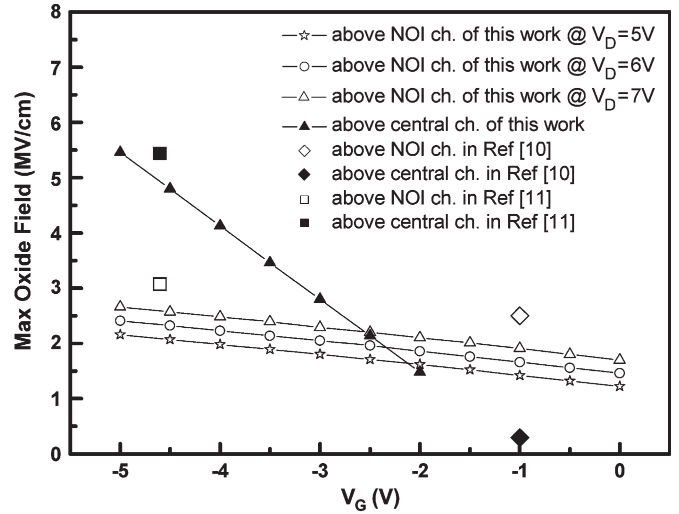

Fig. 7. Maximum gate oxide field in NOI devices under various drain and gate biasing conditions are simulated in the erasing operation. The maximum erased oxide field is mainly dependent on V_D under low V_G biasing (< 2 V) and dominated by V_G under high V_G biasing (> 2 V).

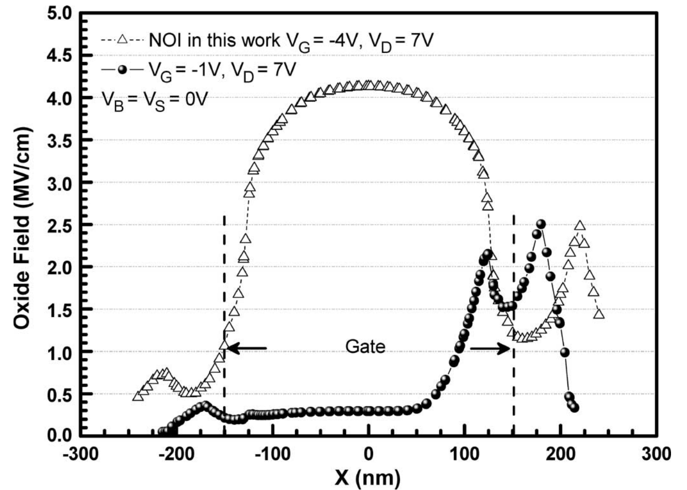

Fig. 8. Electrical field distributions in the gate oxide of the current and previous NOI devices are simulated under specified erasing conditions. A local maximum electric field of the current NOI device is induced near the drain junction and similar to that of an earlier NOI device under the same drain bias.

Fig. 6 plots the lateral channel field under an SiN spacer with SiN spacer lengths of 65 nm, 80 nm, and 125 nm under specified programming conditions. The figure reveals that the NOI device with 65 nm SiN spacers has the highest E-field, at about 0.67 MV/cm [10], near its drain junction. However, the peak field in programming the NOI device with 125 nm SiN spacers is higher, at about 0.75 MV/cm, than that of the cited work [10]. The simulations in Figs. 5 and 6 indicate that the programming field of the new NOI using $V_G = 8$ V, $V_D = 7$ V, and $V_S = 0$ V has relaxed the gate oxide stress and enhanced the channel carrier acceleration, as compared to those under operating conditions in the cited work [10]. The SiN spacer length effects of the NOI devices during programming were discussed and simulated. As shown in Figs. 4–6, the potential and electrical field in the central channel region and the lateral electrical field under the SiN spacer regions fall as the SiN spacer length increases. The electrical potential and field applied to the devices are reduced because a longer SiN spacer corresponds to a longer NOI channel region and a higher turn-on channel resistance in the NOI devices. The concern regarding the oxide-related reliability, associated with the high applied voltages, is relieved in NOI devices with an extended spacer length. Restated, NOI devices with a higher programming voltage and longer SiN spacers exhibit improved programming speed and improved oxide-related reliability.

Fig. 7 shows the maximum induced gate oxide field in simulated NOI devices with 125 nm SiN spacers under various drain and gate biasing conditions in the erasing operation, as well as under two reference conditions from other works [10], [11]. The maximum erased oxide field above the central channel is independent of V_D because the channel is not turned on. A relatively low oxide field is necessary to erase NOIs since a long erasing time is expected, as previously reported [10]. However, the low oxide field near the drain junction may result in slow hole injection. Again, the key consideration in erasing is to maintain a sufficiently strong oxide field above the NOI channel and reduce the oxide field above the central channel. Under the condition $V_D = 7$ V and $V_G = -4$ V, the resulting electric field of the gate oxide increases to about 4 MV/cm above the central channel, as indicated in Fig. 8. Under specified conditions, a local maximum electric field of as high as 2.5 MV/cm is induced near the drain junction, where the field is similar to that of an earlier NOI device [10]. This simulated oxide field ensures that no lowering of the significant erasing field below those obtained previously.

III. Results and Discussion

A. P/E Speed

Fig. 9 shows the programming characteristics of new NOI devices with a fixed $V_D = 7$ V and various V_G from 6 to 8 V. Fukuda *et al.* [11], [12] improved the programming fringing

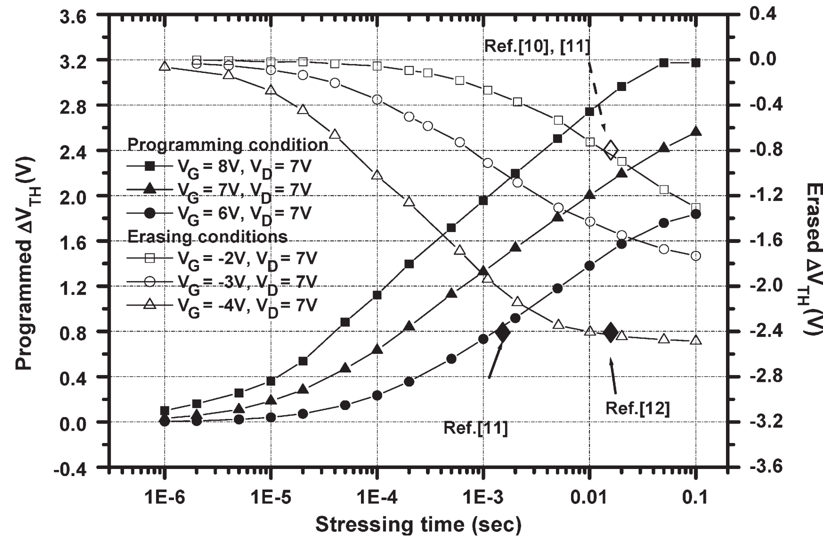

Fig. 9. Programming and erasing characteristics of the current NOI device are examined with a fixed $V_D = 7$ V. The programming time of 40 μs is needed to yield a V_{th} shift of 0.8 V at $V_G = 8$ V and $V_D = 7$ V. The erasing time of 60 μs is needed to yield a V_{th} shift of 0.8 V at $V_G = -4$ V and $V_D = 7$ V.

field by about 30% by using a thinner SiO_2 under the SiN sidewall spacer than that under polysilicon gate, increasing the write/erase efficiency. However, Fukuda's proposal may also degrade charge retention since the tunneling oxide is too thin to retain the trapped charges in the SiN spacers. The fastest programming was found at $V_G = 8$ V, with the highest fringing field. The programming speeds of two similar devices in other works [10], [11] are highlighted in Fig. 9 for direct comparison.

Lusky *et al.* [7] proposed that the charge injection and trapping region in NROM was about 40 nm wide. Fukuda *et al.* [11], [12] also reported a sidewall trapping nMOSFET with a 20 nm-wide SiN spacer but achieved a programming time of only 100 ms in programming speed. However, based on current NOI doping simulation, the NOI's gate-to-drain nonoverlapped region under the spacer is significantly increased from the previous works' 25 to 75 nm, where the NOI device can still be programmed to yield the same V_{th} shift as previous works in 40 μs. The fringing capacitance and local V_{th} measurement of the NOI device herein suggest that these injected and trapped charges are very sensitive to local V_{th} through the relatively low fringing capacitance, resulting in fast programming. The programming speed of NOI devices was improved by raising its operating voltages and extending the SiN spacer length. However, this improvement is attributable not only to an increase in operating voltage. For a given technology node, the new NOI devices are inherently better for high-voltage operations, in terms of gate oxide reliability and punchthrough capability. The programming speed of an NOI device is still less than that of the currently used NROM because NOI has a low fringing field in the charge injection region. Nevertheless, the full compatibility with industrial logic processes and the need for no extra mask are the major advantages of NOI devices. This programming speed can be improved by increasing the fringing field, but the gate oxide then suffers from reliability issues. Simulation and measurement results suggested that increasing the gate oxide thickness of the NOI will relieve the gate oxide stress and maintain a sufficient tunneling oxide field over the NOI channel to enhance charge injection.

Fig. 9 also presents the erasing characteristics of new NOI devices. The erasing speed was characterized with V_D fixed at 7 V and V_G varied from -2 to -4 V. For fixed V_D, V_G can be varied to increase the erasing speed and the programming speed of the new NOI devices. Under the same erasing conditions, $V_G = -1$ V and $V_D = 7$ V, the new NOI device is slower than that previously described [10]. The erasing speed is improved to about 60 μs under the condition $V_G = -4$ V and $V_D = 7$ V for a V_{th} shift of -0.8 V. The erasing speeds of those devices in the cited literature [10], [11] are also highlighted in Fig. 9 for direct comparison. Unlike the conventional SONOS-type NVMs, the new NOI device has a fast erasing speed that is of the same order of magnitude as its fastest program speed in the experiment conducted herein.

B. Disturbance, Cycling Endurance, and Charge Retention

The effects of high drain field disturbance under P/E bias (namely $V_D = 7$ V) on the NOI device must be verified in array patterns that correspond to two basic cases: 1) common drain and 2) common S/D. Fig. 10 plots the V_{th} loss of the programmed and erased bits under two disturbing prevention conditions for 1) suppression of common drain disturbance and 2) suppression of common S/D disturbance. The V_{th} loss of programmed bits can be effectively suppressed under these two disturbing prevention conditions. The P/E window closure is as large as 0.18 V for a disturbing time of 10 s under the condition $V_G = V_S = V_B = 0$ V and $V_D = 7$ V. It can be well suppressed to only about 0.04 V by applying the other condition, which is $V_G = V_S = 3.5$ V, $V_D = 7$ V, and $V_B = 0$ V.

The new NOI nMOSFETs with extended SiN spacer lengths have advantages in relaxing the oxide field under high-voltage programming conditions based on the above simulation. A simple V_G switching operation without changing the applied V_D

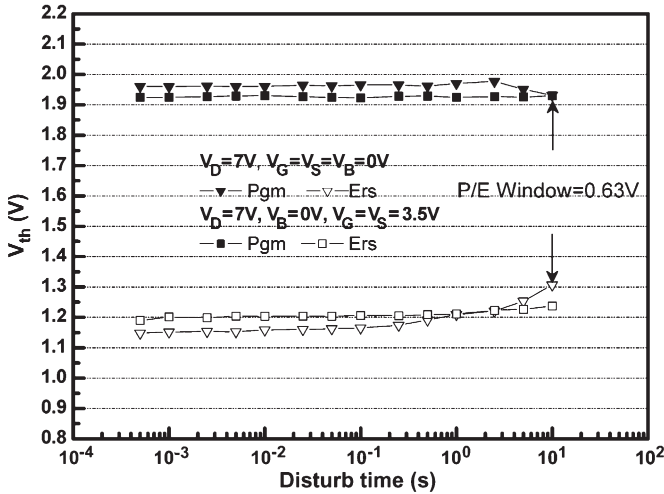

Fig. 10. $V_{\rm th}$ shifts of programmed and erased bits are measured under two disturbing prevention conditions $V_G/V_D/V_S = $ 0/7/0 V and 3.5/7/3.5 V. The P/E window closure can be well suppressed to about 0.04 V by applying the condition $V_G = V_S = $ 3.5 V and $V_D = $ 7 V.

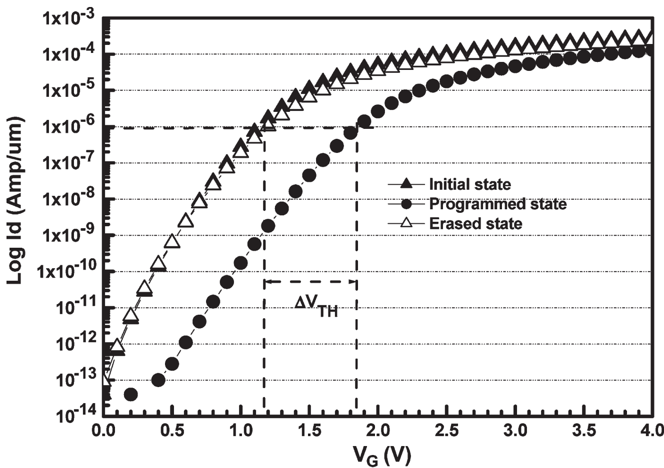

Fig. 11. Typical I_D–V_G curves of the current NOI nMOSFET in initial, programmed, and erased states. They are measured by the "Reverse Read" scheme at $V_D = $ 1.5 V.

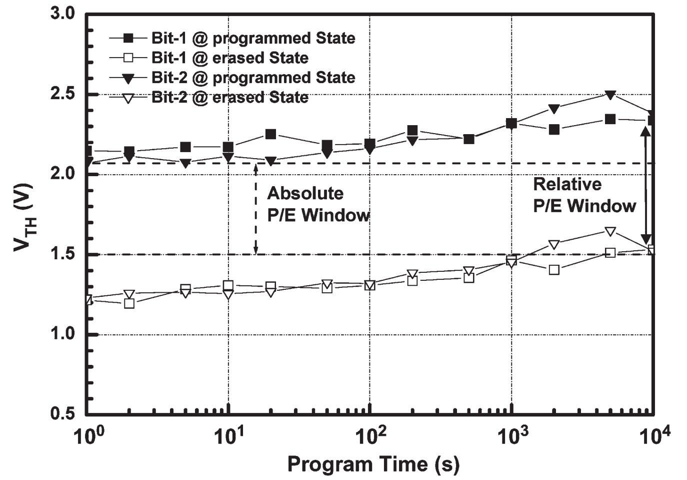

Fig. 12. Cycling endurance of the new NOI nMOSFET is examined. The NOI's P/E window between programmed and erased states remains 90% of its initial P/E window at 10K cycles.

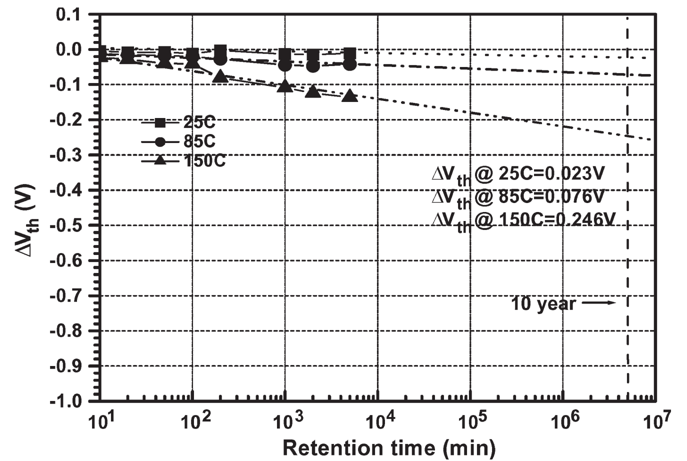

Fig. 13. Charge retention of an NOI nMOSFET with one single bit programmed is characterized under various temperature conditions. An extrapolated $V_{\rm th}$ loss of 0.25 V is observed under 150 °C for ten years.

was used for both programming and erasing NOI. Fig. 11 plots the typical I_D–V_G characteristic curves of an NOI nMOSFET in initial, programmed and erased states. The $V_{\rm th}$ shift reaches 0.8 V after programming, and $V_{\rm th}$ returns to its initial state after erasure. A very little mismatch exists between the initial and erased I_D–V_G curves. This mismatch may be attributed to the difference between programming and erasing carrier injection sites and distributions [14].

The endurance of a cycled NOI nMOSFET is again shown to be much improved, as illustrated in Fig. 12. One P/E cycle comprises the sequence bit-1-programmed, bit-2-programmed, bit-1-erased and bit-2-erased. An overerase approach is used to improve P/E window separation. This P/E cycling scheme can be implemented more than 10K times. However, it has a similar positive $V_{\rm th}$ shift in both programmed and erased states, as described in the cited work [10]. Throughout 10K cycles, the absolute P/E window between the minimum programmed state and maximum erased state is kept at 50% of its initial P/E window. At 10K cycles, the P/E window between the programmed and erased states remains 90% of its initial P/E window, and is better than that described in the cited work [10] for the same number of cycles. After 10K P/E cycles, the NOI device is degraded by damage to its gate oxide and junctions. No obvious difference exists between bit-1 and bit-2 in two-bit P/E cycling.

Fig. 13 shows the charge retention of an NOI nMOSFET with one single bit programmed under various temperature conditions (25 °C, 85 °C, and 150 °C). A $V_{\rm th}$ loss of less than 0.1 V was found after 5K min at temperatures of 25 °C and 85 °C. A $V_{\rm th}$ loss of NOI devices of as much as 0.25 V is found at the highest temperature, which is 150 °C, as determined by extrapolation to ten years.

IV. Device Scalability

Exploring the scaling ability of NOI devices is important in meeting high density memory demand. The initial $V_{\rm th}$ and the amount of charge trapped in the programmed state under

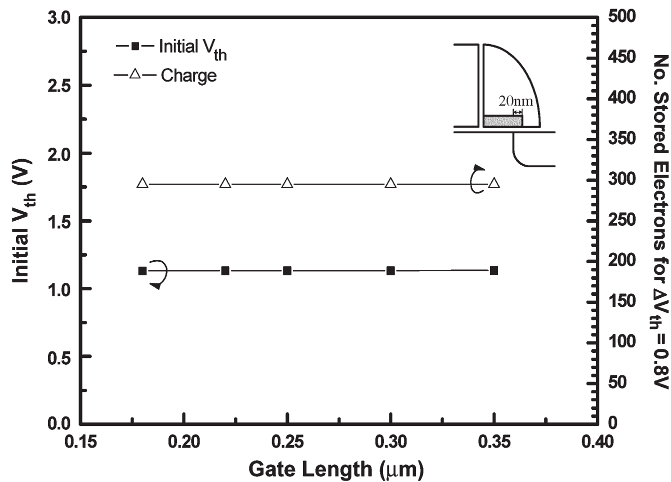

Fig. 14. Initial $V_{\rm th}$ and the amount of stored electrons for $\Delta V_{\rm th} = 0.8$ V are simulated at various gate lengths. The number of required trapped charges is about 300 as the gate length is varied.

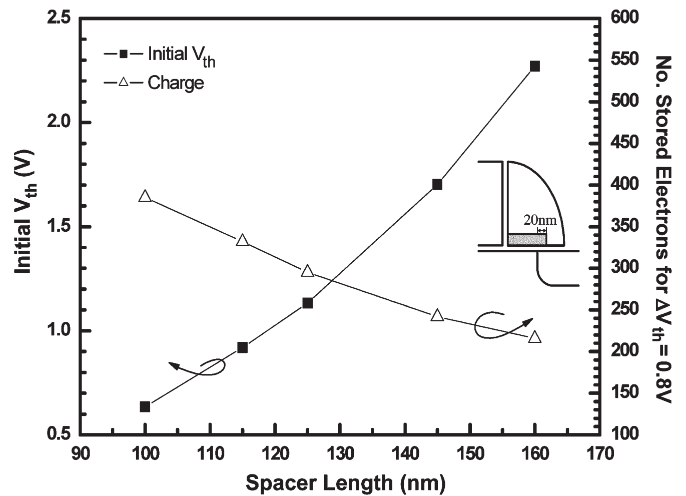

Fig. 15. Initial $V_{\rm th}$ and amount of stored electrons for $\Delta V_{\rm th} = 0.8$ V are simulated at various SiN spacer lengths. As the SiN spacer length increases from 100 to 160 nm, the number of trapped electrons required for $\Delta V_{\rm th} = 0.8$ V decrease from 385 to 216.

various device dimensions are simulated and discussed. The programmed NOI device is simulated by placing a single charge bar in the SiN spacer and above the drain junction. The length of the charge bar equals that of the NOI channel plus a 20 nm overlap on the drain region and the height of the charge bar is a fixed 2 nm [7]. The initial I_D–V_G of the NOI is first simulated without charge trapping, and the results were fitted with measured data. The programmed I_D–V_G is then simulated by adjusting the charge density in the charge bar to represent trapped charges.

A. Gate Length Scaling

The gate length scaling of NOI devices is examined. The initial $V_{\rm th}$ of a NOI device is simulated at different gate lengths, and the results are shown in Fig. 14. The initial $V_{\rm th}$ of nonprogrammed NOI devices correlates weakly with their gate lengths. The initial $V_{\rm th}$ is kept almost constant at 1.25 V while the gate length declines from 0.35 to 0.18 μm. The amount of trapped charges that are required to program a NOI device with $\Delta V_{\rm th} = 0.8$ V is also deduced at different gate lengths, as shown in Fig. 14. The number of required trapped charges is about 300, not varying significantly as while the gate length is scaled.

B. Spacer Length Scaling

Comparing the performance of the NOI herein with that in the cited work indicates that the spacer length is crucial in NOI devices because it is strongly related to the NOI channel length, the fringing field, and the fringing capacitance [10]. Fig. 15 plots the initial $V_{\rm th}$ of NOI devices with various SiN spacer lengths. The initial $V_{\rm th}$ increases from 0.65 to about 2.3 V as the SiN spacer length is increased, indicating that the NOI devices are very sensitive to their SiN spacers. Increasing the NOI channel length reduces the fringing field near the drain junction, such that a higher local threshold voltage is required to turn on the NOI channel [15]. Fig. 15 also plots the simulated amount of electrons that are required to achieve $V_{\rm th}$ shift of 0.8 V in NOI devices with various SiN spacer lengths. As the SiN spacer length increases from 100 to 160 nm, the number of trapped electrons required for $\Delta V_{\rm th} = 0.8$ V decreases from 385 to 216; also, the drain junction moves farther from the gate electrode, reducing the local fringing capacitance, making the local $V_{\rm th}$ more sensitive to the trapped charges. The reduction in the amount of charges required for programming and erasing the new NOI device again improves the P/E speed of the NOI and potentially its tunneling oxide endurance.

V. Conclusion

NOI nMOSFETs with 125 nm SiN spacers were comprehensively simulated and electrically characterized to improve their NVM performance. Their P/E conditions were optimized and had less impact on device reliability as the SiN spacer length increased, because of their reduced gate oxide stress. Under high bias conditions, these NOI devices exhibited improved P/E efficiency (program time $= 40$ μs, erase time $= 60$ μs) for a P/E window of 0.8 V. Their ability to retain charge was substantially improved. The number of two-bit P/E cycles of the new NOI device exceeded 10K times with a P/E window separation of 90% of the initial value. These improvements in speed, cycling and endurance are attributed to not only the optimized operations but also the increased SiN spacer length. Various aspects of both factors, sidewall width and operating voltage, should be considered. The operating voltages essentially affect P/E speed and P/E efficiency. Spacer length tuning may be complicated when the overall characteristics, including device reliability, cell size, and cycling endurance are considered. The scalability of NOI devices is studied based on the major technology nodes in logic devices. The effects of gate length and spacer length scaling were also simulated and discussed. The initial $V_{\rm th}$ and amount of trapped charges in NOI devices are highly sensitive to the spacer length, which directly correlates with fringing capacitance. The SiN spacer

length in NOI devices dominates their scaling. Therefore, different scaling schemes for gate length and spacer length should be used in future NOI scaling. Unlike other SONOS-based memories, NOI devices provide beneficial features and freedom in scaling and individual optimization of the physical dimensions of the control gate, the charge trapping spacer, the gate oxide, and the tunneling oxide in future nanoscale NVM devices. Moreover, NOI devices as single-polysilicon multibits-per-transistor NVM offer advantages of device simplicity and complete compatibility with pure logic CMOS technologies. NOI devices will attract much attention for their potential use in embedded high-density memory applications.

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