Effect of Fin Angle on Electrical Characteristics of Nanoscale Round-Top-Gate Bulk FinFETs

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***Abstract*—In this brief, electrical characteristics of 25-nm round-top-gate fin-typed field-effect transistors (FinFETs) on silicon wafers are numerically explored. With an ideal fin angle (i.e., $\theta = 90^\circ$), the FinFETs with doped and undoped (for this case, the device has a metal gate) channels that was fabricated on silicon and silicon-on-insulator wafers are simulated and compared. With a 3-D quantum-correction-transport simulation, characteristic comparison shows that bulk FinFETs with the undoped channel possess promising electrical characteristics. By considering different short-channel effects, dependence of the device performance on the nonideal fin angle and fin height is further investigated. Optimal structure configuration for the round-top-gate bulk FinFETs is thus drawn to show the strategy of fabrication in sub-25-nm MOSFET devices.**

***Index Terms*—Bulk fin-typed field-effect transistors (FinFETs), fin angle, manufacturability, metal gate, modeling and simulation, round-top gate.**

I. Introduction

FIELD-EFFECT transistors (FETs) with multiple-gate structures, such as fin-type FETs (FinFETs) [1]–[8], have been of great interest for potential sub-32-nm technology application. Excellent controlling ability of carriers in the device's channel is observed on FinFETs, where the short-channel effects (SCEs) are suppressed. Channel doping for adjusting the threshold voltage is still necessary in nowadays manufacturing process. However, heavily doped channel leads to some drawbacks, such as mobility degradation induced by impurity scattering and unexpected dispersion in electrical characteristics. It becomes worse when the feature size of sub-65-nm MOSFETs is continuously scaled. On the other hand, multiple-gate MOSFETs with undoped channel have been extensively studied. At the same time, instead of polysilicon gate, a metal gate is alternatively chosen to substitute in obtaining the proper threshold voltage. The device performance is thus improved by eliminating polysilicon depletion and reducing the gate leakage [6]. In fabricating the nanoscale FinFETs, the minimum dimension of the device has transferred from the gate length to the fin thickness. Top of the fin is formed to a round shape naturally [2], [3], [7], and the fin bottom is not actually rectangular for the lithography and silicon-etching processes. These nonideal processes will result in a wider fin bottom with respect to the fin top; thus, it leads to a slanted edge of the channel fin [2], [3], [7], [8]. Such geometric derivation degrades device performance and raises serious SCEs, such as a large subthreshold swing (SS), low ratio of the ON- and OFF-state currents, and large drain-induced barrier lowering (DIBL). Many studies concerning design guideline and consideration and simulation have been reported for studying multiple-gate devices [9]–[16]. However, effects of geometry aspect ratio of the silicon fin and its fin angle on electrical characteristics for scaled bulk FinFETs have not been clearly explored yet.

In this brief, we numerically explore electrical characteristics of the doped and undoped channel for round-top-gate FinFETs on the silicon and silicon-on-insulator (SOI) wafers. A 3-D device simulation with solving a set of density-gradient-based drift-diffusion equations is adopted and performed to account for quantum–mechanical effects (see, for instance, [5] and references therein). For a device with an ideal fin angle (i.e., $\theta = 90^\circ$), we examine electrical characteristics for 25-nm FinFETs with doped and undoped channels on the silicon and SOI wafers. Among the devices, the bulk FinFETs with an undoped channel exhibit good performance. Particularly, dependence of the round-top undoped bulk FinFETs' performance on nonideal fin angle and the fin height is further investigated, which is subject to different SCEs. By varying the fin angle, in 3-D device simulation, an optimal configuration of structure for the explored round-top-gate bulk FinFETs is drawn, according to manufacturability.

This brief is organized as follows. In Section II, we report and discuss the simulation results. Finally, we draw conclusions.

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II. Simulation Results and Discussion

Electrical characteristics of a 25-nm FinFET with the silicon and SOI substrates, as shown in Fig. 1, are examined first, where the oxide thickness, the fin width, and the fin height are fixed at 1.2, 20, and 50 nm, respectively. The physical settings and simulation results are summarized in Table I. We notice that the parameters are adjusted so that the four explored devices have very similar threshold voltage, and the examination is simply assumed that the simulated devices are with a flat-top gate, where the ideal fin angle of 90° is fixed.

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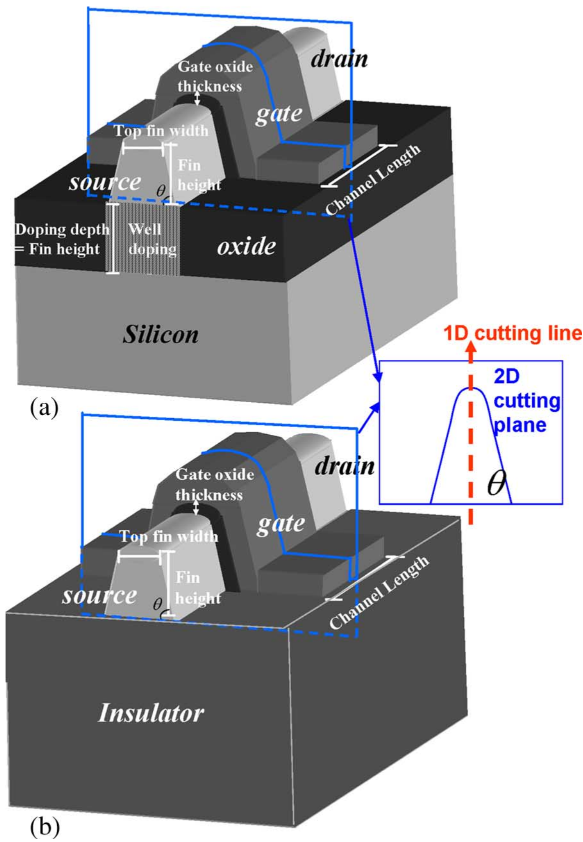

Fig. 1. Three-dimensional schematic plots for the (a) bulk and (b) SOI FinFETs. The symbol θ is the fin angle, and the inset shows a 2-D cutting-plane extracting from the center of the channel.

We observe that the metal-gate device (for this case, the device is with an undoped channel) on silicon bulk wafer exhibits better performance than others with and without heavily doped channel on different wafers. For the round-top-gate FinFETs to be explored as follows, we have performed the same investigation and obtained similar tendency. We further investigate the effect of fin angle on the electrical characteristics for the 25-nm round-top-gate bulk FinFET with the undoped channel, where the work function is 4.45 eV. Different angle of the fin taper is examined subject to the aforementioned electrical characteristics of the device.

For the drain voltage of 1.0 V and the gate voltage of 1.0 V, the distributions of potential and electron density for the device with the fin height = 30 nm [Fig. 2(a)] and 50 nm [Fig. 2(b)] are extracted according to the 1-D cutting line, as shown in the inset of Fig. 1. The plots are devices with three different angles of fin taper as follows: 70°, 80°, and 90°. Nonuniform distributions of the potential and electron density along the longitudinal direction are observed. We notice that all plots of 1-D cutting lines start near the interface of silicon and silicon dioxide. This is a direct result of a donor's and the bias' impacts on the channel along the direction of the fin top to bottom. The potential attains the minimum value at the fin bottom, which increases rapidly toward the fin top. For the same distance, the larger potential associated with the larger fin taper angle is perceived from the fin bottom. The electron density is reduced when the distance (from the top fin) is broadened; similarly, it

TABLE I
PHYSICAL PARAMETERS USED IN THE DEVICE SIMULATION AND THE RESULTS WITH DOPED AND UNDOPED CHANNELS ON SILICON AND SOI WAFERS. THE BULK METAL MEANS THAT THE DEVICE WITH UNDOPED CHANNEL ON SILICON WAFER. THE BULK POLY-Si IS THE DEVICE WITH DOPED CHANNEL ON SILICON WAFER. FOR SOI METAL AND SOI POLY-Si, WE SIMILARLY INDICATE THAT THE DEVICES ARE FABRICATED ON THE SOI WAFER. WE NOTICE THAT THE SLIGHTLY DIFFERENT VALUES OF THE PARAMETERS HAVE BEEN ADOPTED, WHICH ARE MAINLY FOR ADJUSTING VERY SIMILAR THRESHOLD VOLTAGE AMONG DEVICES

	Bulk Metal	Bulk Poly-Si	SOI Metal	SOI Poly-Si
Gate workfunction (eV)	4.45	4.17	4.505	4.17
Well doping (cm^{-3})	10^{18}	10^{18}	0	0
Source / Drain doping (cm^{-3})	10^{20}	10^{20}	10^{20}	10^{20}
Channel doping (cm^{-3})	10^{16}	$4.68\text{x}10^{18}$	10^{16}	$4.6\text{x}10^{18}$
Background doping (cm^{-3})	$1\text{x}10^{15}$	$1\text{x}10^{15}$	$1\text{x}10^{15}$	$1\text{x}10^{15}$
DIBL (mV)	37	82	56	66
SS (mA / mV)	71.83	81.48	76.75	78.3
Ion / Ioff	$3.08\text{x}10^{7}$	$3.35\text{x}10^{6}$	$5.06\text{x}10^{7}$	$6.82\text{x}10^{6}$

has the minimum value at the fin bottom. For the device with the fin height = 30 nm, as shown in the left plot of Fig. 2(a), we find that the case of 90° (i.e., the solid lines) exhibits the most uniform distribution of the potential in the center of the channel. The potential decreases more quickly with a more slanted fin angle, which leads to a stronger longitudinal electric field and may degrade the device performance. Similar results can be observed for the cases with a fin height of 50 nm. Moreover, it is found that the variation of potential almost keeps constant within the longest distance inside the channel region. The potential variation is significant when the fin angle is decreased, and the case of 70° (the dashed lines) possesses the largest potential variation among the three angles. The variation is even more appreciable when the fin height is increased. For the different fin angles and fin heights, the right plots of Fig. 2(a) and (b) disclose the variation of the electron density versus the distance from the fin bottom. The variation of this physical quantity predicts the same trend as depicted earlier. It is found that the device with an approximately ideal fin angle (i.e., the fin angle approaches to 90°) has the most uniform distribution of the examined physical quantities within the device channel.

Plots of the drain–current versus the gate voltage for the three fin angles and two fin heights are shown in Fig. 3(a). The case for the fin height of 30 nm, as shown in the left plot of Fig. 3(a), allows a larger variation of the fin angle, compared with the result of the fin height = 50 nm. It means that the fin height of 30 nm maintains the highest ratio of the ON- and OFF-state currents and implies better performance. The parameters of SCE versus the fin angle are calculated accordingly, as shown in Fig. 3(b). We notice that a larger taper angle is necessary for fabrication of nanoscale bulk FinFETs

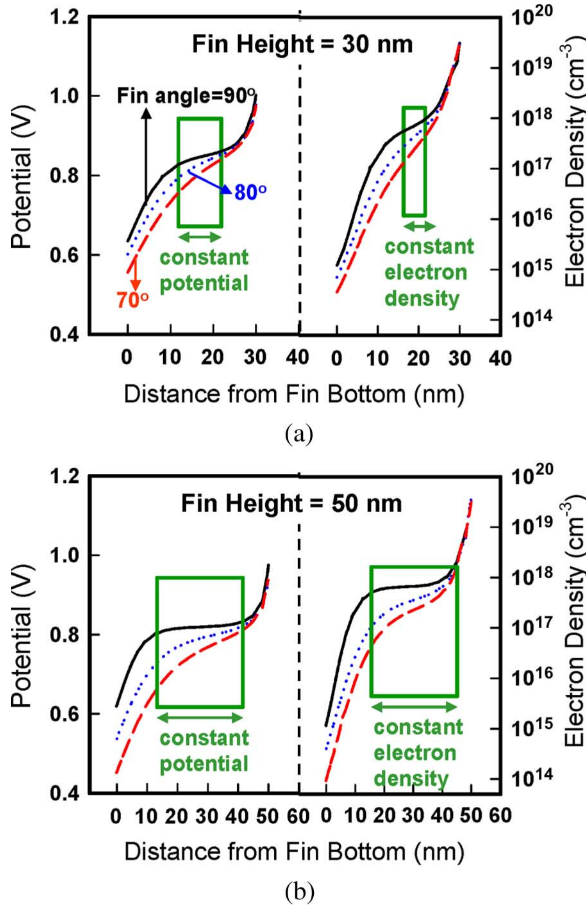

Fig. 2. Plots of 1-D cutting lines of the potential and electron density at the center of the channel. The device is with the fin height of (a) 30 and (b) 50 nm, where the solid line is the result for the 90°, the dotted line is for the 80°, and the dashed line is for the 70°. The circled windows indicate the regimes where nearly constant potential and electron density occurred in the device channel.

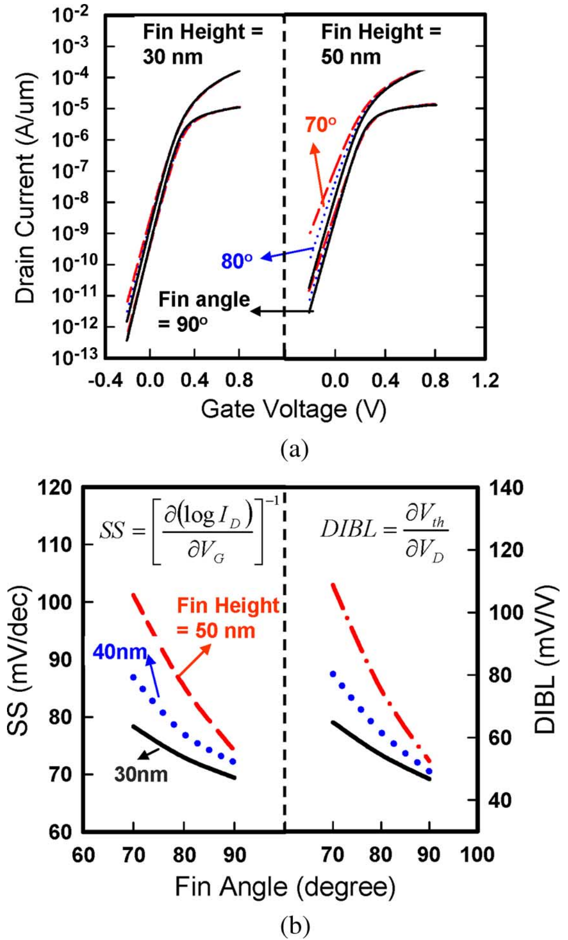

Fig. 3. (a) Characteristics of the drain–current versus the gate voltage for the device with respect to different fin angles and heights. The solid lines are the result for the 90°, the dotted lines are for the 80°, and the dashed lines are for the 70°. (b) Results of (the left plot) SS and (the right one) DIBL versus the fin angle, where the solid lines are the result for the 30 nm, the dotted lines are for the 40 nm, and the dashed lines are for the 50 nm.

to obtain robust electrical characteristics. Besides, Fig. 3(b) implies that a smaller fin height is essential for the device of 25-nm gate length. The calculated SS suggests that an increase of the fin angle will result in better SS; in particular, for those silicon fins with higher fin height, which improve the SCE remarkably. Similarly, we also find the evidence for the DIBL. Consequently, for the cases with a small fin angle, the device may not have an acceptable performance. In addition, for the bulk FinFET with a high fin height, the situation is getting worse simultaneously. For this reason, we summarize that the fin height and the fin angle are the two critical limiting factors when the dimension of the bulk FinFET is continuously scaled down. In a word, they are the most important parameters that have to be optimized according to the fabrication point of view. A structure of bulk FinFET with a nearly rectangular configuration leads to better electrical characteristics. If the ratio between the fin height and the top-fin width (i.e., the fin height/the top-fin width) is greater than one, then the fin taper angle improves the device characteristics significantly. Therefore, for the device with a large ratio between the fin height and the top-fin width, the controllability of manufacturing the fin taper angle is exceptionally important, and much more effort on processing should be made.

III. CONCLUSION

In this brief, electrical characteristics of nanoscale bulk FinFET have been numerically studied by using a 3-D density-gradient drift-diffusion simulation. For the studied 25-nm bulk FinFET, the ON-state current, the SS, the DIBL, the distribution of electrostatic potential, and the distribution of electron density have been calculated with respect to different fin taper angles. The SCEs are degraded due to slant of the sideward wall of silicon fin. Nonrectangular structure of fin leads to current crowding and deteriorates the performance of a device. Consequently, we can conclude that fin height and the fin angle of a device are the two most important parameters in optimizing the fabrication processes. A nearly rectangular-shaped fin is only crucial for the device with a higher fin height. The critical angles for the case of SS $<$ 75 mV/dec and DIBL $<$ 75 mV/V are summarized in Table II. We can find the critical angles when fin height/top-fin width = 1.5, 2, and 2.5, and the critical angles are 71.9°, 79.3°, and 87°, respectively. Therefore, with a larger fin height/top-fin width, the critical angle becomes larger and approaches 90° (the most severe limitation), which means that an ideal rectangular shape of fin is necessary for good electrical characteristics.

TABLE II
LIST OF THE SUGGESTED DESIGNING PARAMETERS FOR FABRICATION OF NANOSCALE BULK FinFETs

Fin height (nm)	30	40	50
Fin height / Top fin width	1.5	2.0	2.5
Critical angle (degree)	71.9	79.3	87.4

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