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Microelectronics Reliability 47 (2007) 2100–2108
MICROELECTRONICS RELIABILITY
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Effects of width scaling and layout variation on dual damascene copper interconnect electromigration

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Received 6 June 2006; received in revised form 3 October 2006
Available online 1 December 2006

Abstract

Electromigration versus line width in the 0.12–10 μm range and the configuration of the via/line contact in dual damascene Cu has been investigated. There are two scenarios for width scaling impact on electromigration. One is the width < 1 μm region, in which the MTF shows a weak width dependence, except for the via-limited condition. The other is the width > 1 μm region, in which the MTF shows a strong width dependence. A theory was proposed to explain the observed behavior. For polycrystalline lines (width > 1 μm), the dominant diffusion paths are a mixture of grain boundary and surface diffusion. The activation energy for the dominant grain boundary transport (width > 1 μm) is approximately 0.2 eV higher than that of the dominant surface transport (width ~ 1 μm). The derived activation energies for grain-boundary and surface diffusion are obtained from Cu drift velocity under electromigration stressing. The mechanisms governing the electromigration lifetime of interconnects leads to via interconnect design rules for maximizing lifetime being identified.

1. Introduction

Electromigration (EM) is critical wear-out mechanism in copper metallization, limiting the lifetime of interconnect systems. EM failure leads to void formation at the cathode and extrusion at the anode. The EM reliability issue has been very important in interconnect technology since Al thin film wires were found to exhibit EM in 1966. Over the past 40 years, Al has been the interconnect conductor of choice in the microelectronic industry. The drive toward improved chip performance has resulted in a rapid push toward greater circuit density. Higher circuit density is a consequence of shrinking wire dimensions. This aggressive wire dimension scaling has resulted in an increase in current density. The probability of circuit failure induced by EM increases when current density increases. The back-end-of-line (BEOL) RC delay has gradually become a major limiting factor in circuit performance as a result of the rapid shrinking of critical dimensions. With reduced resistivities and dielectric constants, the metallization system for the interconnect structures has shifted from Al(Cu)/oxide to copper/low-*k* dielectrics. The reliability of Cu/low-*k* interconnects thus has become an important topic in 0.13 μm technology node and beyond [1]. Cu electromigration reliability is the key issue that limits the lifetime of advanced interconnect systems [2]. The rapid decrease in Cu conductor dimensions while maintaining a high current capability and a high reliability emerges as a serious challenge.

Many studies have investigated methods of optimizing the Cu electromigration performance of narrow interconnects (<1 μm). Lloyd et al. [3] found that the adhesion between Cu and the upper surface cap material directly correlates to the electromigration lifetime. Hatano et al. [4] reported an improvement in electromigration lifetime using a P-SiC cap layer when compared to P-SiN. Hu et al. [5] reported an improved electromigration lifetime for Cu interconnects with a selective electroless metal coating of CoWP, CoSnP, or Pd, on the top surface of Cu damascene lines. Fischer et al. [6] and Glasow et al. [7]

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doi:10.1016/j.microrel.2006.10.004

discussed the influences of the preclean process after via etch and SiN cap deposition for a variety of preclean intensities. Process improvements are necessary to enable an increase in EM performance, while some geometric features of the testkey design also play a significant role in EM [8]. On one hand, the effect of via/line contact configuration was examined in this work. On the other hand, the effect of width scaling on EM was investigated to identify the EM diffusion mechanism. EM involves atomic diffusion, typically along the dominant diffusion path. In contrast to Al-based interconnects, it has been shown that microstructure does not play a dominant role in the EM of Cu interconnects [9]. The fastest diffusion path is the Cu/cap interface [10,11], and the second fastest is the grain boundaries or Cu/liner interface [12], the slowest path should be grain bulk. Once the Cu diffusion along the top surface has been sufficiently slowed, the grain structure or interface boundary should affect reliability. The microstructure characteristics and the EM in Cu damascene line have been reported [13–15]. The grain size decreased as the line width decreased. Electroplated Cu has relatively larger grains, resulting in a longer EM lifetime than the CVD Cu. For wide lines, CVD Cu (3 μm) polycrystalline structure, and narrow lines (0.5 μm), quasi-bamboo structure, provide almost the same activation energy $E_a \sim 0.65$ eV. Even with a polycrystalline orientation, PVD Cu samples showed a better activation energy value $E_a \sim 1.02$ eV. However, a question remains as to why the PVD Cu process showed such a higher E_a value than that of the CVD Cu process. It may be that surface diffusions have less effect, meaning that a higher E_a value was obtained from the experimental samples having a quasi bamboo grain microstructure using PVD Cu process. The interaction between the surface and the grain boundary diffusion provided the impetus for the investigation into electroplated Cu dual-damascene process. However, few studies have reported on the effect of line widths from $w = 0.14$ μm to 10 μm on the MTF values. Therefore, the present study focuses on the effects of the wide linewidths region. The effects of width scaling were evaluated after Cu/cap process optimization, that is to say the surface diffusion is sufficiently slow. Electromigration experiments were conducted in wide and narrow lines in order to emphasize the main diffusion path in a full Cu dual-damascene process. Especially, suitable EM test structures were designed to evaluate the properties of Cu. These test structures were more realistic than pure metal lines, and used a sufficient number of via to eliminate any via-limited failures. The effect of width scaling on EM has been investigated to identify an EM diffusion mechanism that may be different for both narrow lines and wide lines. A theory was proposed to explain the results.

2. Experimental detail

The EM tests were carried out at the package level. Samples were fabricated using a 90 nm Cu dual damascene process on 300 mm wafers. The film stacks in the test structures were fabricated using a dual-damascene process in which both the via and line were etched into the low-k dielectric followed by backfilling with a liner, a Cu seed, and electroplated Cu. The excess Cu and liner films were removed by chemical mechanical polishing process. The TaN/Ta liner and Cu seed layers were deposited sequentially by using physical vapor deposition (PVD). In addition, re-sputtering leads to excellent side wall coverage and void-free vias. Testing was typically conducted at 300 °C with a current density of $1.2–2.0 \times 10^6$ A/cm^2. The EM failure criterion was defined as a 10% increase in resistance, or when the extrusion monitor current exceeded 1 μA. Fig. 1(a) and (b) are schematic diagrams of the three-level interconnect structures discussed in this paper. The line length was designed to be 400 μm long to minimize the effect of EM induced back flow. The down-stream case is defined according to the electrons flowing from the upper wide metal line over the via into the narrow metal line below. While, the up-stream case is defined according to the electrons flowing from the lower wide metal line under the via into the narrow metal line above. The sample size per EM test was greater than 20. Stress temperatures were in the range of 250–350 °C (typically 300 °C). In order to determine the effect of Joule heating, we measured sample resistance as a function of current and temperature. The difference between the increase in sample resistance during stressing (high) and measuring (low) current is attributed to increases in temperature due to the Joule heating effect. The applied stressing current ranged from 0.4 to 24 mA; the measuring current was 0.1 mA. The sample temperatures ranged from 25 to 350 °C. The relation between metal resistance and temperature is given by $\mathrm{TCR}(T) = [1/R(T)]\Delta R/\Delta T$, where TCR is

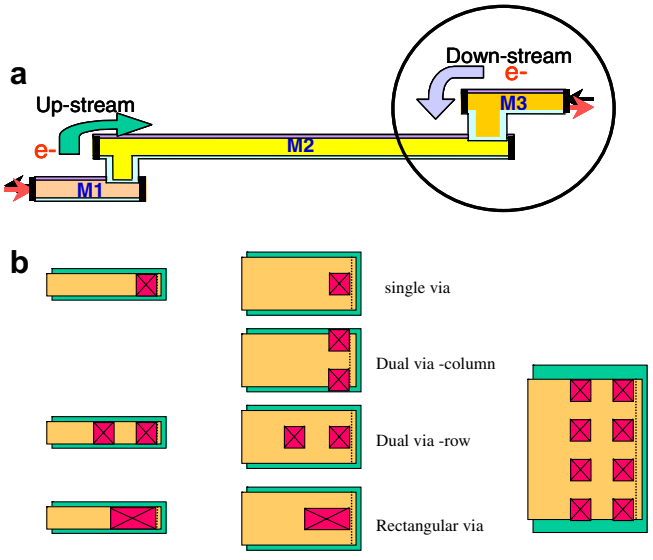

Fig. 1. Schematics of EM test structures used. (a) Via terminated line structure. Line length is equal to 400 μm. (b) Various EM structures for width dependence, left $w = 0.14$ μm, middle $w = 0.42$ μm, right $w > 0.42$ μm. Stress direction is defined by electron current flow direction. Down-stream is evaluated.

the temperature coefficient of resistance, R is the resistance, and T is the sample temperature. TCR was determined by resistance measurements in steps of 50 °C in the range from 50 to 300 °C. The correlation between R and T within the investigated temperature range was close to linear. The average TCR value is estimated at $0.0030 \pm 0.00016\ ^{\circ}C^{-1}$ with 271 samples, whose line width are at 0.14 μm, for a specific process. Reduced stress current densities in the range of $0.6–2.0 \times 10^6$ A/cm^2 (defined with respect to the cross section of the metal line) were used to control the temperature rise due to Joule heating to less than 3 °C even for low-k materials known for possessing small thermal conductivity. Testing was conducted typically at 300 °C at a current density of 1.6×10^6 A/cm^2.

3. Results and discussion

3.1. The via/line configurations on EM performance

EM test structure of various widths were designed to evaluate the effects of width scaling on EM performance. The direction of current used to apply the stress had a marked effect on EM results in the via-terminated three-level metal line structure and related failure modes. In order to examine the worst case EM performance, the structures were tested using currents applied in both directions. As can be seen in Fig. 2, the up-stream results for two different metal line widths showed a much better EM lifetime performance than in the down-stream case. A brief explanation is described as below. The dominant failure mode for up-stream case is voiding along metal lines above the via. A large volume of Cu is necessary to cause significant resistance change. The probability of voiding inside the upstream stressed via is very low as a result of excellent gap filling of via. However, for the down-stream case, failure modes corresponding to voiding in the via/metal interface was found. A small amount of Cu depletion around the via/metal interface can cause a large resistance change and requires a much shorter time to cause via/metal interface depletion than metal lines depletion. The following EM results in this work are stressing in down-stream current direction. The cumulative lifetime data for lines 0.14–0.42 μm in width, fitted using a lognormal distribution, is shown in Fig. 3, and the values of σ in the lognormal distributions, even in wider lines, are all quite similar. The median time to failure (MTF) was measured at different line widths, and the results are plotted in Fig. 4(a). The MTF decreases sharply as the line width increases in the range below 0.42 μm. Voids, which grow at the bottom of a via, cause the line to fail [16]. Due to large current crowding, and the lack of liner redundancy [17], design rules that allow maximum width with a single via show the worst MTF result. The maximum current allowed to pass through the interconnects defined by the EM rule is proportional to the width of the line, while the maximum current allowed to pass through individual via is defined per via. As the line width increases to a point that allows current of line to be larger than allowed to pass through the via, the MTF will be restricted by the via current limitations. To remove the restriction on the current imposed

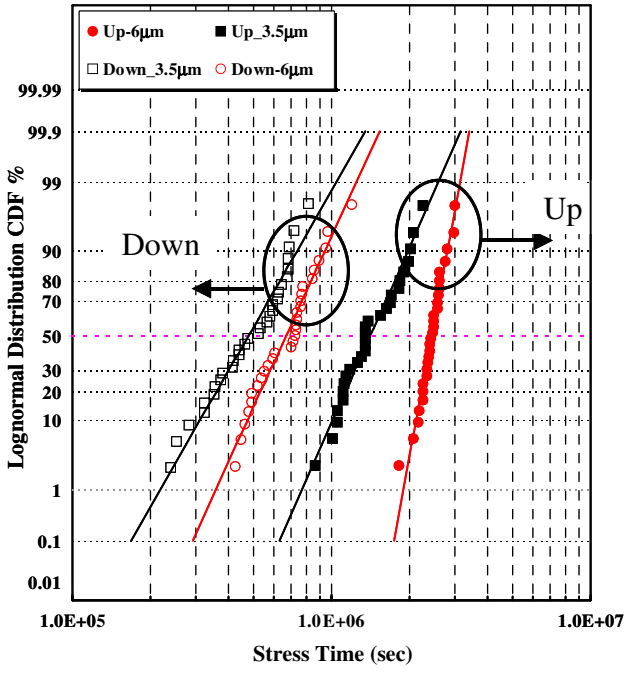

Fig. 2. Typical time-to-failure distribution plots for up-stream and down-stream cases. The sample size is more than 24 for up-stream/down-stream case. EM fail time obtained at 300 °C under current density of 1.6×10^6 A/cm^2. The worse case is down-stream direction.

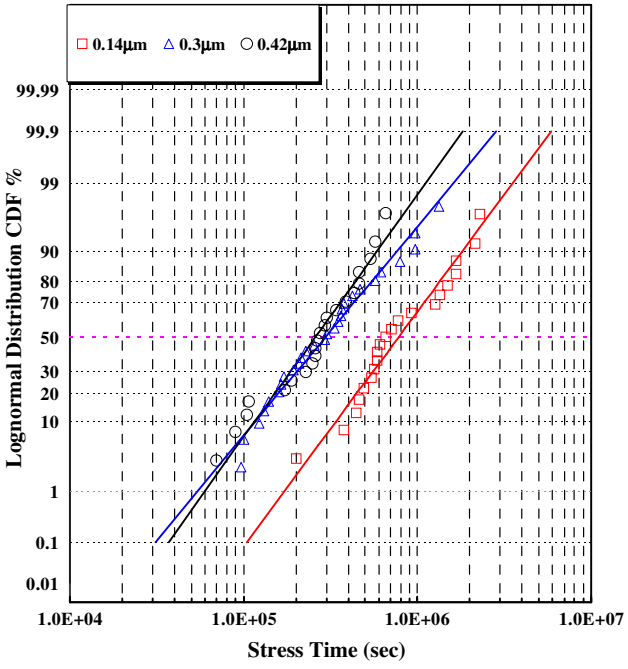

Fig. 3. Lognormal time-to-failure distribution plots for $w = 0.14$, 0.3, 0.42 μm for down-stream case. Similar distributions are shown. Stress conditions are the same for all tests.

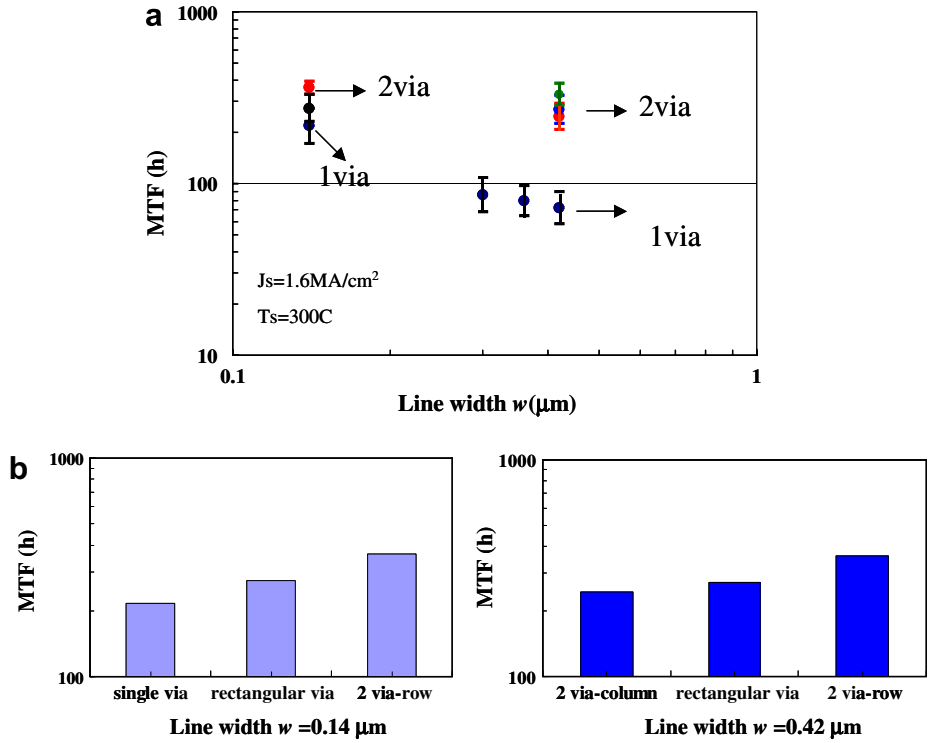

Fig. 4. (a) Plot of the MTF as a function of linewidth ($w < 0.42$ μm), 90% confidence levels are lower and upper bound. (b) Plot of the MTF of different via/line configurations for 0.14 and 0.42 μm, stress conditions are the same for various structures.

by the via-limit on wide lines, dual vias are designed to relieve the via-related failure mode. For 0.42 μm wide lines, three different via arrangements were designed, i.e. a rectangular via, a dual via-row, and a dual via-column. The MTF increased by more than three times when compared to a single via structure. The variation of the MTF for different dual via designs is shown in Fig. 4(b). It is obvious that for wide lines with a dual via-row, which are parallel to the line length, the MTF is the longest due to the requirement for a large volume of Cu depletion. The MTF of the rectangular via decreases around 20% compared to that of a dual via-row. However, the width of the lines beneath the test structure can be decreased for the rectangular via, which is a trade-off between reliability and line routing design area. The results may be explained by considering the Cu reservoir effect on EM. Reservoirs are metal parts that act as a source to provide atoms to areas where the atoms migrate away due to electrical current. The use of such reservoirs can prolong EM lifetime; this is called the ''reservoir effect''. The modeling and experimental characterization of 'reservoir effect' around via's on Al interconnect which drastically can influence lifetime have been reported [18,19]. For a 0.14 μm narrow line, the MTF of the dual via-row is around 1.6 times that of a single via. In comparison with a 0.42 μm wide line, the MTF of dual via-row increases to 4.6 times that of a 0.42 μm wide line with single via. It is interesting that for structures using a dual via design, the MTF of a 0.42 μm line is very close to that of a 0.14 μm line. The via-limit restriction on allowed current passing line, the case where a single via limits the EM performance in a 0.42 μm wide line, are eliminated. The via-related fails will not contribute to the current carrying capability for lines. The results indicate that the via/line configuration has remarkable impact on the current carrying capability in interconnects system. The via/line contact configuration needs to be evaluated for layout design.

3.2. The microstructure grain size of Cu

The grain sizes were revealed by FIB in dual-damascene lines with the geometry of electromigration patterns. The microstructure of Cu in line trenches can be very different from that of a blanket film since the grain growth is confined by the width of the trenches. The microstructure of Cu must be quantified as dual-damascene lines. Fig. 5(a) show top view FIB images of 0.14 μm, 0.42 μm and 1 μm wide EM patterns lines. A bamboo-like microstructure was found in the 0.14 μm lines, while a mixture of bamboo-like and polycrystalline structure was found in the 0.42 μm wide lines. The wide lines (1 μm) show a polycrystalline line structure where many grains coexist in the line width. The average grain size and dispersion were calculated for various line widths, and a lognormal distribution of grain size was assumed, using a mean lineal intercept, or Heyn's technique. The mean lineal intercept length is the average length of a line segment that crosses a sufficiently large number of grains. An example of a lognormal plot

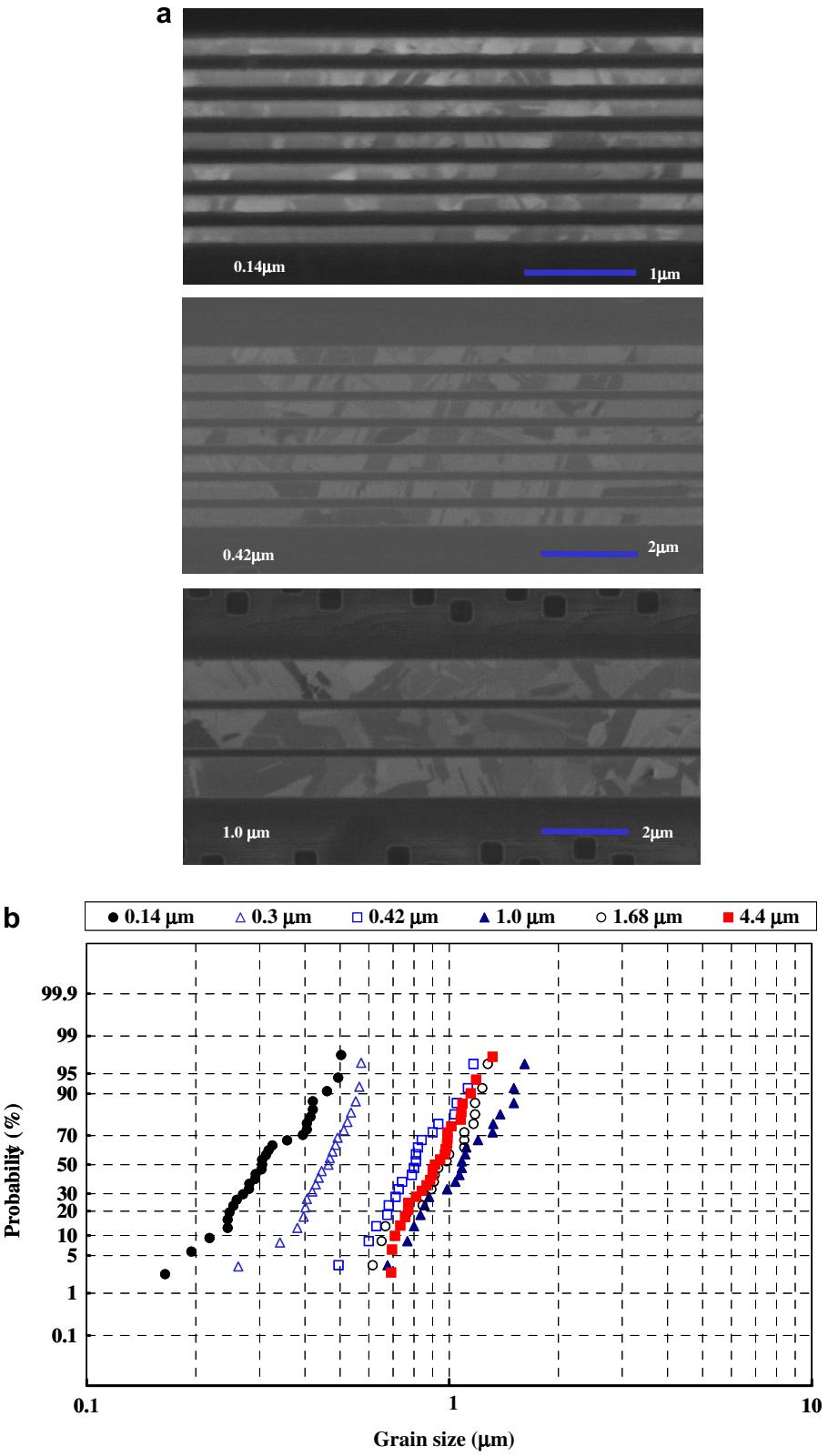

Fig. 5. (a) FIB images of 0.14 μm (top), 0.42 μm (middle) and 1.0 μm (bottom) EM structures, bamboo like and mixture microstructure are shown. (b) Grain size distribution versus line widths.

of the grain size for various widths of electroplated Cu lines is shown in Fig. 5(b). They are quite well lognormal distributed. Table 1 summarizes the medium grain size and standard deviation for each sample investigated. The median grain size decreases when the line width is smaller than the grain size. However, median grain size values can be

Table 1
Median grain size (probability = 0.5) (D) and standard deviation (σ) versus metal line widths

Linewidth (μm)	D (μm)	σ
0.14	0.30	0.09
0.30	0.46	0.08
0.42	0.80	0.18
1.00	1.08	0.27
1.68	0.96	0.20
4.40	0.91	0.16

larger than the width of the line, such as a value of 0.3 μm observed in the 0.14 μm Cu lines. A quasi-bamboo microstructure was also observed in narrow lines. Although different line widths show various grain sizes, the MTF shows weak width dependence. These results further confirm that microstructure does not play a dominant role in Cu electromigration if the via-limited issue is eliminated. For line widths larger than 1 μm, the median grain size decreases slightly, and the value is very close to 1 μm.

3.3. The behavior of EM MTF on wide line regions

The cumulative lifetime data for the 1–3.5 μm wide lines are shown in Fig. 6, and the values of σ, even in wider lines, are all about 0.3. The failure mode remains unchanged. SEM images illustrating failure samples for 1.68 μm are shown in Fig. 7. The images for various samples show almost the same void size. The void shape indicates that the void probably started at the first via, and then continued to expand until it reached the second via. Here, the bottom of the vias is exposed, and an instantaneous fail is shown on the relative resistance plots, or line failed by open-circuit failure. No voids were found to have formed directly under the via bottom, such as a very thin slit void. It is reasonable to assume that EM lifetime does not degrade by via-limited issue. The temperature coefficient of resistance (TCR) has been used as a parameter to qualitatively monitor the Al metal properties [20]. TCR values have been investigated with regard to median grain size and defects in the crystal lattice, respectively. High TCR values indicate large median grain sizes, whereas low TCR values correspond to a fine-grained microstructure. The correlations between TCR and both the microstructure and the stress-voiding behavior of Cu interconnects were comprehensively investigated in a previous work [15]. The TCR value was found to increase monotonically with linewidth, but reached a maximum where $w \sim 1$ μm and then slightly decreased to a constant value, as shown in Fig. 8. Since the thickness of the electroplated Cu film before CMP is 1 μm, the grain size is limited by the deposited Cu thickness rather than by the metal width. The MTF as a function of linewidth is plotted in Fig. 9. Here, the MTF of linewidth for $w = 0.14$ μm was got from 1-via case, while the MTFs of linewidth in a range of $0.42 < w < 1.0$ μm were obtained from 2-via case. The purpose of the MTF data extraction from different via cases is to maintain EM

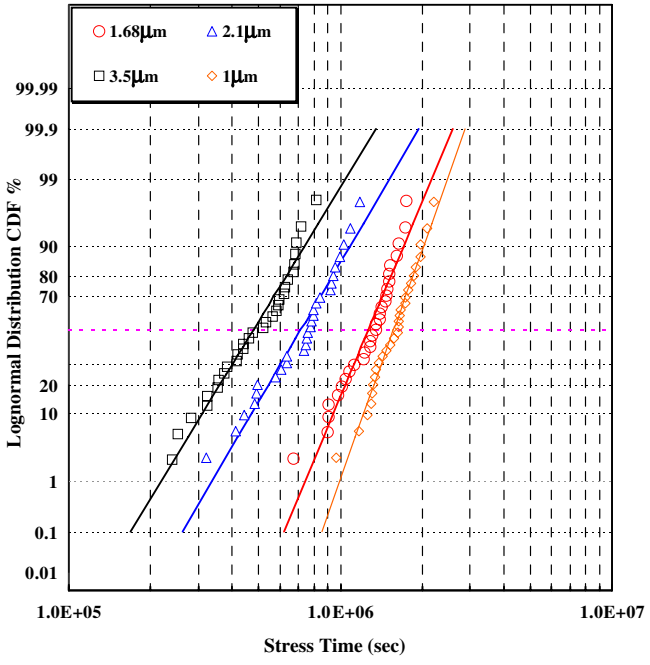

Fig. 6. Lognormal time-to-failure distribution plots for $w = 1$, 1.68, 2.1 and 3.5 μm for down-stream case. Similar distributions are shown. Stress conditions are the same.

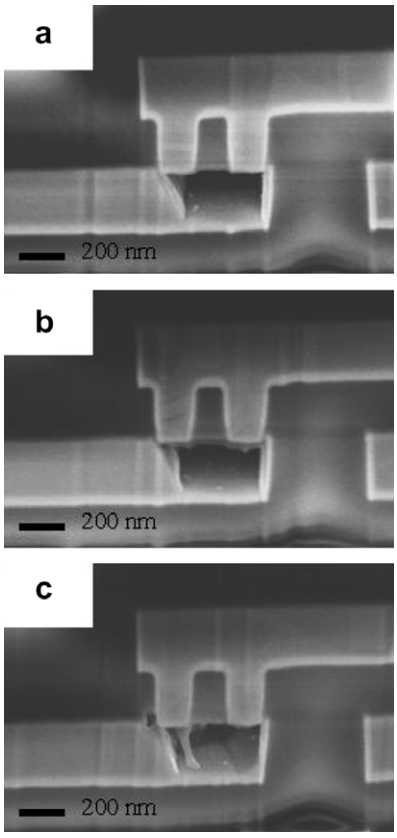

Fig. 7. SEM images for $w = 1.68$ μm wide line structure. Void was found in via bottom. Large trench void cross other via is depleted. The bottoms of the vias are exposed. (a)–(c) Represent different failure samples.

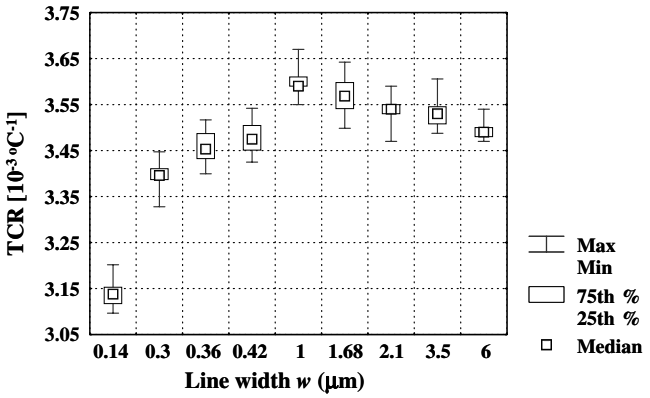

Fig. 8. Plot of TCR as a function of line widths. It reaches a maximum at $w \sim 1$ μm and then slightly decreases to a constant value.

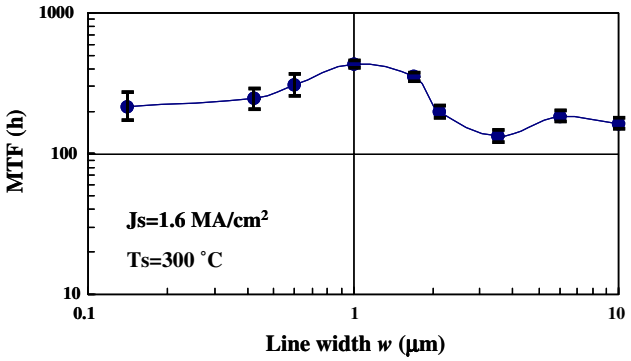

Fig. 9. Plot of the MTF as a function of line widths. 90% confidence levels are lower and upper bounds. For $w > 0.42$ μm, sufficient vias are designed to relieve the via-limited issue. Stress conditions are the same.

performance consistency in various linewidth and to increase via current limitations. To remove the restriction on the current imposed by the via-limit on wide lines, dual vias are used to relieve the via-related failure mode. The MTF slightly increases with linewidth w, but reaches a maximum where $w \sim 1$ μm and then sharply decreases to a minimum where $w \sim 3.5$ μm. Where $w > 3.5$ μm, the MTF slightly increases to a constant value. The observed width dependency behavior can be explained by the equation below. For polycrystalline line structures, the Cu drift velocity can be written as Eq. (1) [10]

$$V_d = [(\delta_{GB}/d)(1 - d/w)D^0_{GB} e^{(-Q_{GB}/kT)} Z^*_{GB} + \underline{\delta_S(1/h)} D^0_S e^{(-Q_S/kT)} Z^*_S + \underline{\delta_I(2/w + 1/h)} D^0_I e^{(-Q_I/kT)} Z^*_I] e\rho j/kT \quad (1)$$

where the subscripts GB, S, and I refer to the grain boundary, surface, and metal/liner interface; respectively, δ_{GB}, δ_S, and δ_I denote the width of the grain boundary, surface, and metal/liner interface; respectively, d is the grain size, and h is the thickness. The mass transport contribution along metal/liner interface is very smaller (10×–100×) than that of through the surface [21], so this term can be neglected. The surface diffusion velocities are almost the same for

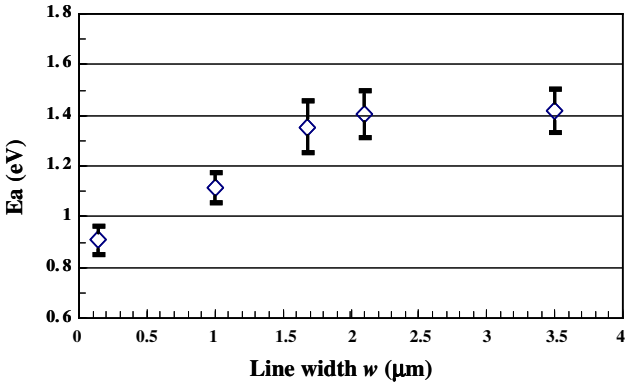

Fig. 10. The activation energy E_a as a function of line widths.

all large w regions. However, for $w = 1$ μm in GB diffusion term, the grain size $d \sim 1$ μm, so the grain boundary diffusion term can be neglected. As a result, the MTF reaches a maximum where $w \sim 1$ μm. Since d is almost the same in the $w > 1$ μm range, as w increases, the impact of grain boundary diffusion on EM will increase. The MTF sharply decreases to a minimum where $w = 3.5$ μm. Thus we see once the Cu diffusion along the top surface is sufficiently slowed, the grain structure or interface boundary should affect reliability. The activation energy represents the energy barrier against the diffusive process resulting in electromigration. Different activation energies are associated with different diffusion paths in Cu interconnects. The plot illustrating activation energy (E_a) versus line width in Fig. 10 further supports the hypothesis. The activation energy where the dominant diffusion transport is the grain-boundary transport (width > 1 μm) is approximately 0.2 eV higher than that where surface mixed grain-boundary transport is dominant (width ~ 1 μm). Lower E_a value for $w = 1$ μm, imply that the surface diffusion term has a significant contribution to mass transport induced by EM. When $w > 5$ μm, dielectric slots are automatically generated to prevent CMP dishing; EM induced atom diffusion will be scattered by the dielectric slot. As a result, the MTF will increase slightly for $w = 6$ μm. However, EM behavior is completely different when $w < 5$ μm.

3.4. The theory of drift velocity on wide line regions

The relative resistance vs. time plots show that the line resistance slowly increases (delta resistance change <1%) for line widths larger than the 1 μm region, followed by an instantaneous rise. The instantaneous resistance increase occurred when the void grew and crossed the via bottom area, as shown in Fig. 7. As most sample failures are instantaneous mode, the void size is approximately equal to the spacing between the vias plus the width of each via. A long line dimension (length = 400 μm) was used in the present study, thus the effect of the EM induced back flow on the drift velocity at the cathode end can be ignored. The drift velocity of Cu is directly related to the rate of displacement

and can be obtained as $v_d = \Delta L/\Delta t$. The Cu drift velocity was estimated using $\langle \Delta L \rangle / \langle \tau \rangle$, assuming a constant drift velocity, where $\langle \Delta L \rangle$ and $\langle \tau \rangle$ are the mean void size and mean lifetime, respectively. We assume that $\langle \Delta L \rangle$ is approximately equal to the spacing between the vias plus the width of each via, and $\langle \tau \rangle$ is equal to the MTF. Fig. 11 shows the mean Cu drift velocity $\langle v_d \rangle$ as a function of line width (w) and sample temperature (T). It is interesting that drift velocity increases as line width increases especially at high temperature while slightly increases to a constant value when the sample temperature decreases. According to the E_a measurement shown in Fig. 10, higher E_a value was obtained on wider line width. It is clear that larger E_a yields higher drift velocity especially at higher temperatures. Because the drift velocity is related to the product of mobility and driving force and uses Nernst–Einstein relation, $\mu = D/kT$, where μ is mobility, D is diffusivity, T is the test absolute temperature, and k is Boltzmann constant. It can be obtained as $v_d = \mu F = (D/kT)F$, where F is driving force, and diffusivity $D \sim \exp(-E_a/kT)$. The phenomenon probably is that gain-boundary density increase creates more flux divergence sites, which induce the void nucleation and formation quickly. The lines are the least-squares fits of the data to Eq. (1). The film thickness ($h = 0.25$ μm), and the value of $e\rho j/kT$ are known. For line widths larger than the 1 μm region, the grain size d is very close to 1 μm since the thickness of the electroplated Cu file before CMP is 1 μm. Eq. (1) can be simplified as following:

$$V_d = [A(1 - 1/w) + B(4)]e\rho j/kT \tag{2}$$

where A corresponds to the grain boundary term,

$$A = \delta_{GB} D_{GB} Z^*_{GB} \tag{3}$$

and B refers to the surface term

$$B = \delta_S D_S Z_S * \tag{4}$$

The solid lines shown in Fig. 11 are the least-squares fits and the best values of fitting parameters (A and B) are extracted. A careful inspection of Fig. 11 shows that error of least-square fitting for a low sample temperature is smaller than that of a high sample temperature. The ratio of B/A increases as the sample temperature decreases with a value range of 0.03–0.1. This implies that the surface diffusion contribution to mass transport induced by EM increases as the sample temperature decreases. It should be noted that the interaction of grain boundary and surface diffusion is temperature dependence. In practice, electromigration assessments are based on tests conducted at accelerated conditions (i.e., high temperature and current density), which are then scaled back to use conditions. A model proposed here indicates that grain boundary diffusion dominates for wide lines at high temperature and surface diffusion contribution to mass transport increases as temperature decreases. It is difficult to predict precisely lifetime at operating conditions without clear relationship between grain boundary and surface diffusion. There is room for further investigation that the top surface diffusion will be the dominant mechanism at operating conditions. The extracted values of fitting parameters from the data in Fig. 11, $\delta_{GB} D_{GB} Z^*_{GB} \rho j$ and $\delta_S D_S Z^*_S \rho j$, as a function of e/kT are plotted in Fig. 12. The activation energies of surface and grain-boundary diffusion are estimated to be 0.92 eV and 1.45 eV, respectively. The derived value of activation energy for grain-boundary diffusion is in favorable agreement with the value of $w > 2$ μm in Fig. 10. This indicates that the major void growth is due to the grain-boundary diffusion for the polycrystalline wide line ($w > 2$ μm). The derived value of activation energy is also very close to the reported value of 0.9 eV [10] for the activation energy of surface diffusion. The derived activation energy of grain-boundary is found to be 0.5 eV higher than that of the surface diffusion. In comparison, the activation energy for the dominant grain boundary transport (width > 1 μm) is approximately 0.2 eV higher than that of the surface and grain-boundary transport (width ~ 1 μm) from E_a measurement. This result further confirms that the grain-boundary term has significant contribution to mass transport induced by EM for the wide line ($w > 2$ μm) region, while the grain-boundary transport contribution decreases at line widths of around 1 μm. It

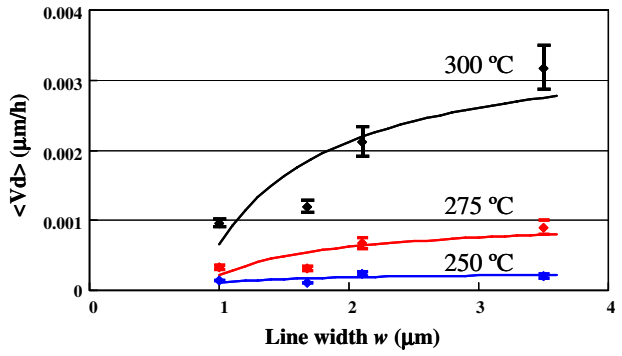

Fig. 11. Plot of mean Cu drift velocity under EM stressing as function of line widths and sample temperatures. The solid lines are least-square fitting.

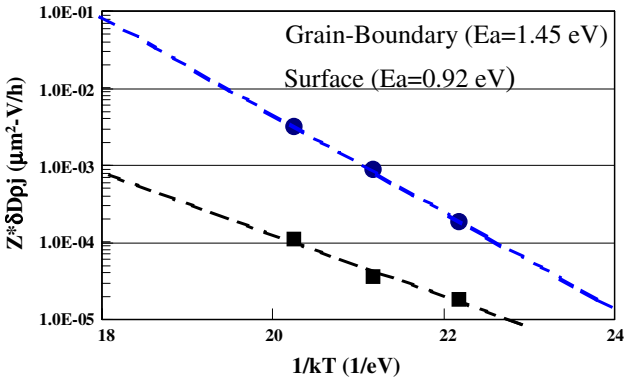

Fig. 12. Plot of $Z^*_S \delta_S D_S \rho j$ and $Z^*_{GB} \delta_{GB} D_{GB} \rho j$ as function of $1/kT$. The solid lines are least-square fitting.

follows from what have been demonstrated that it is consistent with the data and proposed model.

4. Conclusions

In conclusion, the effect of line widths on electromigration in dual damascene Cu interconnects has been investigated. The via/line configuration has remarkable impact on the current carrying capability in interconnects system. The via/line contact configuration needs to be evaluated for critical layout designs. Width scaling was adjusted to improve reliability. There are two scenarios for width scaling. One is the $w < 1$ μm region, in which the MTF shows a weak width dependence, except for the via-limited condition. The other is the $w > 1$ μm region, in which the MTF shows a strong width dependence. The observed EM behavior was well explained by a proposed theory. The derived value of activation for grain-boundary diffusion is approximately 0.5 eV higher than that of surface diffusion. This study may lead to a better understanding of the effects of width scaling and may provide some contribution to the development of line routing for robust EM designs.

Acknowledgements

The authors would like to acknowledge financial support from National Science Council (NSC), Taiwan under contract no. NSC94-2215-E009-009 and thank Dr. A. Fischer and Dr. C.-K. Hu for useful discussions. UMC technology development, reliability and failure analysis groups for many helpful comments and great support are gratefully acknowledged.

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