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前瞻矽奈米元件變異性及傳輸特性綜合研究(II)
研究成果報告(精簡版)

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計 畫 主 持 人：蘇彬

計畫參與人員：碩士班研究生-兼任助理人員：余昌鴻
碩士班研究生-兼任助理人員：江俊賢
碩士班研究生-兼任助理人員：周劭衡
博士班研究生-兼任助理人員：吳育昇
博士班研究生-兼任助理人員：郭俊延
博士班研究生-兼任助理人員：胡璧合

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一、中文摘要

本計畫針對前瞻矽基奈米元件的變異性及載子傳輸特性，進行綜合研究。在工作項目一中，我們探討使用應變矽(strained silicon)對奈米元件隨機匹配之溫度相依性的影響。這項研究不僅對使用先進 CMOS 製程的電路設計很重要，也有助於對矽奈米元件本質參數變異的深入了解。在工作項目二中，我們藉由載子遷移率之超低溫量測與分析，探討應變對矽元件表面粗糙散射遷移率(surface-roughness limited mobility)的影響。這項研究有助於了解應變矽元件的載子傳輸機制，並對提升載子遷移率的元件設計提供洞見。在工作項目三中，著眼於未來可使用鍺作為通道材料以進一步提升元件效能，並採用超薄層(ultra-thin body)結構改善鍺元件的靜電特性，本研究發展解析理論模型，用以探討並比較量子侷限效應對於極微縮超薄層鍺及矽通道元件的通道長度變異敏感度的影響。我們的元件模型也將有助於未來超薄層電晶體的設計。

關鍵詞：
應變矽，超薄層電晶體，量子侷限，匹配，變異性，表面粗糙散射遷移率

Abstract

This project conducts a comprehensive study of variability and carrier transport for advanced silicon-based nanodevices. In task I, we investigate the impact of uniaxial strain on the temperature dependence of mismatching properties of nanoscale MOSFETs. This study is important not only for circuit designs using advanced strained-silicon technologies, but also for the fundamental understanding of intrinsic parameter fluctuations in CMOS devices. In task II, we provide an experimental assessment of surface-roughness limited mobility under uniaxial strain through cryogenic temperature measurements. This study has facilitated the understanding of carrier transport in strained-silicon, and provided insights in device designs for future mobility scaling. In task III, we report the impact of quantum confinement on the short-channel effect (SCE) and threshold-voltage sensitivity to channel-length variation for ultra-thin-body (UTB) GeOI and SOI MOSFETs using a derived analytical solution of Schrödinger equation. Our theoretical study indicates that, due to the discrepancy in effective mass, the impact of quantum confinement must be considered when one-to-one comparisons between UTB GeOI and SOI MOSFETs regarding the SCE are made.

Keywords :
Strained silicon, ultra-thin-body transistor, quantum confinement, mismatch, variability, surface-roughness limited mobility

二、計畫目的及研究方法

This project aimed to conduct a comprehensive study of variability and carrier transport for advanced silicon-based nanodevices [1]. This report details the following three major tasks carried out during the project:

Task I: Temperature dependence of drain current mismatch in nanoscale uniaxial-strained MOSFETs [2]

Task II: Experimental investigation of surface-roughness limited mobility in uniaxial strained MOSFETs [3]

Task III: Impact of quantum confinement on the threshold-voltage roll-off of ultra-thin-body GeOI and SOI MOSFETs [4]

Task I

Device mismatch and its temperature dependence are becoming increasingly important because they may limit the achievable accuracy in analog applications and mixed-mode integrated circuits [5]-[7]. Regarding the temperature dependence of MOSFET mismatching properties, Andricciola *et al.* [6] have shown that as temperature decreases, both the threshold voltage mismatch ($\sigma\Delta V_{th}$) and the normalized current factor mismatch ($\sigma(\Delta\beta)/\beta$) increase. In addition, Mennillo *et al.* [7] have suggested that the enhanced current factor mismatch as temperature decreases can be attributed to the increased Coulombic scattering. As strained-silicon is widely used in state-of-the-art CMOS technologies [8]-[10], however, the impact of strain on the temperature dependence of mismatching properties for nanoscale transistors is rarely known and merits investigation.

In this work, we examine the drain current mismatch of uniaxially-strained pMOSFETs under various temperatures and report our findings on the intrinsic effect of uniaxial strain.

Task II

Strain technology has been considered as a key process knob for advanced CMOS technologies [11]. It is known that strain can improve phonon-scattering limited mobility (μ_{PH}) by reducing intervalley phonon scatterings and effective conduction mass [12]. Whether strain can improve the surface-roughness limited mobility (μ_{SR}) is still not clear and demands more experimental investigations. Recently, the biaxial strain dependence of μ_{SR} has been examined by Bonno *et al.* [13] and Zhao *et al.* [14]. These studies have shown that μ_{SR} has strong strain sensitivity for both NFETs and PFETs due to surface morphology engineering with biaxial strain. The temperature dependences of hole mobility by mechanical uniaxial strain [15] and process-induced uniaxial strain [16] have also been studied experimentally. However, the temperature range was higher than 87 K, and the phonon scattering mechanism was not fully suppressed. To investigate the uniaxial strain dependence of surface roughness mobility, it is necessary to extract mobility with temperature down to 20 K to suppress the phonon scattering mechanism.

In this work, we report our new findings on the impact of process-induced uniaxial strain on the μ_{SR} of short-channel pMOSFETs with temperature down to 20 K.

Task III

Germanium as a channel material has been proposed to enable the mobility scaling for CMOS devices. As the higher permittivity makes Ge more susceptible to short-channel effects (SCEs), ultra-thin-body (UTB) Ge-on-Insulator (GeOI) structure with thin buried oxide (BOX) has been suggested to improve the electrostatic integrity [17][18]. With the scaling of channel thickness, the quantum-confinement effect may become significant and impact the SCE of scaled UTB devices. Using density gradient model [19], Omura *et al.* [20] have observed increased threshold voltage (V_{th}) roll-off due to quantum confinement in UTB Si-on-insulator (SOI) devices. Whether there exists any difference between GeOI and SOI devices regarding the impact of quantum confinement on SCEs is not clearly known and merits investigation.

In this work, we tackle the problem using an analytically derived solution of Schrödinger equation verified with TCAD simulation. We report our new findings for UTB GeOI MOSFETs with thin BOX. The theoretical model provides us a physical and efficient method to explore the impact of quantum-confinement effect.

三、結果與討論

1. Temperature Dependence of Drain Current Mismatch in Nanoscale Uniaxial-Strained MOSFETs [2]

This work investigates the drain current mismatch of uniaxially-strained pMOSFETs under various temperatures. Fig. 1 shows the Pelgrom plot of $\sigma\Delta V_{th}$ under various temperatures for the strained and unstrained devices. The geometries of the devices are W/L_{gate}=1μm/54nm, 0.3μm/54nm, and 0.15μm/54nm. Note that the L_{gate} for strained devices needs to be the same in order to keep similar strain in the channel because the channel strain is gate-length dependent in process-induced strain silicon devices [10]. The linear relationship between $\sigma\Delta V_{th}$ and $(WL_{gate})^{-1/2}$ indicates a random-dopant-fluctuations origin $\sigma\Delta V_{th}$ [24]. In addition, the strained device shows similar temperature dependence of $\sigma\Delta V_{th}$ as compared with its control counterpart. Since the $\sigma(\Delta I_d)/I_d$ in the low $|V_{gst}|$ regime is mainly determined by the $\sigma\Delta V_{th}$ [22], the similar temperature dependence of $\sigma\Delta V_{th}$ results in similar temperature dependence of $\sigma(\Delta I_d)/I_d$ for the strained and unstrained devices as shown in Fig. 2.

In the high $|V_{gst}|$ regime, however, the strained device shows different temperature dependence of $\sigma(\Delta I_d)/I_d$ as compared with its control counterpart. It can be seen from Fig. 3 that in the high $|V_{gst}|$ linear regime the $\sigma(\Delta I_d)/I_d$ increases with decreasing temperature for both the strained and unstrained devices. The temperature dependence of $\sigma(\Delta I_d)/I_d$ in Fig. 3 can be explained by the temperature dependence of $\sigma(\Delta\beta)/\beta$, as shown in Fig. 4. The increased $\sigma(\Delta\beta)/\beta$ with decreasing temperature has been attributed to the Coulombic scattering [6][7]. However, it should be noted that the $\sigma(\Delta I_d)/I_d$ of the strained device in Fig. 3 exhibits smaller temperature dependence than that of the unstrained one. The smaller temperature dependence of $\sigma(\Delta I_d)/I_d$ for strained devices results from the smaller temperature dependence in $\sigma(\Delta\beta)/\beta$ (Fig. 4). It is the significantly enhanced β for the strained device as temperature decreases that reduces the temperature sensitivity of $\sigma(\Delta\beta)/\beta$ and $\sigma(\Delta I_d)/I_d$ for the strained device. The larger temperature sensitivity of β present in the compressively-strained PFET results from the larger temperature sensitivity of carrier mobility, as reported in [16].

Fig. 5 compares the temperature dependence of $\sigma(\Delta I_d)/I_d$ for the strained and unstrained devices in the high $|V_{gst}|$ saturation regime. It can be seen that the temperature dependence of $\sigma(\Delta I_d)/I_d$ for the strained device is opposite to that of the unstrained one. In other words, the compressive strain has changed the temperature trend in drain current mismatch and the $\sigma(\Delta I_d)/I_d$ decreases with temperature for the strained PFET. In the high $|V_{gst}|$ saturation regime, both the threshold voltage mismatch and current factor mismatch are relevant to the $\sigma(\Delta I_d)/I_d$ [22]. The decreased $\sigma(\Delta I_d)/I_d$ for the strained device results from the larger reduction in g_m/I_d reduction as temperature decreases (Fig. 6), while the $\sigma(\Delta I_d)/I_d$ of the unstrained device is weakly dependent on temperature because of the opposite temperature dependence of $\sigma\Delta V_{th}$ (Fig. 1) and g_m/I_d (Fig. 6). The larger reduction in g_m/I_d as temperature decreases for the strained device is also a consequence of the larger temperature sensitivity of carrier mobility [16].

In summary, we have investigated and analyzed the device mismatching properties of nanoscale uniaxial strained pMOSFETs under various temperatures. Our result indicates that the drain current mismatch versus temperature trend for the strained device is different from the unstrained one. In the high $|V_{gst}|$ linear regime, the compressively-strained device shows smaller increment in drain current mismatch than the unstrained counterpart as temperature decreases. In the high $|V_{gst}|$

saturation region, opposite to the unstrained case, the drain current mismatch of the compressively-strained device decreases with temperature. The underlying mechanism is the larger temperature sensitivity of carrier mobility for the strained device.

2. Experimental Investigation of Surface-Roughness Limited Mobility in Uniaxial Strained MOSFETs [3]

This work investigates the impact of process-induced uniaxial strain on the surface-roughness limited mobility, μ_{SR}, of short-channel pMOSFETs. Fig. 7 shows the measured carrier mobility versus vertical electric field (E_{EFF}) with various temperatures. It can be seen that, under high E_{EFF}, the mobility tends to increase as the temperature decreases due to suppressed phonon scattering. At a temperature lower than 60 K, the mobility at high E_{EFF} saturates because the phonon scattering mechanism is fully suppressed. In other words, the mobility at high E_{EFF} within this temperature range can be viewed as the surface-roughness limited mobility.

Fig. 8 shows the extracted carrier mobility versus temperature at E_{EFF} = 1.6 MV/cm for various stressors. It can be seen that the compressive uniaxial strain results in a significant mobility enhancement due to band engineering and carrier repopulations [10]. In addition, μ_{SR} dominates the total mobility for temperature < 60 K for all kinds of stressors.

Fig. 9 shows the mobility enhancement percentage ($\Delta\mu/\mu$) versus temperature with compressive and tensile stressors. As the temperature decreases, it can be observed that the mobility enhancement increases and saturates at temperature < 60 K where surface roughness scattering dominates. It indicates that μ_{SR} has stronger stress sensitivity than the phonon-scattering limited mobility, μ_{PH}. Furthermore, the μ_{SR} enhancement tends to saturate and shows little sensitivity to temperature.

It is worth noting that our experimental results are consistent with the reported results by simulations [15][25][26]. Specifically, it was reported in [25] that the scattering rate with interfacial roughness can be reduced by smoother interfaces in biaxial strained NFETs. In addition, the atomic scale model in [26] also indicated weaker surface scattering potential in strained Si due to the nature of primitive defects. For the uniaxially strained PFET case, it is plausible that the lighter effective conduction mass [5] induced by compressive strain may result in the μ_{SR} enhancement.

Fig. 10 shows the extracted carrier mobility versus effective vertical electric field (E_{EFF}) for neutral and compressive stressors at 20 K. Within this temperature range, both the Coulomb scattering and surface roughness scattering mechanisms are crucial in the determination of the overall carrier mobility. It can be seen that the mobility is dominated by the surface roughness scattering mechanism for E_{EFF} higher than 1.2 MV/cm. The inset of Fig. 10 shows that the μ_{SR} enhancement increases with E_{EFF} in the high-E_{EFF} regime where the carrier mobility is dominated by surface roughness scatterings.

In summary, by accurate split *C–V* mobility extraction, the strain dependence of μ_{SR} in short-channel pMOSFETs has been investigated under cryogenic temperatures. Our measured data indicate that μ_{SR} can be significantly enhanced by the uniaxial compressive strain. Furthermore, the μ_{SR} has higher strain dependence than the μ_{PH}. Our experimental results confirm the previously reported results based on simulations.

3. Impact of Quantum Confinement on the Threshold-Voltage Roll-Off of Ultra-Thin-Body GeOI and SOI MOSFETs [4]

This work investigates the impact of quantum confinement on the short-channel effect (SCE) and threshold-voltage sensitivity to channel-length variation for ultra-thin-body (UTB) GeOI and SOI MOSFETs using a

derived analytical solution of Schrödinger equation. Note that for long-channel undoped UTB devices, the conduction band edge $E_C(x)$ was usually treated as a triangular well [27]. However, to account for the source/drain coupling due to SCEs, the conduction band edge $E_C(x)$ should be treated as a parabolic well [28] with potential energy $E_C(x) = \alpha x^2 + \beta x + \gamma$ where α, β, and γ are channel-length-dependent coefficients and can be obtained from the channel potential solution of Poisson's equation under subthreshold region [29]. Using the parabolic-well treatment, the wavefunction can be expressed as $\Psi_j(x) = \sum d_n \cdot x^n$ where the coefficients d_n's can be determined by the recursive relationship [4].

The jth eigen-energy E_j can be determined by the boundary condition $\Psi_j(x=0) = \Psi_j(x=T_{ch}) = 0$ where $x=0$ and $x=T_{ch}$ (channel thickness) are defined as the interface positions of BOX/channel and channel/gate oxide, respectively. Thus, the eigen-energy and eigenfunction of short-channel UTB MOSFETs under subthreshold region can be derived. We have verified our model using the TCAD simulation that numerically solves the self-consistent solution of 2-D Poisson and 1-D Schrödinger equations [30]. Fig. 11(a) and (b) show that for both the triangular potential well of long-channel devices and the parabolic well (due to SCEs) of short-channel ones, the E_j's calculated by our model are fairly accurate. Note that a scalable quantum-confinement (QC) model with accurate channel length dependence is crucial to this work.

Using the calculated eigen-energies and wavefunctions, the electron density can be derived [4]. Fig. 12 shows that the peak of electron density calculated by the classical (CL) model is not located at the channel/BOX interface (x=0) because the use of thin BOX (10nm) instead of thick BOX suppresses the buried-insulator induced barrier lowering (BIIBL) [20]. Although the peak of electron density calculated by the QC model is shifted toward the channel center, the main current flow paths predicted by both models are quite similar for the UTB structure with thin BOX.

To assess the impact of quantum confinement on V_{th}, the V_{th} is defined as the V_{GS} at which the average electron density of the cross-section at $y = L_{eff}/2$ (highest potential barrier for low V_{DS}) exceeds the channel doping concentration. Fig. 13 shows that for GeOI MOSFETs with channel thickness (T_{ch}) = 10nm, the V_{th} roll-off (defined as $V_{th}(L) - V_{th}(L=100nm)$) predicted by the QC model is larger than that predicted by the CL model. This is consistent with the result reported for SOI MOSFET [20], and can be explained as follows. The V_{th} shift due to the QC effect can be expressed as $\Delta V_{th}^{QM} \cong S/(\ln 10 \cdot kT/q) \cdot \Delta\psi_s^{QM}$ with S being the subthreshold swing and $\Delta\psi_s^{QM}$ being the equivalent surface potential shift due to the QC effect. The inset of Fig. 13 shows that for GeOI devices with larger T_{ch} (10nm), the "electrical confinement" [27] dominates the carrier quantization. The E_0 (ground-state eigen-energy) of the triangular well (for long-channel devices) is much larger than that of the parabolic well (for short-channel devices) because of the larger electric field in the triangular one. As $\Delta\psi_s^{QM}$ is mainly determined by E_0, the $\Delta\psi_s^{QM}$ and thus ΔV_{th}^{QM} for the long-channel device is larger than that of the short-channel one. Therefore, the V_{th} roll-off considering the QC effect is larger in Fig. 13.

As the T_{ch} scales down, however, a different trend can be observed. Fig. 14 shows that for GeOI MOSFETs with T_{ch} = 5nm, the V_{th} roll-off predicted by the QC model becomes smaller than that predicted by the CL model, which is opposite to the larger T_{ch} case. This can not be explained by the reduction of BIIBL due to the QC effect [20] because in this study, thin BOX (T_{BOX} = 10nm) is used and the impact of BIIBL is not significant (see Fig. 12). Since the "structural confinement" [27] dominates the carrier quantization for GeOI devices with smaller T_{ch} (5nm), the inset of Fig. 14 shows that the E_0 (and hence $\Delta\psi_s^{QM}$)

of the long-channel device is close to that of the short-channel one. Nevertheless, due to the SCE, the subthreshold swing S of the short-channel device is larger than the long-channel one. Therefore, the ΔV_{th}^{QM} of the short-channel device is larger than that of the long-channel device and the V_{th} roll-off considering the QC effect is smaller. This mechanism is important because it may alter the comparison result for V_{th} roll-off between SOI and GeOI devices. Fig. 15 shows that, contrary to the prediction by the CL model, the V_{th} roll-off for GeOI devices with smaller T_{ch} can be smaller than that of the SOI counterparts as the QC effect is considered.

In summary, depending on T_{ch}, the quantum-confinement effect may increase or decrease the SCE of UTB devices. The critical channel thickness ($T_{ch,crit}$) determining whether the QC effect increases or decreases the V_{th} roll-off depends on the BOX thickness (T_{BOX}) and the channel material. Fig. 16 shows that the $T_{ch,crit}$ of GeOI MOSFETs increases with T_{BOX}. In addition, for a given T_{BOX}, the $T_{ch,crit}$ of SOI MOSFETs is smaller than that of the GeOI MOSFETs. This may explain why the suppression of V_{th} roll-off by the QC effect was not observed for the UTB SOI devices (with T_{ch} = 10nm) in [20].

四、計畫成果自評

In this project we have conducted a comprehensive study of variability and carrier transport for advanced silicon-based devices. We have investigated the impact of uniaxial strain on the temperature dependence of mismatching properties of nanoscale MOSFETs. This study is important not only for circuit designs using advanced strained-silicon technologies, but also for the fundamental understanding of intrinsic parameter fluctuations in CMOS devices. In addition, we have experimentally examined the impact of uniaxial strain on the surface-roughness limited mobility using cryogenic temperature measurements. This study has facilitated the understanding of carrier transport in strained-silicon, and provided insights in device designs for future mobility scaling. Besides, we have investigated the impact of quantum confinement on the short-channel effect for UTB GeOI and SOI MOSFETs using derived analytical solution of Schrödinger equation. Our theoretical study indicates that, due to the discrepancy in effective mass, the impact of quantum confinement must be considered when one-to-one comparisons between UTB GeOI and SOI MOSFETs regarding the short-channel effect and variability are made.

These research works have been crucial to the education of our graduate students to become leading researchers in silicon-based nanoelectronics. Finally, it is worth mentioning that our recent work [31] (also supported by this NSC project) regarding the impact of self-heating on random mismatch has been accepted and will be presented at 2011 IEDM, the world preeminent forum for reporting technological breakthroughs in the areas of semiconductor and electronic device technology, design, physics, and modeling.

五、參考文獻

[1] International Technology Roadmap for Semiconductors (http://www.itrs.net).

[2] J. J.-Y. Kuo, W. P.-N. Chen, and P. Su, "Temperature Dependence of Drain Current Mismatch in Nanoscale Uniaxial-Strained PMOSFETs," *IEEE Electron Device Lett.*, vol. 32, no. 3, pp. 240-242, March 2011.

[3] W. P.-N. Chen, J. J.-Y. Kuo, and P. Su, "Experimental Investigation of Surface Roughness Limited Mobility in Uniaxial Strained pMOSFETs," *IEEE Electron Device Lett.*, vol.32, no.2, pp.113-115, Feb. 2011.

[4] Y.-S. Wu, H.-Y. Hsieh, V. P.-H. Hu, and P. Su, "Impact of Quantum Confinement on Short-Channel Effects for Ultra-Thin-Body Germanium-On-Insulator MOSFETs," *IEEE Electron Device Lett.*, vol. 32, no. 1, pp. 18-20, January 2011.

[5] A. Bhavnagarwala, S. Kosonocky, C. Radens, K. Stawiasz, R. Mann, Q. Ye, and K. Chin, "Fluctuation limits & scaling opportunities for CMOS SRAM Cells," *IEDM Tech. Dig.*, Dec. 2005, pp. 659–662.

[6] P. Andricciola and H. P. Tuinhout, "The Temperature Dependence of Mismatch in Deep-Submicrometer Bulk MOSFETs," *IEEE Electron Device Lett.*, vol. 30, no. 6, pp. 690–692, June 2009.
[7] S. Mennillo, A. Spessot, L. Vendrame, L. Bortesi, "An Analysis of Temperature Impact on MOSFET Mismatch," *Proc. ICMTS* 2009, pp. 56–61.
[8] C. Hu, "Device Challenges and Opportunities," *VLSI Symp. Tech. Dig.*, June 2004, pp.4-5.
[9] Y. Tateshita *et al.*, "High-Performance and Low-Power CMOS Device Technologies Featuring Metal/High-k Gate Stacks with Uniaxial Strained Silicon Channels on (100) and (110) Substrates," *IEDM Tech. Dig.*, Dec. 2006. pp. 63-66.
[10] S.E. Thompson *et al.*, "A 90-nm logic technology featuring strained-silicon," *IEEE Trans. Electron Devices*, vol. 53, no. 5, p. 1010, May 2006.
[11] Z. Luo *et al.*, "High performance transistors featured in an aggressively scaled 45 nm bulk CMOS technology," in *VLSI Symp. Tech. Dig.*, June 2007, pp. 16–17.
[12] S. E. Thompson, G. Sun, Y. S. Choi, and T. Nishida, "Uniaxial process-induced strained-Si: Extending the CMOS roadmap," *IEEE Trans. Electron Devices*, vol. 53, no. 5, pp. 1010–1020, 2006.
[13] Bonno *et al.*, "High-field electron mobility in biaxially-tensile strained SOI: Low temperature measurement and correlation with the surface morphology," in *VLSI Symp. Tech. Dig.*, June 2007, pp. 134–135.
[14] Y. Zhao *et al.*, "A novel characterization scheme of Si/SiO2 interface roughness for surface roughness scattering-limited mobilities of electrons and holes in unstrained- and strained-Si MOSFETs," *IEEE Trans. Electron Devices*, vol. 57, no. 9, pp. 2057–2066, Sep. 2010.
[15] X. Yang *et al.*, "Temperature dependence of enhanced hole mobility in uniaxial strained p-channel metal–oxide–semiconductor field-effect transistors and insight into the physical mechanisms," *Appl. Phys. Lett.*, vol. 93, no. 24, p. 243 503, Dec. 2008.
[16] W. P.-N. Chen, J. J.-Y. Kuo, and P. Su, "Impact of process-induced uniaxial strain on the temperature dependence of carrier mobility in nanoscale pMOSFETs," *IEEE Electron Device Lett.*, vol. 31, no. 5, pp. 414–416, May 2010.
[17] E. Pop, C. O. Chui, S. Sinha, R. Dutton, and K. Goodson, "Electro- thermal comparison and performance optimization of thin-body SOI and GOI MOSFETs," in *IEDM Tech. Dig.*, pp. 411-414, 2004.
[18] S. W. Bedell, A. Majumdar, J. A. Ott, J. Arnold, K. Fogel, S. J. Koester, and D. K. Sadana, "Mobility Scaling in Short-Channel Length Strained Ge-on-Insulator P-MOSFETs," *IEEE Electron Device Letters*, Vol. 29, No. 7, pp. 811-813, July 2008.
[19] A. Wettstein, A. Schenk, and W. Fichtner, "Quantum device simulation with the density-gradient model on unstructured grids," *IEEE Trans. Electron Devices*, Vol. 48, No. 2, pp. 279-284, Feb. 2001.
[20] Y. Omura, H. Konish, and S. Sato, "Quantum-Mechanical Suppression and Enhancement of SCEs in Ultrathin SOI MOSFETs," *IEEE Trans. Electron Devices*, Vol. 53, No. 4, pp. 677-684, April 2006.
[21] J. J.-Y. Kuo, W. P.-N. Chen, and P. Su, "A Comprehensive Investigation of Analog Performance for Uniaxial Strained PMOSFETs," *IEEE Trans. Electron Devices*, vol. 56, no. 2, pp. 284-290, Feb. 2009.
[22] J. J.-Y. Kuo, W. P.-N. Chen, and P. Su, "Investigation and Analysis of Mismatching Properties for Nanoscale Strained MOSFETs," *IEEE Trans. Nanotechnology*, vol. 9, no. 2, pp. 248-253, Mar. 2010.
[23] J.A. Croon, M. Rosmeulen, S. Decoutere, W. Sansen, H.E. Maes, "An easy-to-use mismatch model for the MOS transistor," *IEEE J. Solid-State Circuits*, vol. 37, no. 8, pp.1056, Aug. 2002.
[24] T. Mizuno, J. Okamura, and A. Toriumi," Experimental Study of Threshold Voltage Fluctuation Due to Statistical Variation of Channel Dopant Number in MOSFET's " *IEEE Trans. Electron Devices*, pp.2216, Nov. 1994.
[25] M. V. Fischetti, F. Gamiz, and W. Hansch, "On the enhanced electron mobility in strained-silicon inversion layers," *J. Appl. Phys.*, vol. 92, no. 12, pp. 7320–7324, Dec. 2002.
[26] S. T. Pantelides, L. Tsetseris, M. J. Beck, S. N. Rashkeev, G. Hadjisavvas, I. G. Batyrev, B. R. Tuttle, A. G. Marinopoulos, X. J. Zhou, D. M. Fleetwood, and R. D. Schrimpf, "Performance, reliability, radiation effects, and aging issues in microelectronics—From atomicscale physics to engineering-level modeling," in *Proc. ESSDERC*, Sep. 2009, pp. 48–55.
[27] V. P. Trivedi and J. G. Fossum, "Quantum-Mechanical Effects on the Threshold Voltage of Undoped Double-Gate MOSFETs," *IEEE Electron Device Letters*, Vol. 26, No. 8, pp. 579-582, Aug. 2005.
[28] Y.-S. Wu and P. Su, "Analytical Quantum-Confinement Model for Short-Channel Gate-All-Around MOSFETs Under Subthreshold Region," *IEEE Trans. Electron Devices*, Vol. 56, No. 11, pp. 2720-2725, Nov. 2009.
[29] V. P.-H. Hu, Y.-S. Wu, and P. Su, "Investigation of Electrostatic Integrity for Ultra-Thin-Body Germanium-On-Nothing (GeON) MOSFET," *IEEE Trans. Nanotechnology*, Vol. 10, No. 2, pp. 325-330, March 2011.
[30] *ATLAS User's Manual*, SILVACO, Santa Clara, CA, 2008.
[31] J. J.-Y. Kuo and P. Su, "Self-Heating Induced Feedback Effect on Drain Current Mismatch and Its Modeling," *2011 International Electron Devices Meeting (IEDM)*, Washington DC, USA, Dec. 2011.

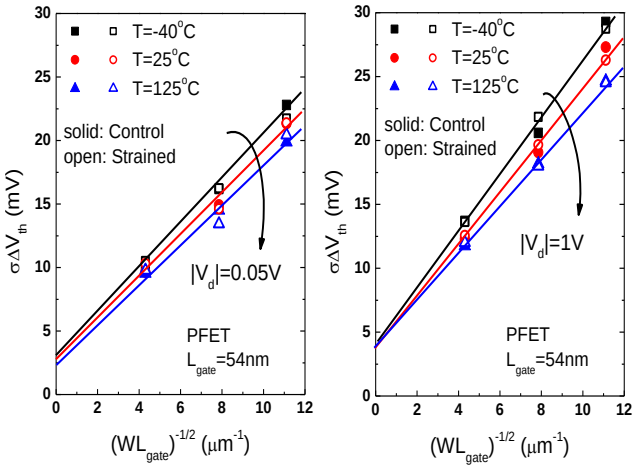

Fig. 1 The strained device shows similar temperature dependence of $\sigma(\Delta V_{th})$ as that of the control device at (a) $|V_d|$=0.05V, and (b) $|V_d|$=1V.

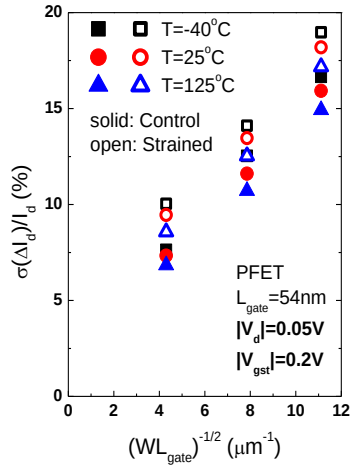

Fig. 2 The strained device shows similar temperature dependence of $\sigma(\Delta I_d)/I_d$ as that of the control device at $|V_{gst}|$=0.2V and $|V_d|$=0.05V.

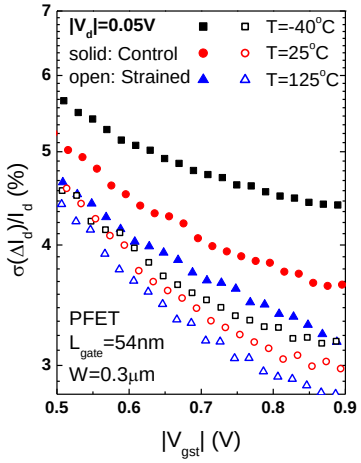

Fig. 3 The strained device shows smaller temperature dependence as compared with the unstrained one in the $|V_{gst}|$ regime with $|V_d|$=0.05V.

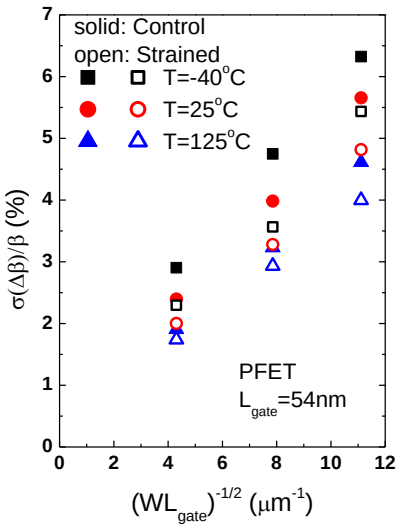

Fig. 4 Pelgrom plot of $\sigma(\Delta\beta)/\beta$ showing smaller temperature dependence of $\sigma(\Delta\beta)/\beta$ for the strained device.

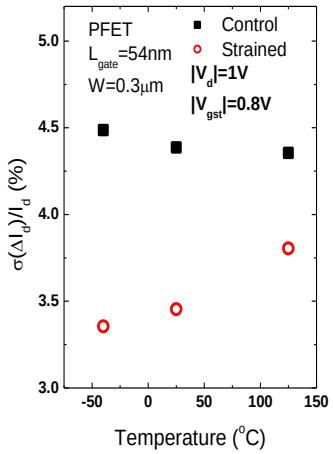

Fig. 5 $\sigma(\Delta I_d)/I_d$ vs. temperature characteristics showing reduced $\sigma(\Delta I_d)/I_d$ for the strained device as temperature decreases.

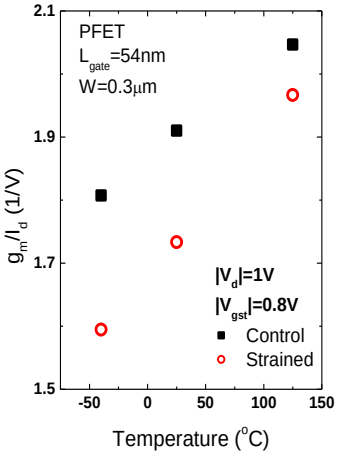

Fig. 6 The strained device shows larger reduction in g_m/I_d as temperature decreases.

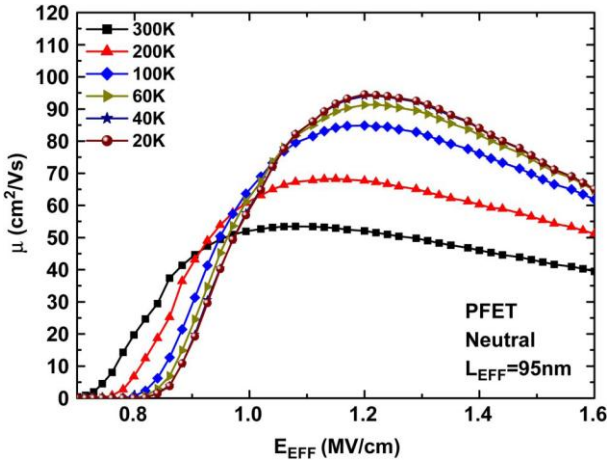

Fig. 7 Extracted carrier mobility versus vertical electric field under various temperatures.

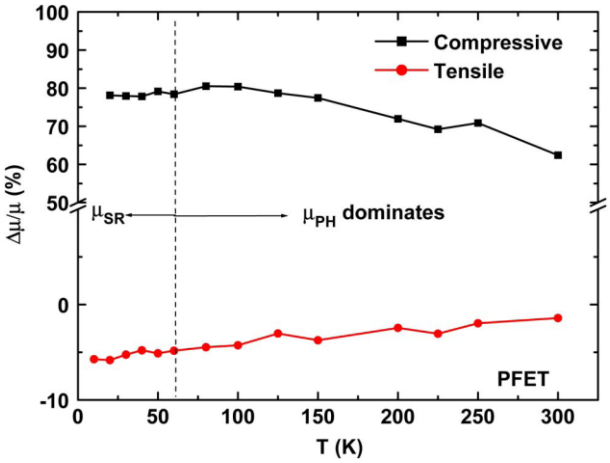

Fig. 9 Mobility enhancement percentage ($\Delta\mu/\mu$) versus temperature with compressive and tensile stressors.

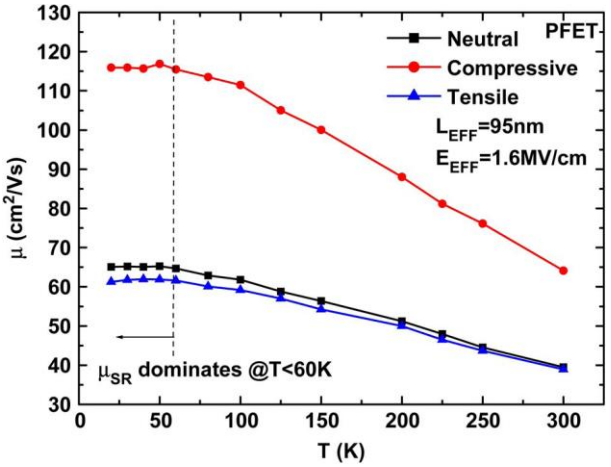

Fig. 8 Extracted carrier mobility at E_{EFF}= 1.6 MV/cm with various stressors. μ_{SR} dominates the total mobility for temperature < 60 K.

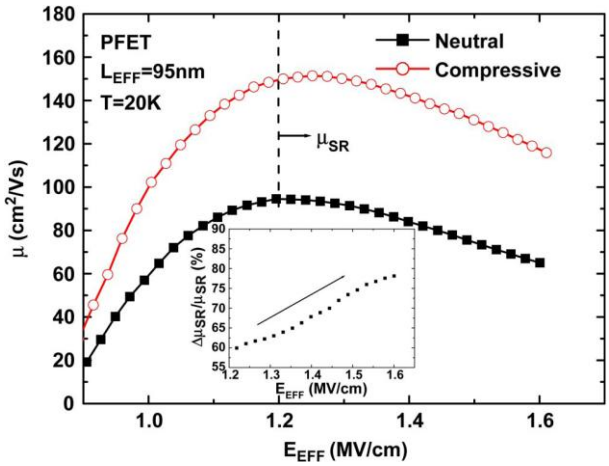

Fig. 10 Extracted carrier mobility versus vertical electric field at 20 K for the neutral and compressive stressors. (Inset) Surface roughness mobility enhancement increases as E_{EFF} increases.

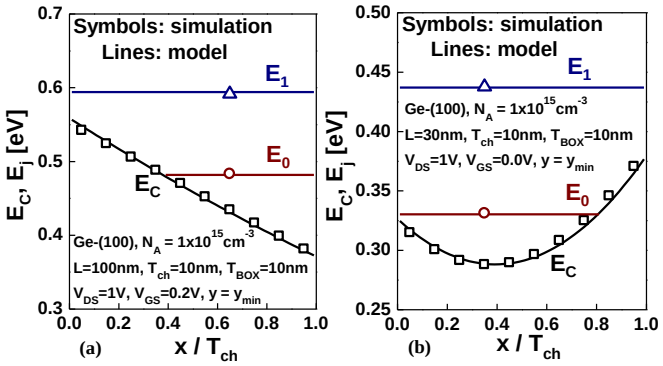

Fig. 11 Conduction band edge and quantized eigen-energies of lightly doped GeOI MOSFETs. (a) A long-channel device with triangular well. (b) A short-channel device with parabolic well.

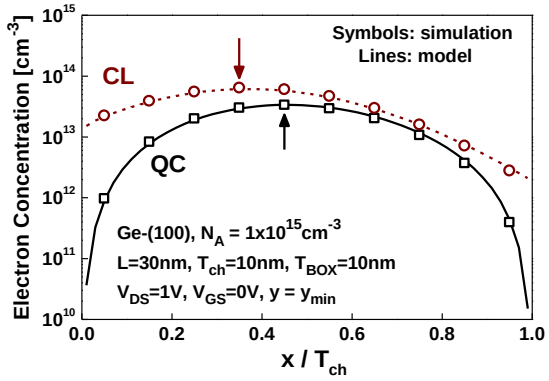

Fig. 12 Comparison of the electron density distribution with and without considering quantum-confinement (QC) effect. The electron density is calculated from 2-D density-of-states, eigen-energies, and wavefunctions.

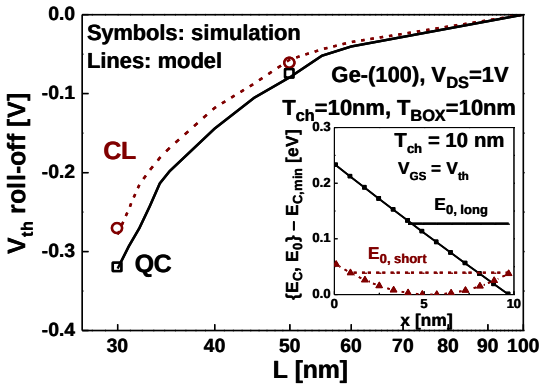

Fig. 13 Comparison of the V_{th} roll-off between QC and CL models for T_{ch} = 10nm. The inset indicates that for GeOI MOSFETs with larger T_{ch}, the difference in E_0 for long-channel ($E_{0,long}$) and short-channel ($E_{0,short}$) devices is significant due to electrical confinement.

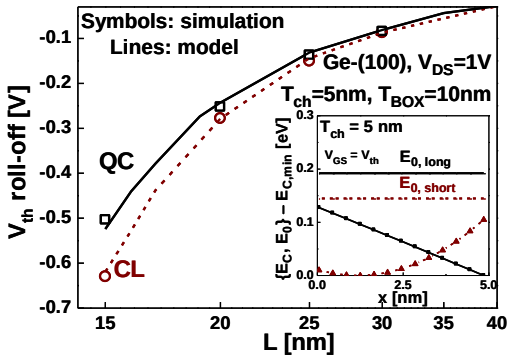

Fig. 14 Comparison of the V_{th} roll-off between QC and CL models for T_{ch} = 5nm. The inset indicates that for GeOI MOSFETs with smaller T_{ch}, the difference in E_0 for long-channel ($E_{0,long}$) and short-channel ($E_{0,short}$) devices is small because the degree of structural confinement is similar.

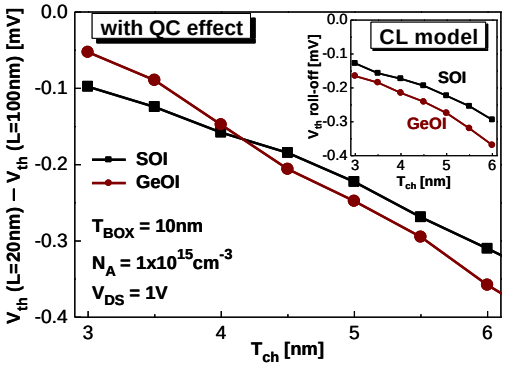

Fig. 15 V_{th} roll-off comparison between SOI and GeOI devices. As the QC effect is considered, a crossover near T_{ch} = 4nm can be seen.

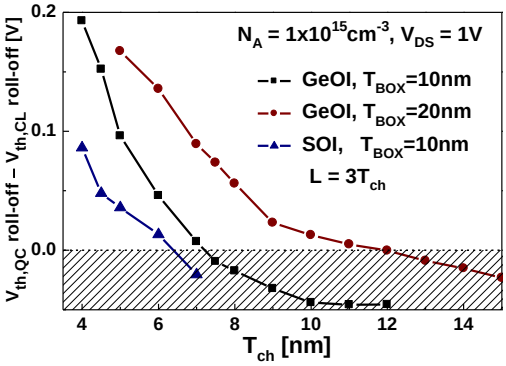

Fig. 16 The difference in V_{th} roll-off between the QC and CL models depends on T_{BOX} and channel material. The filled region denotes that the QC effect enhances the V_{th} roll-off, while the blank region denotes that the QC effect suppresses the V_{th} roll-off.

附件四

國科會補助專題研究計畫項下出席國際學術會議心得報告

日期：100年7月31日

計畫編號	NSC99－2221－E－009－174		
計畫名稱	前瞻矽奈米元件變異性及傳輸特性綜合研究(II)		
出國人員姓名	蘇彬	服務機構及職稱	國立交通大學電子工程學系教授
會議時間	100年6月12日至100年6月13日	會議地點	Kyoto, Japan
會議名稱	2011 Silicon Nanoelectronics Workshop		
發表論文題目	Detailed Study of "Dark Space" and Electrostatic Integrity for Ge MOSFETs with High-k Dielectric Using Analytical Solution of Schrodinger Equation		

一、參加會議經過

Silicon Nanoelectronics Workshop (SNW), supported by the Japan Society of Applied Physics and the IEEE Electron Device Society, is a major international workshop focusing on the area of silicon-based nanoelectronics that is closely related to VLSI technology. This year, the 2011 SNW was held in Kyoto from June 12th to June 13th. In spite of the catastrophic earthquake and tsunami just occurring in east Japan, the workshop still attracted many attendees in this year. The two-day program included 5 invited talks, 26 oral presentations, and numerous poster presentations. These presentations were scheduled in the following 8 sessions: *1. Plenary & SiGe/Ge Channel FETs, 2. Nanoscale FETs: Variability & RTS, 3. Nanoscale FETs: Nanowire FETs, 4. Graphene & More-than-Moore, 5. Posters, 6. Highly Doped Devices & Single-Electron/Dopant Phenomena, 7. MRAM & Nonvolatile Memory using Capacitance, and 8. RRAM.*

Our paper was scheduled in the first session, in which there were 5 oral presentations in

total. After the first talk (Plenary) by Intel's Dr. Robert Chau and the second talk by SEMATECH, the third and fourth talks were both from IMEC. Our presentation, the fifth one, was regarding the quantum-mechanical modeling of advanced Ge MOSFETs. Ge as channel material to improve the transport property of CMOS devices is one recent important topic in silicon-based nanoelectronics. Our work is crucial to predicting the electrostatic integrity as well as the random variability of advanced Ge devices. Our presentation went smoothly and received several constructive feedbacks from the audience.

二、與會心得

Silicon Nanoelectronics Workshop is one decent international workshop that focuses more on in-depth understanding of nano-device physics. The audience has usually included quite a few leaders from industry and academia who will also attend the Symposium on VLSI Technology right after the SNW at the same location. I remember in Session 6 Dr. J.-P. Colinge, a pioneer in SOI, gave an invited talk regarding Junctionless Transistors. This new device structure has recently attracted much attention due to its several advantages over the conventional bulk MOSFET. After his presentation, however, Dr. T. Skotnicki from STMicroelectronics expressed his concerns regarding the random dopant fluctuation inherent to the junctionless transistor. Through their in-depth questions and answers I gained valuable insights and new thoughts to this new device.

Right after the SNW at the same location, I also attended the 2011 Symposium on VLSI Technolgy from June 14th to June 16th. The VLSI Symposium has been recognized as one of the premiere forums showcasing the latest breakthroughs in semiconductor technologies. One recent trend we can observe from the conference is the growing importance of the device/circuit interaction and co-optimization in nanoscale CMOS. For example, one "Focus Session" newly added in this year's VLSI Symposium - "Design Enablement" aimed to address how new device/process/material technologies will impact circuit designs (through design rules, device models, DFM, etc.). In addition, a two-day overlap

(joint session) between the Technology and Circuits Symposia also attempted to promote a closer interaction between device engineers and circuit designers for more innovative use (design) of advanced technologies.

三、建議

This new trend is expected to continue and can be further demonstrated by the fact that in 2011 IEDM a new subcommittee – Circuit and Device Interaction (CDI) has been formed. The related topics include device/circuit scaling issues, technology/circuit co-optimization, power/performance/area analysis, impact of emerging device structures on circuit design, and technology variability, etc. We believe this new area is crucial to the continuous flourishing of the semiconductor industry. Since this area is usually interdisciplinary in nature, here we would like to suggest our National Science Council provide more support and encouragement to the related NSC proposals in the future. Finally, we are grateful to our National Science Council for supporting this fruitful Kyoto trip. The insights we gained from the trip will be beneficial to our future research in silicon-based nanoelectronics.

四、攜回資料名稱及內容

2011 Silicon Nanoelectronics Workshop 論文集

2011 Symposium on VLSI Technology 論文集

2011 Symposia on VLSI Technology and Circuits 光碟

2011 VLSI Technology Short Course 光碟

論文被接受發表之E-mail通知

-----Original Message-----
From: snw2011@ssn.pe.titech.ac.jp [mailto:snw2011@ssn.pe.titech.ac.jp]
Sent: Wednesday, April 20, 2011 5:10 PMp
To: oison.ee93g@nctu.edu.tw
Subject: SNW2011 Decision Notificatione

Dear Yu-Sheng Wu,

We are pleased to inform you that your abstract entitled

"Detailed Study of ''Dark Space'' and Electrostatic Integrity for Ge MOSFETs with High-k Dielectric Using Analytical Solution of Schroedinger

Equation"

has been accepted for an oral presentation at SNW2011.

The time allotted for your presentation is 20 minutes including discussions. The program of the workshop will be uploaded on the workshop home page soon.

We are looking forward to seeing you in Kyoto.

Sincerely yours,

Ken Uchida, SNW2011 Program Chair

Detailed Study of "Dark Space" and Electrostatic Integrity for Ge MOSFETs with High-k Dielectric Using Analytical Solution of Schrödinger Equation

Yu-Sheng Wu and Pin Su
Department of Electronics Engineering & Institute of Electronics, National Chiao Tung University, Taiwan.
E-mail: pinsu@faculty.nctu.edu.tw

I. Introduction

As the high-k/metal-gate stack is introduced to continue the scaling of equivalent oxide thickness (EOT), high mobility channel materials such as Ge have been proposed to compensate for the mobility loss due to the high-k gate stack [1]. However, larger "dark space" is one major concern for Ge devices [2]. "Dark space" can be viewed as the distance from the interface to the centroid of the carrier layer (normalized with the permittivity ratio) [2]. This dark space is critical because it may significantly increase the overall electrical EOT (EOT_e) in the subthreshold region, and degrade the device electrostatic integrity. In this work, using derived analytical solution of the Schrödinger equation, we provide a detailed study of the dark space for Ge MOSFETs with high-k dielectric.

II. Analytical Solution of Schrödinger Equation

To give a quantitative model of the dark space, we have analytically derived the eigen-energies and eigen-functions of the carriers in the subthreshold region, under which a triangular well $V(x) = q \cdot F_S \cdot x$ [3] with F_S the surface electric field can be used. For high-k dielectric, the barrier height (ϕ_b) is relatively small and the eigen-functions are not zero at the dielectric/channel interface (x=0). Using the boundary conditions that the eigen-function as well as its first derivative divided by the carrier effective mass are continuous across the interface, Eqn. (1) can be derived with $Ai(x)$ and $Bi(x)$ representing Airy functions of the first and second kind, respectively. The eigen-energy E_j can be determined from (1). It can also be expressed as $\boldsymbol{E_j \approx E_j(\phi_b = \infty) - \Delta E_j}$ with $E_j(\phi_b = \infty)$ derived by Stern [3] and ΔE_j (Eqn. (2)) the eigen-energy reduction due to the wavefunction penetration (WP) into high-k dielectric.

Fig. 1 shows that the ground-state eigen-energies (E_0) increase with F_S. In addition, the discrepancy between our model and Stern's one (without WP) also increases with F_S, as indicated by (2). For a given F_S near the onset of threshold, Fig. 2 shows that the discrepancy between the two models increases as the dielectric barrier height decreases, and our model agrees well with the TCAD simulation that numerically solves coupled Poisson and Schrödinger equations [4]. Note that a steep-retrograde doping profile is used in the comparison. Fig. 3 further compares the profiles of the lowest two subband wavefunctions between models and exact solution. Fig. 4 infers that the size of the dark space can be reduced by the wavefunction-penetration effect.

III. Subthreshold Swing & Dark Space Modeling

The dark space degrades the subthreshold swing (SS): $SS \cong (kT/q) \cdot \ln(10) \cdot \{1 - dF_S/dV_G \cdot [(\varepsilon_{ch}/\varepsilon_{di})T_{di} + d(E_0/q)/dF_S]\}^{-1}$

Fig. 5(a) shows that for long-channel Ge NFETs, the SS of (100)-surface is larger than the (110) and (111) counterparts. Moreover, the impact of WP on the SS of (100)-surface is larger than the (110) and (111) counterparts due to the more significant quantum-confinement effect. Moreover, the reduction of SS for Si NFETs with (100) and (110) surfaces due to the WP effect is not as significant as the Ge counterparts. Fig. 5(b) shows that the the impact of wavefunction penetration on the SS increases for short-channel devices.

The reduced SS in Fig. 5 due to WP can be explained by the carrier centroid $X_0 = \int x \cdot \Psi_0^2(x)dx \,/\, \int \Psi_0^2(x)dx$ with $\Psi_0(x)$ being the ground-state wavefunction. The X_0 is equal to $2E_0/(3qF_S)$ if the wavefunction vanishes at the interface [3]. However, as the WP effect is considered, Fig. 6 shows that the X_0 calculated by $d(E_0/q)/dF_S$, which is a more accurate and general expression for X_0, becomes significantly smaller than that calculated by $2E_0/(3qF_S)$. With the accurate modeling of X_0 considering wavefunction penetration, Fig. 7 shows that the dark space ($=X_0/(\varepsilon_{ch}/\varepsilon_{ox})$) can be used to explain the surface-orientation dependence of SS in Fig. 5.

IV. Detailed Study of Dark Space

In addition to surface orientation, the dark space also depends on the material of high-k dielectric because of the different degree of wavefunction penetration. Fig. 8 shows that among the three gate dielectrics, HfO_2 possesses the smallest dark space. Since the substrate bias (V_{sub}) can modulate the surface field F_S (Fig. 6), the dark space decreases with reverse V_{sub} as shown in Fig. 9. Moreover, the relative importance of dark space in the overall EOT_e is increasing with the scaling of the EOT. Fig. 10 shows that for Ge NFET with EOT down scaled to 0.4nm, the dark space is ~60% of the overall EOT_e for (100) surface, and decreases to ~40% for (111) surface. For Ge-PFET, the relative importance of dark space in the overall EOT_e is between (100) and (111) surfaces for Ge-NFET.

V. Summary

We have conducted a detailed study of dark space and electrostatic integrity for high-k-dielectric Ge MOSFETs using derived analytical solution of the Schrödinger equation. Our study indicates that the dark space depends on surface orientation, and for Ge NFET, the dark space for (111) surface is smaller than the (100) and (110) counterparts. Because of the wavefunction-penetration effect, the Ge NFET with HfO_2 as gate dielectric possesses smaller dark space than the Si_3N_4 and Al_2O_3 counterparts. In addition, due to different quantization effective mass, the wavefunction-penetration effect has to be considered when one-to-one comparisons between Ge and Si devices regarding the dark space are made. The modulation of dark space by applying substrate bias is also discussed.

$$\left[Ai(-k_{ch}x_{ch})\cdot Bi'(-k_{di}x_{di}) - (m_{di}/m_{ch})(k_{ch}/k_{di})Bi(-k_{di}x_{di})\cdot Ai'(-k_{ch}x_{ch})\right]\cdot Ai\left(-k_{di}(x_{di}+T_{di})\right) = 0$$
$$k_{ch} = \left(\frac{2m_{ch}qF_S}{\hbar^2}\right)^{1/3},\quad x_{ch} = \frac{E_j}{qF_S},\quad k_{di} = \left(\frac{2m_{di}q(\varepsilon_{ch}/\varepsilon_{di})F_S}{\hbar^2}\right)^{1/3},\quad x_{di} = \frac{E_j - q\phi_b}{(\varepsilon_{ch}/\varepsilon_{di})qF_S} \qquad (1)$$

m_{ch} and m_{di} are effective mass in the channel and dielectric, respectively. ε_{ch} and ε_{di} are permittivity of the channel and dielectric, respectively. T_{di} is the dielectric thickness.

$$\Delta E_j = \frac{qF_S}{\left(\frac{2m_{di}}{\hbar^2}\right)^{1/2}\left[\left(\frac{m_{ch}}{m_{di}} - \frac{\varepsilon_{di}}{\varepsilon_{ch}}\right)\cdot\left(q\phi_b - E_j(\phi_b=\infty)\right)^{1/2} + \left(\frac{\varepsilon_{di}}{\varepsilon_{ch}}\right)\cdot\left(q\phi_b - E_j(\phi_b=\infty) - \frac{\varepsilon_{ch}}{\varepsilon_{di}}\cdot T_{di}\cdot qF_S\right)^{1/2}\right]},\ j = 0,1,2,... \qquad (2)$$

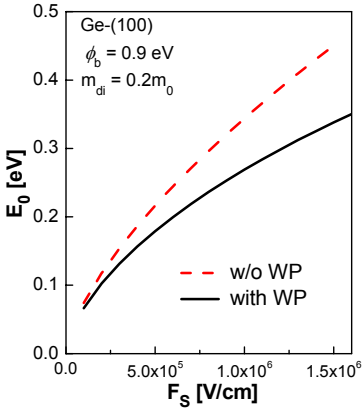

Fig. 1 Comparison of surface electric field dependences of E_0 for Ge-(100) surface calculated with and without wavefunction penetration.

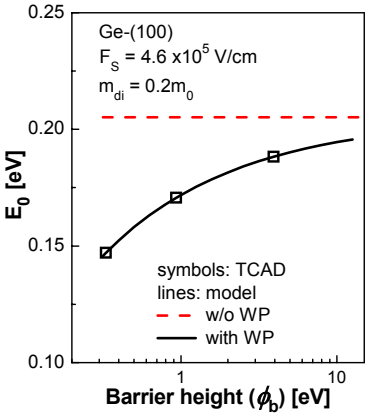

Fig. 2 Comparison of barrier height dependences of E_0 for Ge-(100) surface calculated with and without wavefunction penetration.

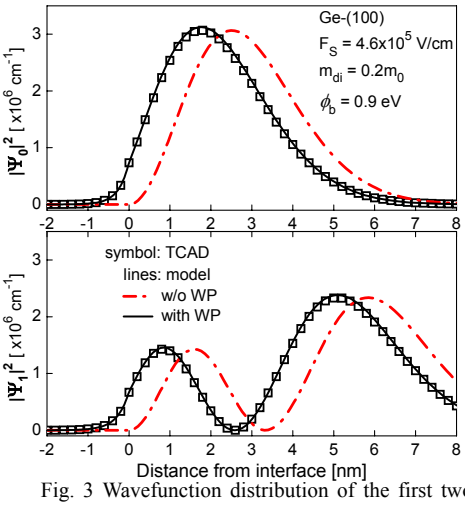

Fig. 3 Wavefunction distribution of the first two subbands for Ge-(100) surface with and without considering wavefunction penetration.

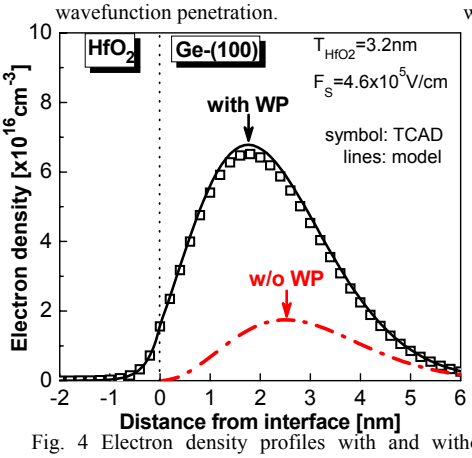

Fig. 4 Electron density profiles with and without considering wavefunction penetration. The ϕ_b and m_{di} used for HfO_2 in this study are 0.9eV and 0.2m_0 [5], respectively.

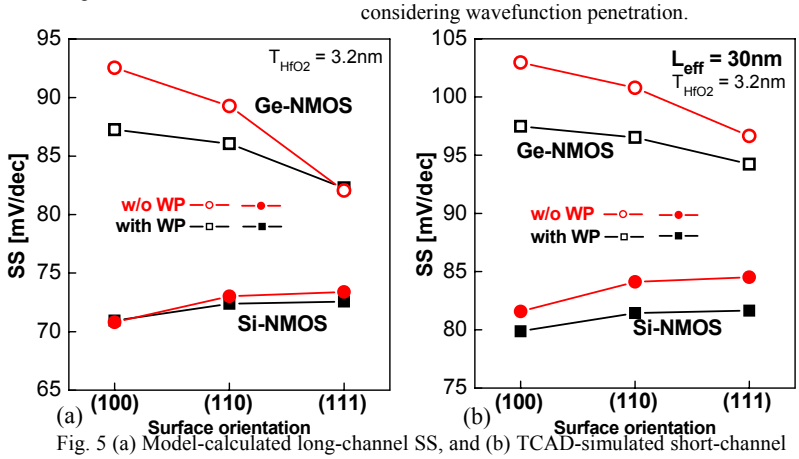

Fig. 5 (a) Model-calculated long-channel SS, and (b) TCAD-simulated short-channel SS for Ge-NFET and Si-NFET with various surface orientations.

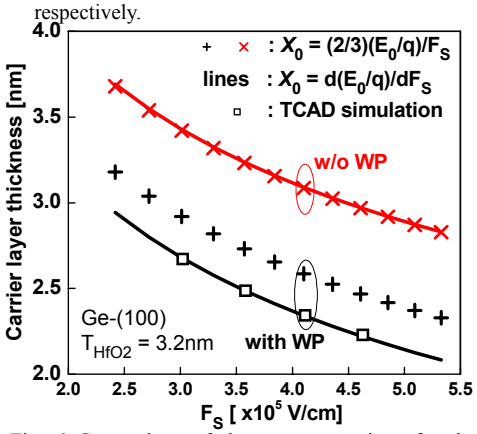

Fig. 6 Comparison of the two expressions for the carrier layer thickness (X_0). The X_0 from TCAD simulation is calculated by $\int x\cdot\Psi_0^2(x)dx/(\int\Psi_0^2(x)dx)$.

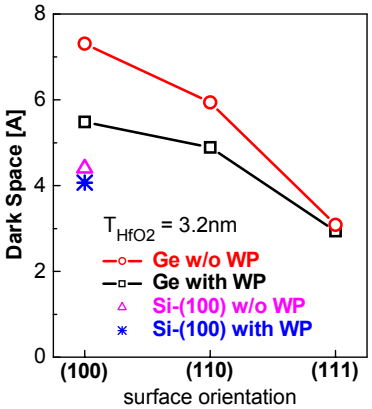

Fig. 7 Dark space of Ge-NFET depends on the surface orientation for a given surface field and dielectric material.

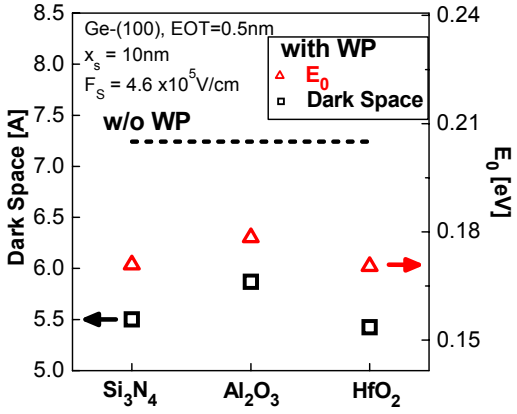

Fig. 8 Dark space and E_0 for Ge-(100) with various high-k dielectrics. The ϕ_b used for Si_3N_4 and Al_2O_3 in our calculation are 1.7eV and 2.6eV, respectively. The m_{di} used for Si_3N_4 and Al_2O_3 are 0.4m_0 and 0.35m_0, respectively [5].

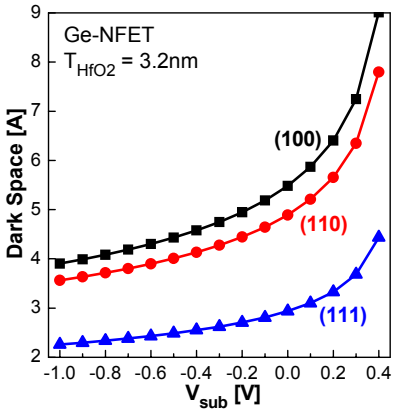

Fig. 9 Substrate bias dependences of dark space for Ge NFET with various surface orientations.

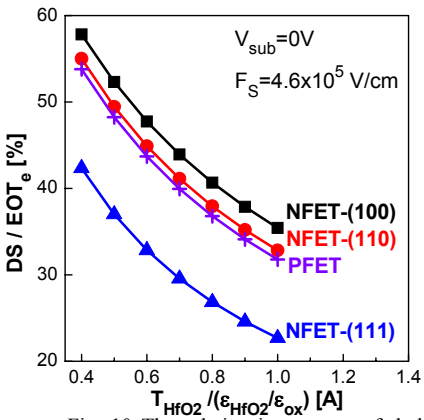

Fig. 10 The relative importance of dark space increases with the down scaling of EOT.

Acknowledgement

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References

[1] S. Takagi and M. Takenaka, VLSI Symp. 2010, p.147.
[2] T. Skotnicki and F. Boeuf, VLSI Symp. 2010, p.153.
[3] F. Stern, Phy. Rev. B, vol. 5, no. 12, p.4891, 1972.
[4] ATLAS User's Manual, SILVACO, 2008.
[5] Y.-C. Yeo et al., APL, vol. 81, no. 11, p. 2091, 2002.

國科會補助計畫衍生研發成果推廣資料表

日期:2011/10/25

國科會補助計畫	計畫名稱: 前瞻矽奈米元件變異性及傳輸特性綜合研究(II)
	計畫主持人: 蘇彬
	計畫編號: 99-2221-E-009-174- 學門領域: 固態電子

無研發成果推廣資料

99 年度專題研究計畫研究成果彙整表

計畫主持人：蘇彬	計畫編號：99-2221-E-009-174-
計畫名稱：前瞻矽奈米元件變異性及傳輸特性綜合研究(II)	

成果項目			量化			單位	備註（質化說明：如數個計畫共同成果、成果列為該期刊之封面故事...等）
			實際已達成數（被接受或已發表）	預期總達成數(含實際已達成數)	本計畫實際貢獻百分比		
國內	論文著作	期刊論文	0	0	100%	篇	
		研究報告/技術報告	0	0	100%		
		研討會論文	0	0	100%		
		專書	0	0	100%		
	專利	申請中件數	0	0	100%	件	
		已獲得件數	0	0	100%		
	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（本國籍）	碩士生	3	3	100%	人次	
		博士生	3	3	100%		
		博士後研究員	0	0	100%		
		專任助理	0	0	100%		
國外	論文著作	期刊論文	8	8	75%	篇	本計畫共支持八篇 IEEE 期刊論文發表（其中四篇為與其他的計畫共同成果).
		研究報告/技術報告	0	0	100%		
		研討會論文	8	8	100%		本計畫發表的國際研討會論文中有一篇為 IEDM (固態電子領域頂尖國際會議): J. Kuo and P. Su*, ' ' Self-Heating Induced Feedback Effect on Drain Current Mismatch and Its Modeling ' '

							USA, December 2011.
		專書	0	0	100%	章/本	
	專利	申請中件數	0	0	100%	件	
		已獲得件數	0	0	100%		
	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（外國籍）	碩士生	3	3	100%	人次	
		博士生	3	3	100%		
		博士後研究員	0	0	100%		
		專任助理	0	0	100%		

其他成果 (無法以量化表達之成果如辦理學術活動、獲得獎項、重要國際合作、研究成果國際影響力及其他協助產業技術發展之具體效益事項等，請以文字敘述填列。)	1.本計畫的其中一項研究成果今年入選深具國際影響力的 IEDM（固態電子領域頂尖國際會議): J. Kuo and P. Su*, ’’ Self-Heating Induced Feedback Effect on Drain Current Mismatch and Its Modeling, ’’ 2011 International Electron Devices Meeting (IEDM), Washington DC, USA, December 2011. 2.指導博士生胡璧合榮獲 2011 ICICDT（IEEE International Conference on IC Design and Technology）國際研討會最佳學生論文獎. 3.本計畫主持人國科會研究成果獲選刊登於國科會工程科技推展中心 101 年 2 月出刊的 123 期《工程科技通訊》以及《工程科技推展電子刊》.

	成果項目	量化	名稱或內容性質簡述
科教處計畫加填項目	測驗工具(含質性與量性)	0	
	課程/模組	0	
	電腦及網路系統或工具	0	
	教材	0	
	舉辦之活動/競賽	0	
	研討會/工作坊	0	
	電子報、網站	0	
	計畫成果推廣之參與（閱聽）人數	0	

國科會補助專題研究計畫成果報告自評表

請就研究內容與原計畫相符程度、達成預期目標情況、研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）、是否適合在學術期刊發表或申請專利、主要發現或其他有關價值等，作一綜合評估。

1. 請就研究內容與原計畫相符程度、達成預期目標情況作一綜合評估

■達成目標

□未達成目標（請說明，以 100 字為限）

□實驗失敗

□因故實驗中斷

□其他原因

說明：

2. 研究成果在學術期刊發表或申請專利等情形：

論文：■已發表 □未發表之文稿 □撰寫中 □無

專利：□已獲得 □申請中 ■無

技轉：□已技轉 □洽談中 ■無

其他：(以 100 字為限)

本計畫的主要研究成果目前已發表在四篇 IEEE 期刊論文. 另有四篇 IEEE 期刊論文為與其他計畫之共同成果.

3. 請依學術成就、技術創新、社會影響等方面，評估研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）（以 500 字為限）

In this project we have conducted a comprehensive study of variability and carrier transport for advanced silicon-based devices. We have investigated the impact of uniaxial strain on the temperature dependence of mismatching properties of nanoscale MOSFETs [1]. This study is important not only for circuit designs using advanced strained-silicon technologies, but also for the fundamental understanding of intrinsic parameter fluctuations in CMOS devices. In addition, we have experimentally examined the impact of uniaxial strain on the surface-roughness limited mobility using cryogenic temperature measurements [2]. This study has facilitated the understanding of carrier transport in strained-silicon, and provided insights in device designs for future mobility scaling. Besides, we have investigated the impact of quantum confinement on the short-channel effect for UTB GeOI and SOI MOSFETs using derived analytical model [3]. Our theoretical study indicates that, due to the discrepancy in effective mass, the impact of quantum confinement must be considered when one-to-one comparisons between UTB GeOI and SOI MOSFETs regarding the short-channel effect and variability are made.

These research works have been crucial to the education of our graduate students to become leading researchers in silicon-based nanoelectronics. In addition, it is worth mentioning that our recent work (also supported by this NSC project) regarding the impact of self-heating on random mismatch has been accepted and will be presented at 2011 IEDM, the world preeminent forum for reporting technological breakthroughs in the areas of semiconductor and electronic device technology, design, physics, and modeling.

Reference:

[1] J. Kuo, W. Chen, and P. Su*, IEEE Electron Device Lett., vol.32, no.3, pp.240-242, March 2011.

[2] W. Chen, J. Kuo, and P. Su*, IEEE Electron Device Lett., vol.32, no.2, pp.113-115, Feb. 2011.

[3] Y. Wu, H. Hsieh, V. Hu, and P. Su*, IEEE Electron Device Lett., vol.32, no.1, pp.18-20, Jan. 2011.