A Statistical Model for Simulating the Effect of LTPS TFT Device Variation for SOP Applications

Ya-Hsiang Tai, Shih-Che Huang, Wan-Ping Chen, Yu-Te Chao, Yen-Pang Chou, and Guo-Feng Peng

***Abstract*—In this paper, the variation characteristics of low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) are investigated with a statistical approach. A special layout is proposed to investigate the device variation with respect to various devices distances. Two non-Gaussian equations are proposed to fit the device parameter distributions, whose the coefficients of determination (R^2) are both near 0.9, reflecting the validity of the model. Two benchmark circuits are used to compare the difference between the proposed model and the conventional Gaussian distribution for the device parameter distribution. The output behaviors of the digital and analog circuits show that the variation in the short range would greatly affect the performance of the analog circuits and would instead be averaged in the digital circuits.**

***Index Terms*—Poly-Si thin-film transistor (TFT), statistical model, variation.**

I. Introduction

LOW-TEMPERATURE polycrystalline silicon (LTPS) thin-film transistors (TFTs) have higher driving capability and better reliability than amorphous silicon TFTs [1], [2]. Therefore, in addition to be the switch devices inside the pixel, poly-Si TFTs are also promising to be integrated to form the peripheral driver circuits of display electronics onto the glass for advanced display application [3]. This is beneficial to fabricate high resolution and high quality displays. Meanwhile, the cost and reliability issues for the IC bonding for the driving circuits can, therefore, be relieved.

However, poly-Si TFTs are found to suffer from serious variation of device behavior. This has most likely resulted from the diverse and complicated grain distribution in the poly-Si film [3]–[5]. Though, nowadays, several novel recrystallization techniques have been proposed [6]–[9], the variation of device behavior would still exist and there are very few papers discussing this issue. The variation of the device parameter will establish the difficulties for panel designers in designing the panel, since the circuit performance varies with devices variation and will cause nonuniformity of display image. In conventional circuit simulation considering device variation, it is usually assumed that the device variation is natural and can be represented by Gaussian distribution [10]. Nevertheless, the distribution of the poly-Si TFT device parameters has never been thoroughly verified. The validity of device parameters would directly affect the output performance of the TFT circuit. In this paper, the distributions of the poly-Si TFT device parameters are studied with a statistical approach. In Section III-A, a special layout is proposed to investigate the device variation with device distance. Parameters are extracted from more than 600 devices and the discussions about the distributions are given. Two non-Gaussian models are proposed to fit the device parameter variation. Then the effects of device parameter variation are investigated via digital and analog circuits. The ring oscillator is chosen as the benchmark for the digital circuit, while differential pair is chosen for the analog. In Section III-B, the effect of device parameter variation on the output behavior of the ring oscillator is discussed with the measured data and the simulated results. In Section III-C, the effect of device variation on differential pair is examined. The effect is investigated with the cumulative probability curve of the common mode reject ratio (CMRR) value.

Manuscript received November 30, 2006; revised May 23, 2007. This work has been supported by the National Science Council, R.O.C., under NSC 94-2218-E-009-026, and in part by the MOEA Technology Development for Academia Project 94-EC-17-A-07-S1-046.

Y.-H. Tai, W.-P. Chen, and Y.-T. Chao are with the Department of Photonics & Display Institute, National Chiao Tung University, Hsinchu 30010, Taiwan, R.O.C.

S.-C. Huang, Y.-P. Chou, and G.-F. Peng are with the Department of Photonics & Institute of Electro-Optical Engineering, National Chiao Tung University, Hsinchu 30010,Taiwan, R.O.C. (e-mail: hansley.eo92g@nctu.edu.tw).

Color versions of one or more figures are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JDT.2007.903155

II. Experimental

The process flow of TFTs is described below. Top gate LTPS TFTs with width/length dimension of 20 μm/5 μm were fabricated using low temperature process. Firstly, the buffer oxide and a-Si:H films with thickness of 50 nm were deposited on glass substrates with PECVD. The samples were then put in the oven for dehydrogenation. The XeCl excimer laser of wavelength 308 nm and energy density of 400 mJ/cm^2 was applied. The laser scanned the a-Si:H film with the beam width of 4 mm and 98% overlap to recrystallize the a-Si:H film to poly-Si. After poly-Si active area definition, 100-nm SiO_2 was deposited with PECVD as the gate insulator. Next, the metal gate was formed by sputter and then defined. For n-type devices, the lightly doped drain (LDD) and the n^+ source/drain doping were formed by PH_3 implantation with dosage 2×10^{13} cm^{-2} and 2×10^{15} cm^{-2} of PH_3, respectively. The LDD implantation was self-aligned and the n^+ regions were defined with a separate mask. The LDD structure did not use on p-type devices. The p^+ source/drain doping was done by B_2H_6 self-align implantation with a dosage of 2×10^{15} cm^{-2}. Then, the interlayer of SiN_X was deposited. Subsequently, the rapid thermal annealing was conducted to activate the dopants. Meanwhile, the poly-Si film was hydrogenated. Finally, the contact hole formation and metallization were performed to complete the fabrication work.

1551-319X/$25.00 © 2007 IEEE

TABLE I
POSSIBLE FACTORS INFLUENCING THE BEHAVIOR OF LONG-RANGE VARIATION AND MICRO VARIATION

	Long-range variation	Micro variation
Effect on device parameters	Common trends over a range	Random fluctuate among devices
Possible factors	gate insulator thickness, ion implantation dosage, channel length, LDD length	defect sites, defect density, activation efficiency

III. RESULTS AND DISCUSSION

A. Device Variation

In MOSFETs, the device variation can be characterized by short correlation distances and global variations characterized by long correlation distances, where the correlation distance is defined as the distance in which a process disturbance affects the device performances [11]. If this distance is shorter than the usual distance between devices, the disturbance constitutes a local variation and affects few devices (e.g., a charge trapped in the gate oxide layer). For the global variation, which is characterized by process disturbances with longer correlation distances (e.g., the gate oxide thickness fluctuation across the wafer surface), affects all the devices within a defined region. Therefore, the devices placed at longer distance are more affected by global variations than devices placed close to each other. For the case of the poly-Si TFTs, since there are grains randomly located in the active region, the variation behavior may be more complicated than that in MOSFETs. In the following discussion for the poly-Si TFT variation, to avoid the unnecessary confusion, the variation behavior is classified as the long-range variation and the micro variation, which respectively correspond to the global variation and the local variation in the MOSFET case. The possible factors affecting the long-range and micro variation are given in Table I.

Intuitively, if the devices are fabricated very close to each other, then the long-range variation can be avoided. In order to investigate the relationship between uniformity issue and device distance, a special layout of the devices, adopted in this work, is shown in Fig. 1(a). Fig. 1(b) shows the captured picture of the proposed layout. The structure of the poly-Si film and the gate metal are in the order that resembles the crosstie of the railroad and, therefore, this layout is called the crosstie type layout of LTPS TFTs. The pitch between two nearest active regions is equally spaced 40 μm. Within this short device distance, the long-range variation may be ignored, and the variation of device behavior can, therefore, be reduced to only micro variation. In order to obtain the more accurate parameter distributions of crosstie layout TFTs, large amount of device parameters are required. In this work, more than 600 devices are measured and the parameters are extracted.

The distributions of threshold voltage $(\mathrm{V_{th}})$ and mobility (Mu) for both the n-type and p-type TFTs are shown respectively in Figs. 2 and 3. The device parameters of the TFTs are given in Table II. It can be seen that both $V_{\rm th}$ and mobility of the n-type and p-type TFTs do not follow the Gaussian

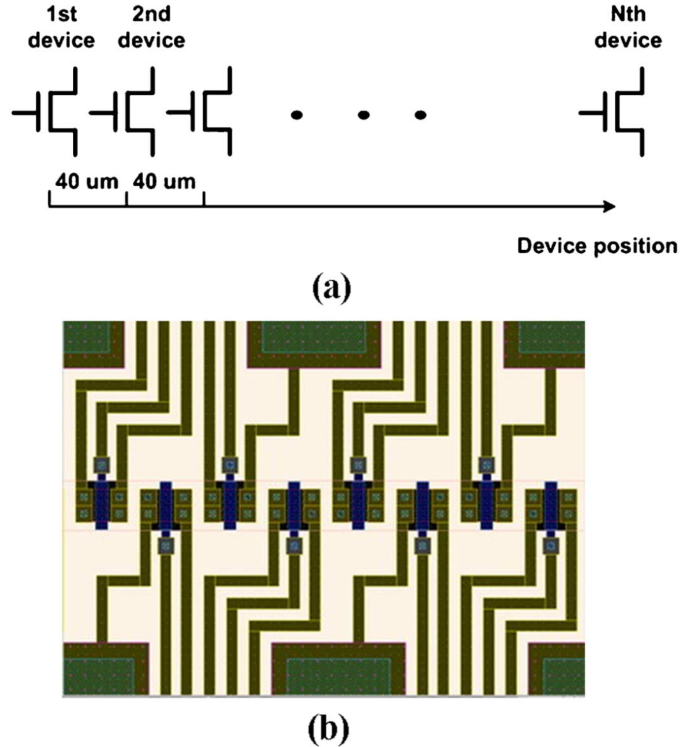


Fig. 1. (a) Figure illustrating the proposed crosstie layout. (b) Captured picture of the proposed layout.

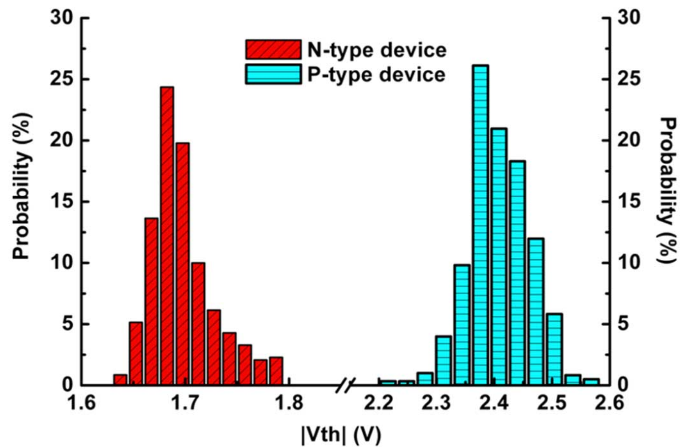


Fig. 2. The $V_{\rm th}$ distribution of the measured crosstie devices for both n-type and p-type devices.

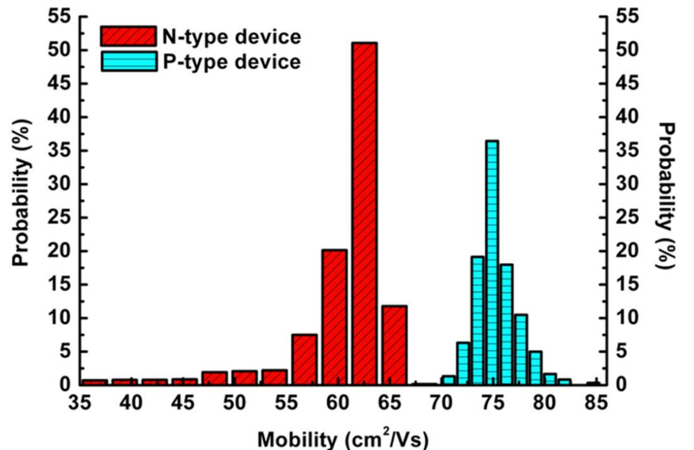


Fig. 3. Mobility distribution of the measured crosstie devices for both n-type and p-type devices.

TABLE II
MEAN VALUE AND THE STANDARD DEVIATION OF THE MEASURED DEVICE PARAMETER

N-type	Vth(V)	Mu(V/dec)
Average	1.69	59.66
Standard Deviation	0.03	7.84
P-type	Vth(V)	Mu(V/dec)
Average	2.41	75.31
Standard Deviation	0.05	2.29

distribution, which contradicts our expectation. This reveals that the conventional Gaussian distribution may not be precise in describing device parameters. Besides, the distribution of mobility exhibits severe nonuniformity behavior. Since the distributions are not symmetric, it would be difficult to build a model to describe the parameters in circuit simulation. In other words, another grouping method should be adopted.

Fig. 4(a) shows the $V_{\rm th}$ distribution of the devices with respect to device position, while Fig. 4(b) shows that of mobility distribution. The distribution resembles the small signal model in electronics. This means that the parameter distribution can be decoupled as the sum of the large signal and the small signal, as shown in Fig. 5. If the parameter difference is calculated within the two nearest devices, the large signal can be subtracted and the true profile of the small signal can then be shown. In this case, the long-range variation can be diminished and the micro variation can then be investigated. The distribution of the $V_{\rm th}$ difference of the two nearest n-type TFTs and p-type TFTs are, respectively, shown in Fig. 6(a) and (b), while that of the mobility difference for n-type and p-type devices are shown in Fig. 7(a) and (b). It can be seen that both the distributions of $V_{\rm th}$ and mobility difference for the devices show symmetric behavior and are quite centered than Gaussian distribution. This reveals that micro variation plays a much centered role for the devices than Gaussian distribution.

Since the distributions of the parameter difference are symmetric, it would be necessary to find a model for circuit simulation. For the distribution of the difference of $\rm V_{th}$, the Gaussian-Lorentzian cross product is applied to the fitting, which is

$$y = \frac{a}{\left(1+d\left(\frac{x-b}{c}\right)^2\right) * \exp\left((1-d) * \frac{1}{2}\left(\frac{x-b}{c}\right)^2\right)}$$

where
- a peak value of the distribution;
- b center of the distribution;
- c fitting parameter related to the width of the distribution;
- d fitting parameter varying from 0 to 1; 0 represents the pure Gaussian function, while 1 is the pure Lorentzian distribution.

As for the distribution of the difference of Mu, the Lorentzian distribution is applied to the fitting, which is

$$y = \frac{a}{1+\left(\frac{x-b}{c}\right)^2}$$

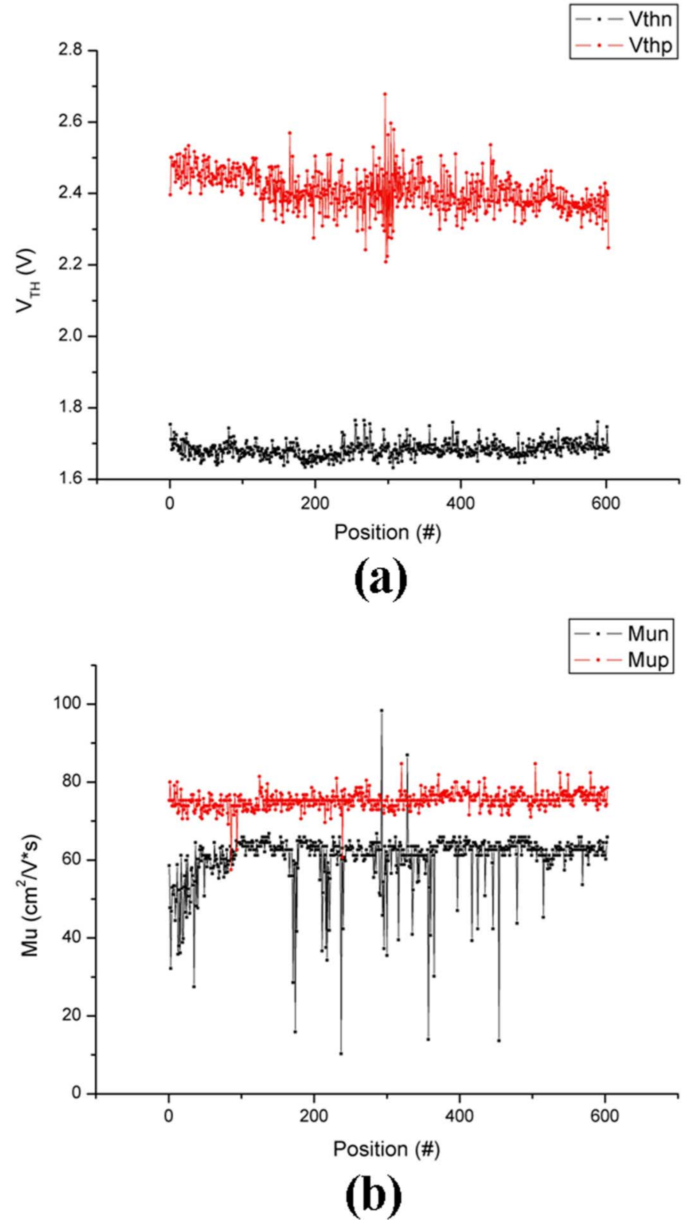


Fig. 4. Distribution of the device parameters with distance for (a) $V_{\rm th}$ and (b) mobility.

where
- a peak value of the distribution;
- b center of the distribution;
- c fitting parameter related to the width of the distribution.

In statistics, the coefficient of determination (R square) is a common index for evaluating the fitness of the proposed model and the real data. Generally, if the value of R square is above 0.7, it means that the specific model shows good fitness with the data [12]. In this work, the values of R square of the above-fitting curves can both approach 0.9, representing the good validity between the proposed model and the real data. However, there could be other equations that could provide higher fitness for describing the micro variation and the corresponding effects on circuit performance. Since the R square reaches above 0.9 for the two proposed models in describing

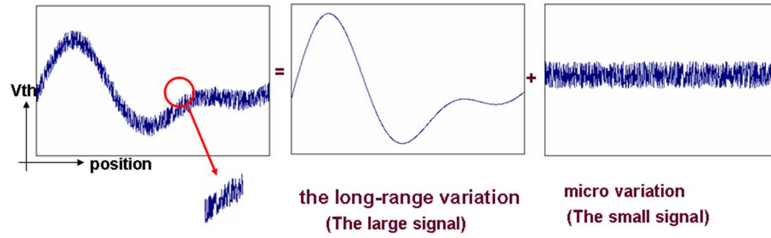
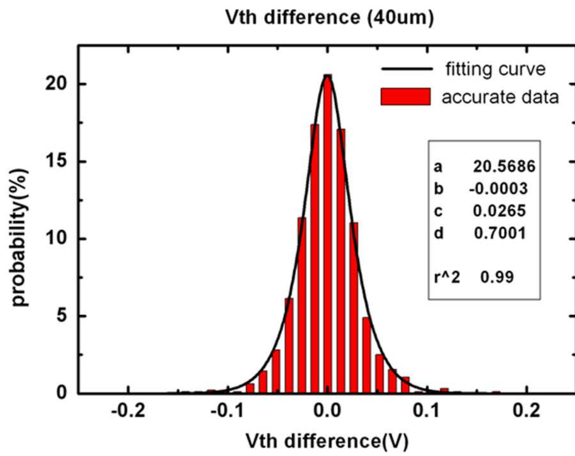


Fig. 5. Figure illustrating the large signal (long-range variation) and the small signal (micro variation) of the device parameters.



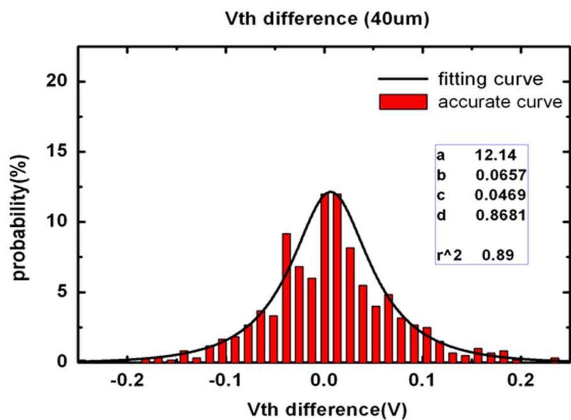
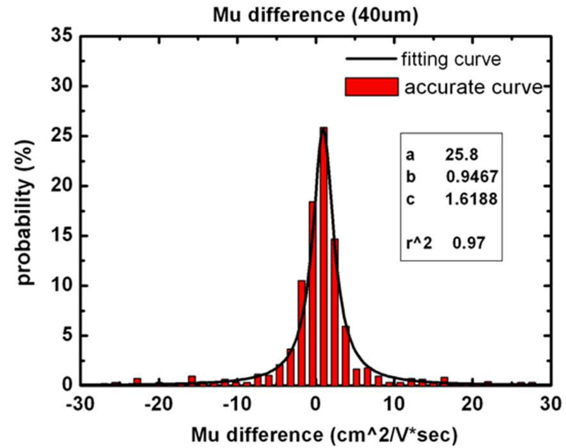


Fig. 6. Proposed model describing the $V_{\rm th}$ variation for the n-type and p-type devices.



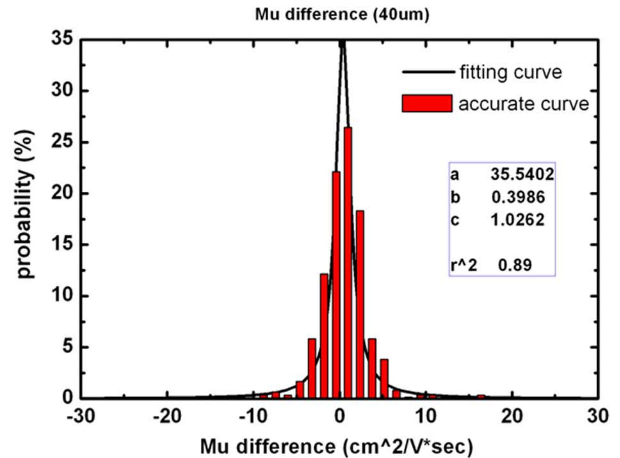


Fig. 7. Proposed model describing the mobility variation for the n-type and p-type devices.

the distribution, it could be fair enough to use these models to evaluate the effect of device variation on both the analog and digital circuits.

B. Effect of Device Variation on Analog Circuits

In the integrated circuit application, coupling effect is a serious problem for signal transmission. Output signal suffering from serious coupling effect may lead to the errors of the retrieved signal and affect the corresponding design window. In order to reinforce the immunity to the noise and the coupling effect during the transmission, the differential signals are widely used for analog circuit design. For the display applications, the differential pairs are commonly used in many blocks of display electronics, such as the input stage of operational amplifier. Fig. 8 shows the basic differential pair structure, where $\rm R_D$ is the resistive load and Rss represents the output impedance of current bias; differential signals are applied to the gate terminal of transistor M1 and M2.

The quality of data transmission will benefit by differential signal. However, device variation would be a serious problem for differential pair. Since these devices are nominally identical, the variation of the device characteristics will result in errors in retrieving the signal and affect the accuracy of the differential signal. In conventional MOSFET circuits, the variation effect is very low and can be suppressed under the well-controlled

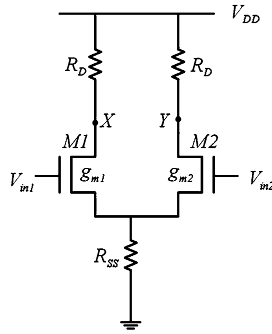


Fig. 8. Conventional structure of the differential pair circuit.

process. As compared to CMOS, LTPS TFTs suffer form worse device variation and the effect of output signal variation may hence be more complicated. In order to evaluate the circuit performance of differential pair by LTPS TFTs, the aforementioned variation models would be adopted to simulate the circuit performance with device variation.

The common mode rejection ratio (CMRR) is a common index for the capability of differential pair against the common mode noise, which can be written as

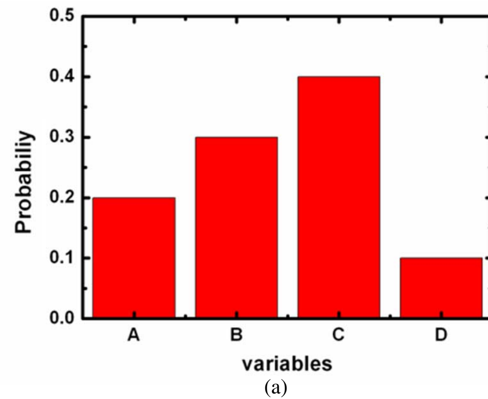
$$\mathrm{CMRR} = \left|\frac{A_{dm}}{A_{cm-dm}}\right| \cong \frac{\mu(V_{\mathrm{GS}} - V_{\mathrm{th}}) + 2\mu^2 C_{\mathrm{ox}} \frac{W}{L}(V_{\mathrm{GS}} - V_{\mathrm{th}})^2 Rss}{\mu\Delta_{\mathrm{th}} + \Delta\mu(V_{\mathrm{GS}} - V_{\mathrm{th}})}.$$

In the equation above, the Δ $\mathrm{V_{th}}$ and $\Delta\mu$ terms represent the differences of threshold voltage and mobility of the two transistors. In this work, the CMRR value is used as the index to examine the accuracy of each simulation skill and model.

Before the simulation, it is essential to transform the variation model into the corresponding value for Monte Carlo simulation. In this work, a method of range mapping is used. Take the distribution consisting of four variables as example, as shown in Fig. 9(a). Based on the probability, a table of range mapping can be established, as shown in Fig. 9(b). For a series of uniformly random values in the range from 0 to 1 generated by the computer, the corresponding series can be obtained by looking up table in Fig. 9(b). If 0.3 is randomly picked from computer, the variable B will be chosen according to Fig. 9(a). Thus, the distribution of the look-up values will match that shown in Fig. 9(a). In the light of statistics thoery, a certain number of data for each distribution can be generated to get the stable and reliable simulation result. In this work, 210 000 times of data transformation for each distribution are executed to obtain the best and stable result for the Monte Carlo simulation.

In simulation, the $\mathrm{V_{GS}}$ is set to 5 V, which is the voltage at the quiescent point. The output impedance of current bias is 3 MΩ, which is extracted from the output resistance at the corresponding bias point. To compare the effects of the device variation on circuit performance with different models, two distribution models are adopted in the Monte Carlo simulation to calculate the CMRR value under the constant device distance of 200 μm. One is the proposed model and the other is the widely adopted Gaussian distribution. The parameters of Gaussian distribution used here are 1.69, 0.03, 59.66 cm^2/V·s and 7.84 cm^2/V·s, which respectively correspond to the mean value and the deviation of the threshold voltage and mobility from the measured database.

The simulation of the cumulative distribution of the CMRR value in decibels is shown in Fig. 10. The results of Monte Carlo method with Gaussian distribution and our proposed



(a)

Random value	Corresponding variable
0 ~ 0.2	A
0.2 ~ 0.5	B
0.5 ~ 0.9	C
0.9 ~ 1.0	D

(b)

Fig. 9. (a) Simple distribution for the variable mapping. (b) A look-up table for the variable mapping base.

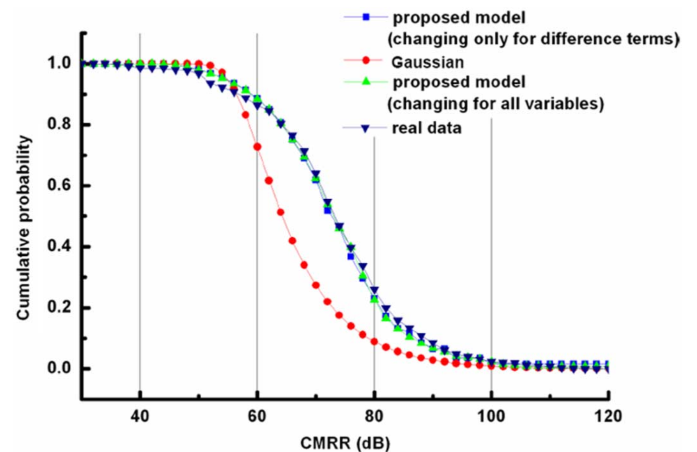


Fig. 10. Cumulative distribution for the CMRR value of the differential pair with a different device parameter model.

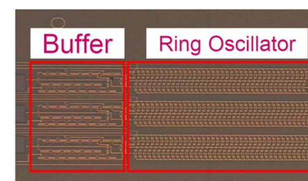


Fig. 11. Photograph of the fabricated ring oscillator circuits.

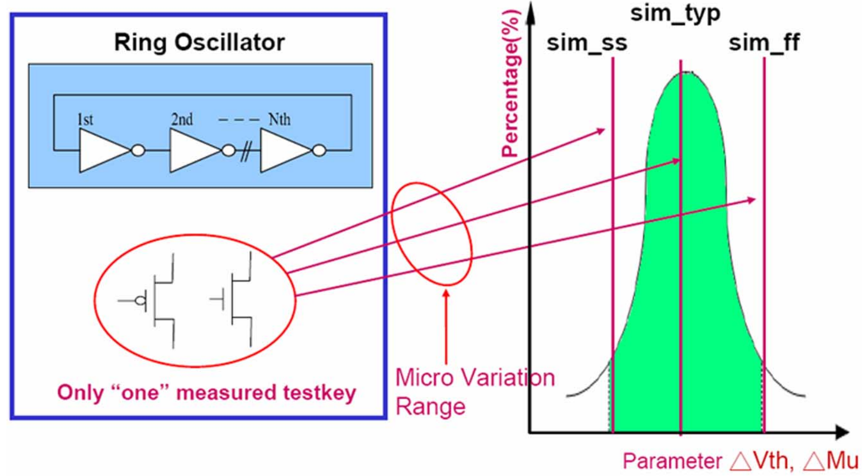


Fig. 12. Figure illustrating the upper and lower bound of the device variation model.

model are represnted by lines with circles, squares and triangles individually. The line with circle symbols is plotted by Monte Carlo method with Gaussian distribution. As for the line with squares and triangles, they are done by Monte Carlo method with our proposed models. For the line with squares, the threshold voltage and mobility and their difference are substituted with real parameter and proposed model. For the line with triangles, the difference term are from the parameters randomly generated from the proposed model while other device parameters are replaced with the average value from the measured database. It can be observed that the lines with squares and triangles are almost overlapped, and this reveals that the difference terms dominate the simulation result of CMRR value. Therefore, the simulation procedure can be simplified as only change the the difference terms instead. Among the lines with circles and triangles, it is found that the curves of the cumulative probability exhibit a difference of 10 dB in average and cross at about 55 dB. It is attributted to the sharper distribution of the difference of $\mathrm{V_{th}}$ and Mu in reality than the Gaussian distribution.

If all the real measured data are used in calculation (the line with inverted triangles) under the constant device distance 200 μm, it can be observed that lines with squares, triangles and inverted triangles are almost the same. The simulation result shows that the Monte Carlo method with our proposed model is more accurate than that with Gaussian model. Generally speaking, the specification of the CMRR value in commerical IC is usually desired to reach above 60 dB. Obviously, design with the conventional Gaussian simulation method will underestimate the circuit performance of differential pair compared with the proposed model. However, it should still be noticed that if it is required to reach a confidence level of 98%, the CMRR specification of the circuit should be set below 50 dB based on the proposed model, instead of 53 dB corresponding to Gaussian model. As for the average performance, simulation adopting Gaussian distribution might give an underestimated prediction. Since the proposed model is the distribution originated from real data, it should provide a more reliable description of the device performance for a large amount of devices.

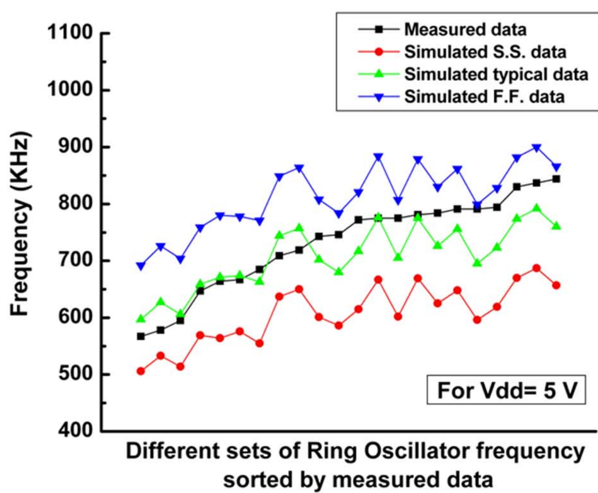
C. Effect of Device Variation on Digital Circuits

In this part, the effects of device variation on the digital circuits are investigated. Though digital circuits do not require high definition of the signals as the analog circuits do, the effect of device variation may still lead to the errors of the output signals. In this work, ring oscillator is set as our benchmark of investigation because of its sensitivity to the simulation model. Because there are more than 100 devices in the circuits, the long-range variation may take place and form the trend in the device parameter distribution. Since so far there is no adequate description to depict the effect of long-range variation on the device parameters, the method used in discussing the output variation of differential pairs may not be suitable here. In other words, another comparing method should be adopted to investigate the effect of micro variation in ring oscillators.

The figure of the implemented circuit and the test device is shown in Fig. 11. The 105-stage ring oscillator is fabricated and a test device is placed just by the ring oscillators. Since the effect of variation could not be compared from device to device, the upper and lower bounds of variation range are used instead. The simulation will be done by three conditions sim_typ, sim_ff and sim_ss. The sim_typ is that all the devices are simulated with the measured test device parameter directly. This depicts the condition that the measured device parameter is the same as all the devices inside the ring oscillator circuit. For the case that the micro variation exists between the test device and the devices in the circuits, two conditions are taken into consideration, as shown in Fig. 12. Sim_ff is simulated with the possibly high mobility and low threshold voltages of both N-TFT and P-TFT at 99.5% and 0.5% of the variation model respectively. This simulation condition describes the conditions that the test device parameters are just the worse performance than those in the circuit. In other words, the devices in the ring oscillator are faster than the test device with the magnitude of 0.5% slow in mobility and 99.5% high in $V_{\rm th}$in the population according to the proposed micro variation model based on measured data. On the contrary, sim_ss is with the possibly low mobility and high threshold voltages at 0.5% and 99.5% of the variation model, respectively. This represents the conditions that the test device

TABLE III
UPPER AND LOWER BOUND OF THE PARAMETERS USED IN THE SIMULATION OF RING OSCILLATOR

Population in the proposed micro variation model	0.50%	99.50%
Δ Vthn (V)	-0.147	0.142
Δ Mun (cm²/Vs)	-10.223	9.723
Δ Vthp (V)	-0.155	0.150
Δ Mup (cm²/Vs)	-9.216	8.716



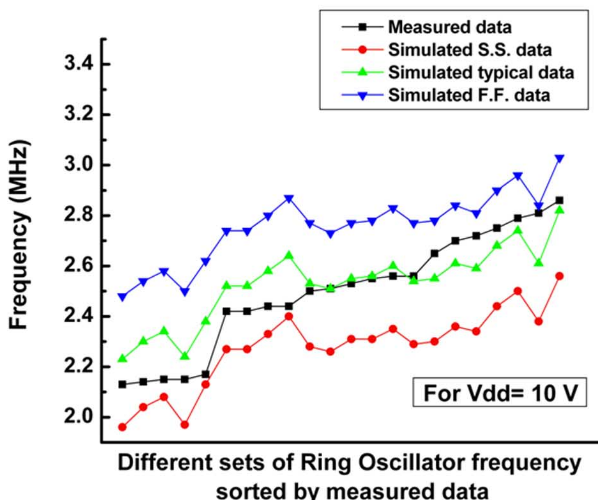


Fig. 13. Simulated and measured ring oscillator operating frequency with (a) operating voltage 5 V and (b) operating voltage 10 V.

just has the better performance than those in the circuit. The parameters used in simulation are shown in Table III. Fig. 13(a) and (b) show the simulation results with micro variation for the 105-stage ring oscillator as the operating voltage is 5 and 10 V, respectively. In this work, 22 sets of ring oscillators and their corresponding test devices next to each other are fabricated and the measured. In these figures, the data are sorted by measured frequency. It can be seen that for both operating voltages, the simulation data from the Sim_ff and Sim_ss form the gap of the operating frequency. It can be seen that the measured data all fall in this gap. This represents that proposed model can fairly describe the range of the micro variation for the devices in the ring oscillator. Besides, there is no large difference between the measured data and the simulation data with the parameters from the test device. This may reveal that though the micro variation exists between the devices in the ring oscillator, the effect of the micro variation on the overall performance will be averaged and, therefore, the micro variation may be ignored in the simulation of ring oscillator. However, it should also be noted that the range of the measured operating frequency is so large comparing to the gap of the lowest driving frequency of the simulation data S.S. and F.F. This means that though the micro variation may be ignored in the ring oscillator simulation, the long-range variation may instead influence the performance and the effect can be very critical. This finding would be important in the characterization and simulation of the digital circuit simulation.

IV. CONCLUSION

This paper focuses on the variation in the behavior of poly-Si TFTs. The variation is classified as the long-range variation and micro variation and a special layout is proposed to characterize the behavior of micro variation. Two non-Gaussian models are proposed to describe the variation behavior. The models are then used to simulate the analog and digital circuits considering device variation. For the analog circuits, it is discovered that the micro variation would directly affect the output performance of the differential pair. On the other hand, the effect of micro variation on the digital circuits would be averaged and instead the long-range variation would be the dominant factor to affect the output performance. These models can be also applied to the simulation for the uniformity of the AMOLED using matched TFT in the pixel design and other analog circuit design in display electronics with LTPS TFTs.

REFERENCES

[1] Y. Nakajima, "Latest development of "system-on-glass" display with low temperature poly-Si TFT," *SID Tech. Dig.*, p. 864, 2004.

[2] H. Oshima and S. Morozumi, "Future trends for TFT integrated circuit on glass substrate," in *IEDM Tech. Dig.*, 1989, p. 157.

[3] K. Yoshiyuki, T. Shuichi, and S. Nobuyuki, "A new grain boundary model for drift-diffusion device simulations in polycrystalline silicon thin-film transistors," *Jpn. J. Appl. Phys., Part 2: Lett.*, vol. 42, no. 6 B, pp. L634–L636, Jun. 2003.

[4] A. W. Wang and K. C. Saraswat, "Modeling of grain size variation effects in polycrystalline thin film transistors," in *IEDM Tech. Dig.*, 1998, pp. 277–280.

[5] A. W. Wang and K. C. Saraswat, "A strategy for modeling of variations due to grain size in polycrystalline thin-film transistors," *IEEE Trans. Electron Devices*, vol. 47, no. 5, pp. 1035–1043, May 2000.

[6] N.-K. Song, M.-S. Kim, Y.-J. Pyo, and S.-K. Joo, "A study on the Pd/a-Si/Ni seed layer for metal-induced lateral crystallization and poly-Si TFTs," *IEEE Electron Device Lett.*, vol. 27, no. 11, pp. 899–901, Nov. 2006.

[7] R. Ishihara, A. Glazer, Y. Raab, P. Rusian, M. Dorfan, B. Lavi, I. Leizerson, A. Kishinevsky, Y. Van Andel, X. Cao, W. Metselaar, K. Beenakker, S. Stolyarova, and Y. Nemirovsky, "A novel Selected Area Laser Assisted (SALA) system for crystallization and doping processes in low-temperature poly-Si thin-film transistors," *IEICE Trans. Electron.*, vol. E89-C, no. 10, pp. 1377–1382, Oct. 2006.

[8] C.-Y. Hou, C.-C. Lin, and Y. C. S. Wu, "Gettering of Ni from Ni-metal induced lateral crystallization polycrystalline silicon films using a gettering substrate," *Jpn. J. Appl. Phys., Pt. 1*, vol. 45, no. 9 A, pp. 6803–6805, Sept. 7, 2006.

[9] M. A. Crowder, M. Moriguchi, Y. Mitani, and A. T. Voutsas, "Parametric investigation of SLS-processed poly-silicon thin films for TFT applications," *Thin Solid Films*, vol. 427, no. 1–2, pp. 101–107, Mar. 3, 2003.

[10] K. Okada, K. Yamaoka, and H. Onodera, "Statistical modeling of gate-delay variation with consideration of intra-gate variability," in *Proc. IEEE Int. Symp. Circuits Syst.*, 2003, vol. 5, pp. V513–V516.

[11] C. Michael and M. Ismail, *Statistical Modeling For Computer-Aided Design of MOS VLSI Circuits*. Amsterdam, The Netherlands: Kluwer Academic, 1993, pp. 8–10.

[12] J. L. Devore, *Probability and Statistics For Engineering and the Sciences*, 3rd ed. Toronto, Canada: Thomson Inf./Publ. Group, 1991, pp. 466–468, 489–490.

Ya-Hsiang Tai received the B.S. and Ph.D. degrees in electronic engineering from National Chiao Tung University, Taiwan, R.O.C., in 1990 and 1996, respectively.

He became a member of Industrial Technology Research Institute/Electronics Research & Service Organization and the TFT LCD development as a panel designer. He joined the project of low temperature polycrystalline silicon (LTPS) thin-film transistor (TFT) development in Prime View International in 2000. In 2001, he joined Toppoly Optoelectronics Corporation, Taiwan, to lead the team of LTPS TFT LCD panel design. He joined the faculty of National Chiao Tung University in 2003, where he is currently an associate professor in the Department of Photonics and Display Institute. His current research emphases are in the areas of TFT device physics, active matrix display panel design, and system on panel.

Dr. Tai is a member of Phi Tau Phi.

Shih-Che Huang received the B.S. degree in physics from National Sun Yat-Sen University. Taiwan, in 2002, and the M.S. degree in electro-optical engineering in National Chiao Tung University', Taiwan, R.O.C., in 2004, where he is now working toward the Ph.D. degree.

His current research interests include the uniformity and applications of low-temperature poly-Si TFTs.

Wan-Ping Chen received the M.S. degree in electro-optical engineering from National Chiao Tung University, Taiwan, R.O.C. in 2006.

Her current research interest is low-temperature poly-Si TFTs circuits for driving methods.

Yu-Te Chao received the B.S. degree in electronic engineering from Chang Gung University, Taiwan, R.O.C., in 2005.

His current research interest is device variation behavior of low-temperature poly-Si TFTs.

Yen-Pang Chou received the B.S. degree in machine engineering and electronic engineering from National Sun Yat-Sen University, R.O.C. in 2002.

After military service he joined the institute of electro-optical engineering in National Chiao Tung University, Taiwan, R.O.C. His current research is the uniformity issue of low temperature polysilicon TFTs.

Guo-Feng Peng received the B.S. degree in electronic engineering from National Taiwan Ocean University in 2004.

He then joined the Institute of Electro-Optical Engineering in National Chiao Tung University, Taiwan, R.O.C. His current interests are the uniformity and reliability issues of low temperature polysilicon TFTs.