HfLaON n-MOSFETs Using a Low Work Function $HfSi_x$ Gate

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***Abstract*—At a 1.2-nm equivalent oxide thickness, $HfSi_x/Hf_{0.7}La_{0.3}ON$ n-MOSFETs showed an effective work function of 4.33 eV, a low threshold voltage of 0.18 V, and a peak electron mobility of 215 $cm^2/(V \cdot s)$. These self-aligned and gate-first $HfSi_x/Hf_{0.7}La_{0.3}ON$ n-MOSFETs were processed using standard ion implantation and 1000-°C rapid thermal annealing, making them fully compatible with current very large scale integration fabrication lines.**

***Index Terms*—HfLaON, HfSi, n-MOSFETs.**

I. Introduction

METAL GATES and high-κ gate dielectrics are necessary for complementary MOSFETs at the 45-nm nodes and beyond [1]–[15] to reduce the dc power consumption from the gate current and continue the very large scale integration (VLSI) scaling. This poses a difficult technological challenge in that the large threshold voltage V_t that results from Fermi-level pinning is opposite to the trend needed for device scaling. To avoid this, it requires appropriate choices of the metal-gate work function and high-κ dielectric—to reduce the pinning to achieve the required low V_t. Previously, we have shown that Fermi-level pinning can be reduced, even after surface plasma nitridation, by adding La_2O_3 to HfO_2 to produce the gate dielectric $Hf_{0.5}La_{0.5}ON$ at 1.6-nm equivalent oxide thickness (EOT). Thus, a relatively low V_t can be achieved with a conventional TaN gate [15]. Here, we report the use of a low work function fully silicided (FUSI) $HfSi_x$ gate for $Hf_{0.7}La_{0.3}ON$ n-MOSFETs at a scaled EOT of 1.2 nm and reduced La composition of 30%. This gate yields a more negative flatband voltage V_{fb} than does a TaN gate. The resulting MOSFETs show a V_t of 0.18 V, a low leakage current of 9.2×10^{-4} A/cm^2 at 1 V above V_{fb}, and 1.2-nm EOT, with an electron mobility of 215 $cm^2/(V \cdot s)$. These devices can endure a rapid thermal annealing (RTA) temperature of 1000 °C, which is common in current poly-Si gate technology.

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II. Experimental Procedure

We used the 4-in p-type Si wafers in these experiments. After a standard RCA clean, the $Hf_{0.7}La_{0.3}O$ was deposited on Si wafers by physical vapor deposition (PVD). Then, the $Hf_{0.7}La_{0.3}O$ surface was exposed to a nitrogen plasma to form the $Hf_{0.7}La_{0.3}ON$ gate dielectric. Amorphous Si of 5-nm thickness was deposited on $Hf_{0.7}La_{0.3}ON$ followed by a PVD of 20-nm-thick Hf. To prevent Hf oxidation, a 30-nm-thick Mo was subsequently deposited above the Hf/Si/$Hf_{0.7}La_{0.3}ON$ to form n-MOS capacitors. For n-MOSFETs, an additional 150-nm-thick amorphous Si was deposited to avoid ion implantation damage through the gate. The n^+ source–drain regions were formed by using a 35-keV phosphorus ion implantation (at a 5×10^{15} cm^{-2} dose) followed by RTA activation at 1000 °C for 5 s. (Note that the FUSI $HfSi_x$ gate was formed at a high RTA temperature, similar to Ir_3Si [14], which is different from a conventional low-temperature salicide process.) For comparison, TaN gates were also deposited on $Hf_{0.7}La_{0.3}ON$ to form the n-MOS capacitors. The fabricated devices were characterized by C–V and I–V measurements using an HP4284A precision inductance–capacitance–resistance meter and HP4156 semiconductor parameter analyzer, respectively.

III. Results and Discussion

In Fig. 1(a) and (b), we show the C–V and J–V characteristics of $HfSi_x/Hf_{0.7}La_{0.3}ON$ and control TaN/$Hf_{0.7}La_{0.3}ON$ capacitors, respectively. For comparison, the characteristics of a capacitor with a TaN gate on $Hf_{0.7}La_{0.3}ON$ are included. The FUSI $HfSi_x$ gate without poly-Si depletion—as formed by Hf deposition on thin 5-nm amorphous Si at 1000-°C RTA—produces devices with a high capacitance density close to those using a TaN gate. However, the V_{fb} of the $HfSi_x$ gate is more negative than for the TaN gate, which is needed for low V_t operation. An EOT of 1.2 nm was found using a quantum–mechanical C–V simulation. A low $\phi_{m\text{-eff}}$ of 4.33 eV was obtained from a V_{fb}–EOT plot for the $HfSi_x/Hf_{0.7}La_{0.3}ON$ devices, making them suitable for n-MOS applications. The leakage current of 9.2×10^{-4} A/cm^2 (at 1 V beyond V_{fb}) is about five orders-of-magnitude lower than that of SiO_2 at a 1.2-nm EOT. This low leakage current is due to the high-κ $Hf_{0.7}La_{0.3}ON$, highlighting the good thermal stability of the $HfSi_x/Hf_{0.7}La_{0.3}ON$ gate structure after a 1000-°C RTA. The higher leakage current at low voltages using TaN gate than that of $HfSi_x$ may be due to the sputter-induced damage to the $Hf_{0.7}La_{0.3}ON$ gate dielectric. Thus, low $\phi_{m\text{-eff}}$

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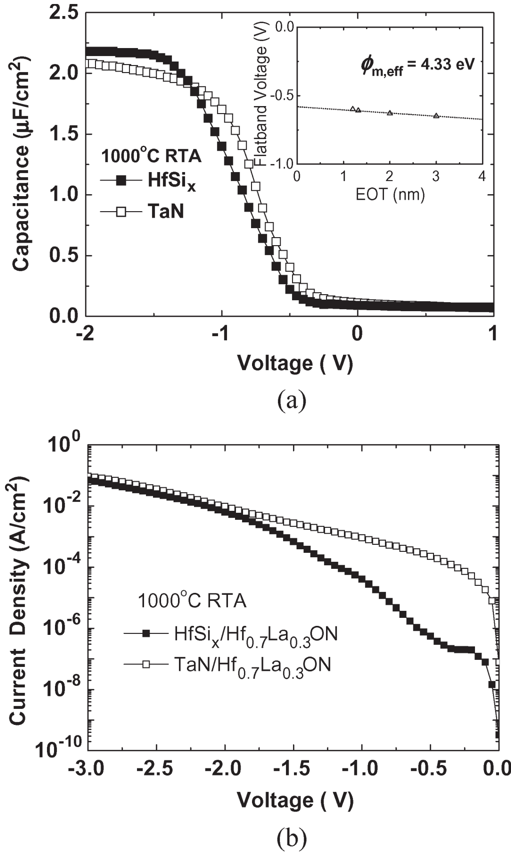

Fig. 1. (a) C–V and (b) J–V characteristics of the $HfSi_x/Hf_{0.7}La_{0.3}ON$ n-MOS capacitors, after a 1000-°C RTA. The inserted figure is a V_{fb}−EOT plot.

and low gate dielectric leakage current can be achieved in $HfSi_x/Hf_{0.7}La_{0.3}ON$ MOS capacitors.

Fig. 2(a) and (b) shows the I_d–V_d and I_d–V_g transistor characteristics of the 1.2-nm EOT $HfSi_x/Hf_{0.7}La_{0.3}ON$ n-MOSFETs. A small V_t of only 0.18 V was measured from the linear I_d–V_g plot—this is due to the low $\phi_{m\text{-eff}}$ of 4.33 eV found from the C–V measurements.

The electron mobility as a function of effective electric field for the $HfSi_x/Hf_{0.7}La_{0.3}ON$ n-MOSFETs is shown in Fig. 3, where the data were derived from measured I_d–V_g curves. High peak electron mobility of 215 $cm^2/(V \cdot s)$ is obtained at a small EOT of 1.2 nm. In Table I, we summarize and compare the important transistor characteristics for various metal-gate/high-κ n-MOSFETs. The merits of the $HfSi_x/Hf_{0.7}La_{0.3}ON$ n-MOSFETs are the small EOT of 1.2 nm, a low V_t of 0.18 V, a good peak mobility of 215 $cm^2/(V \cdot s)$, and simple high-temperature FUSI processing.

IV. Conclusion

We have found good performance in terms of V_t and mobility for $Hf_{0.7}La_{0.3}ON$ n-MOSFETs at 1.2-nm EOT using a low work-function and high-temperature-stable $HfSi_x$ gate. The self-aligned and gate-first $HfSi_x$/HfLaON n-MOSFETs have the advantages of simple high-temperature FUSI processing and compatibility with current VLSI lines.

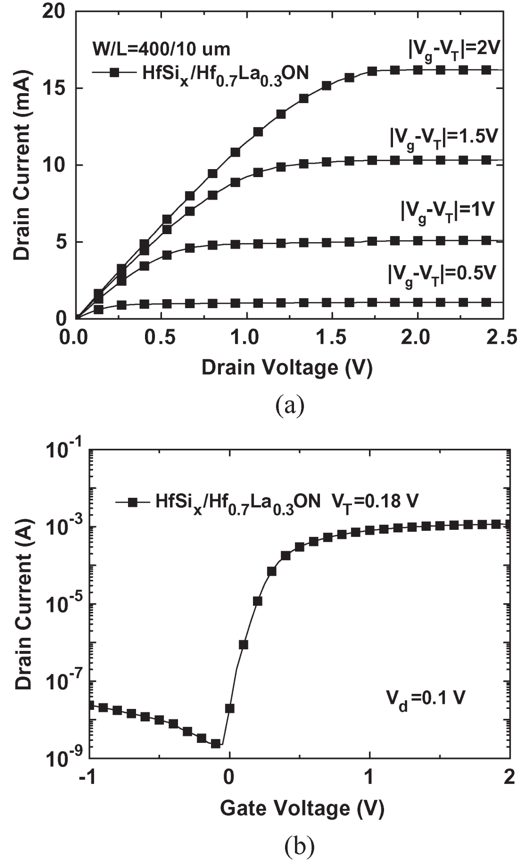

Fig. 2. (a) I_d–V_d and (b) I_d–V_g characteristics of the $HfSi_x/Hf_{0.7}La_{0.3}ON$ n-MOSFETs.

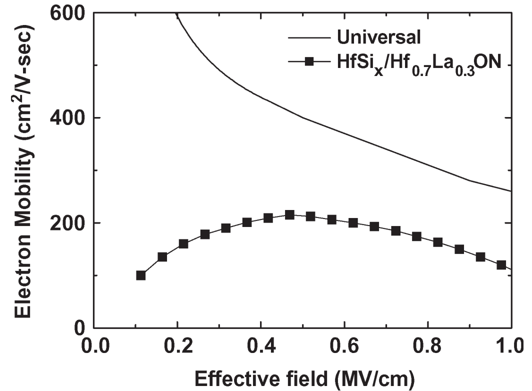

Fig. 3. Electron mobility versus effective electric field for the $HfSi_x/Hf_{0.7}La_{0.3}ON$ n-MOSFETs.

TABLE I
Comparison of Device Parameters for Metal-Gate/High-κ n-MOSFETs

High-κ	Metal Gate	EOT (nm)	V_t (V)	Process Temp.
HfLaON This work	**$HfSi_x$**	**1.2**	**0.18**	**1000oC**
HfLaON [15]	TaN	1.6	0.18	1000oC
HfAlON [11]	Yb_xSi	1.7	0.1	Low Temp. FUSI
HfTaO [10]	TaN	1.6	-	1000oC
HfSiON [13]	TaC	1.2	~0.4	1000oC
HfSiON [12]	NiSi	1.5	0.5	Low Temp. FUSI
HfSiON [9]	$NiSi_2$	1.7	0.47	Low Temp. FUSI

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