A Constant-Mobility Method to Enable MOSFET Series-Resistance Extraction

Da-Wen Lin, Ming-Lung Cheng, Shyh-Wei Wang, Chung-Cheng Wu, and Ming-Jer Chen

***Abstract*—A new method of extracting the MOSFET series resistance $R_{\rm sd}$ is proposed. This method requires only simple dc measurements on a single test device. Experimental demonstration is presented, without requiring quantities such as gate-oxide thickness, physical gate length, or effective channel length. The merit of the method stems from the specifically arranged bias conditions in which the channel carrier mobility remains constant for high vertical electric fields. It is this unique property which makes the proposed method suitable for short-channel devices.**

***Index Terms*—Mobility, MOSFET, series resistance.**

I. Introduction

ON THE BASIS of the MOSFET equivalent circuit (the inset in Fig. 1), the series resistance $R_{\rm sd}$ leads to excess potential drop, reducing the intrinsic voltages and degrading the drive capacity. As the gate length $L_{\rm gate}$ shrinks, the $R_{\rm sd}$ becomes a larger portion of the total resistance. Hence, the drive current degradation is more serious in short-channel devices. Many methods of extracting $R_{\rm sd}$, which rely on the hypothesis that the channel dopant concentration and/or the carrier mobility is independent of $L_{\rm gate}$, have been published in previous literature [1]–[3]. However, in today's MOSFET technology, halo ion implantation and mechanical-stress-dependent dopant diffusion [4] can cause significant nonuniform channel dopant profiles; therefore, use of the traditional methods is problematic.

Here, we present a new method along with experimental demonstration and verification, without accounting for the gate or channel length. This is achieved by means of specifically arranged bias conditions under which the channel carrier mobility is kept constant, regardless of the varying channel dopant concentration caused by threshold-voltage adjustment or the local dopant fluctuation. Unlike the previous methods [1]–[3], [5], which require a considerable number of device samples with different $L_{\rm gate}$ values and/or C–V measurements, the $R_{\rm sd}$ extraction can be realized on a single test device with only dc measurements using this new method.

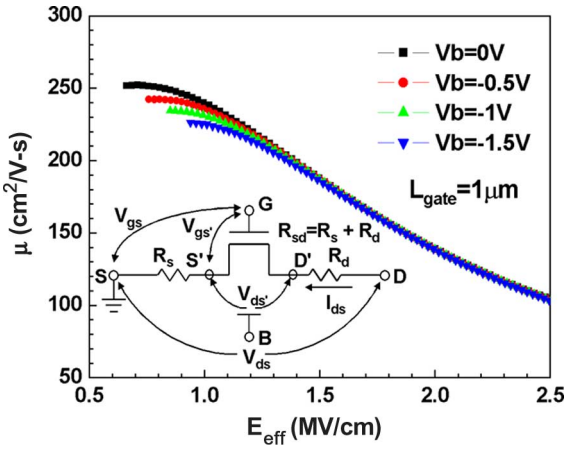

Fig. 1. Measured mobility behavior under different $V_{\rm bs}$ bias conditions. The inversion carrier mobility converges to the same trend when $E_{\rm eff}$ is sufficiently high. The inset is a schematic illustration of the equivalent circuit of the device used in the $R_{\rm sd}$ extraction.

II. Constant-Mobility Bias Conditions

Fig. 1 shows a typical relationship between the measured channel carrier mobility versus the effective silicon vertical electrical field $(E_{\rm eff})$ at the SiO_2/Si interface. Under various back-bias $(V_{\rm bs})$ conditions, the carrier mobility appears to converge toward the universal curve in the high $E_{\rm eff}$ region [6], where surface-roughness scattering becomes the dominant mechanism. If the device is operated in the high $E_{\rm eff}$ region, a constant mobility is achieved for a given $E_{\rm eff}$, regardless of the varying impurity- and phonon-scattering counterparts. The corresponding $E_{\rm eff}$ can be expressed as

$$E_{\rm eff} = \frac{1}{\varepsilon_{\rm Si}}\left(|Q_d| + \frac{1}{\eta}|Q_i|\right) \tag{1}$$

where $\varepsilon_{\rm Si}$ is the silicon permittivity, Q_d is the depletion charge, and Q_i is the inversion-layer charge. η is an empirical factor with the values $\sim$2 and $\sim$3 commonly used for electrons and holes at room temperature, respectively [6]–[11]. Based on the derivation procedure described elsewhere [12], (1) can be further written as

$$E_{\rm eff} = \frac{V_{\rm gs} + (\eta - 1)V_{\rm th} - \eta V_{\rm FB} - 2\eta\Psi_B}{3\eta T_{\rm OX}} \tag{2}$$

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D.-W. Lin is with the Taiwan Semiconductor Manufacturing Company, Hsinchu 300, Taiwan, R.O.C., and also with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C. (e-mail: dwlin@tsmc.com).

M.-L. Cheng, S.-W. Wang, and C.-C. Wu are with the Taiwan Semiconductor Manufacturing Company, Hsinchu 300, Taiwan, R.O.C.

M.-J. Chen is with the Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C.

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where $V_{\rm FB}$ is the flatband voltage, and Ψ_B is the potential difference between the Fermi level and the intrinsic Fermi level. Both $V_{\rm FB}$ and Ψ_B are essentially unchanged for a single device operated under different bias conditions. It follows from (2) that the gate-to-source voltage $V_{\rm gs}$ and the threshold voltage $V_{\rm th}$ can be adjusted simultaneously to achieve a constant $E_{\rm eff}$ under different $V_{\rm bs}$'s. Given an initial $V_{\rm gs}^{(0)}$ and $V_{\rm th}^{(0)}$, the same $E_{\rm eff}$ value can be preserved for other biases $V_{\rm gs}^{(1)}$ and $V_{\rm th}^{(1)}$, satisfying $V_{\rm gs}^{(1)} = V_{\rm gs}^{(0)} + (\eta - 1)(V_{\rm th}^{(0)} - V_{\rm th}^{(1)})$. Consequently, a constant mobility can be obtained.

III. Series-Resistance Extraction

By incorporating the constant-mobility criterion into the current equation of MOSFETs operating in the linear region, the results for the two specific bias conditions (separately labeled with the superscripts 1 and 2) are

$$I_d^{(1)} = \frac{C_{\rm ox} W_{\rm eff} \mu^{(1)}}{L_{\rm eff}} \left(V_{\rm gs}^{(1)} - V_{\rm th}^{(1)} - \frac{1}{2} V_{\rm ds} \right) \times \left(V_{\rm ds} - R_{\rm sd} I_d^{(1)} \right) \tag{3}$$

$$I_d^{(2)} = \frac{C_{\rm ox} W_{\rm eff} \mu^{(2)}}{L_{\rm eff}} \left(V_{\rm gs}^{(2)} - V_{\rm th}^{(2)} - \frac{1}{2} V_{\rm ds} \right) \times \left(V_{\rm ds} - R_{\rm sd} I_d^{(2)} \right). \tag{4}$$

Here, $V_{\rm ds} = 0.05$ V is used to ensure a linear operation mode. As previously mentioned, the mobility is the same between the two specific voltages $V_{\rm gs}$ and $V_{\rm th}$, i.e., $\mu^{(1)} = \mu^{(2)}$ under a high $E_{\rm eff}$ condition. By dividing (3) by (4), the $R_{\rm sd}$ can be derived as

$$R_{\rm sd} = \left(\frac{B}{I_d^{(2)}} - \frac{A}{I_d^{(1)}} \right) \frac{V_{\rm ds}}{\eta \left(V_{\rm th}^{(1)} - V_{\rm th}^{(2)} \right)} \tag{5}$$

where $A = V_{\rm gs}^{(1)} - V_{\rm th}^{(1)} - 0.5 V_{\rm ds}$, and $B = V_{\rm gs}^{(1)} + (\eta - 1) V_{\rm th}^{(1)} - \eta V_{\rm th}^{(2)} - 0.5 V_{\rm ds}$. The inversion gate-oxide capacitance $C_{\rm ox}$, the channel length $L_{\rm eff}$, and the channel width $W_{\rm eff}$ are cancelled out because they are identical for a single device. This unique property makes the proposed method particularly favorable for the short-channel devices in which an unambiguous definition of $C_{\rm ox}$, $L_{\rm eff}$, and $W_{\rm eff}$ is difficult to achieve.

IV. Results and Discussion

In this letter, the state-of-the-art low-power devices featuring 17.5-Å (effective oxide thickness) gate oxide and heavily doped source/drain extensions (S/D-exts) are utilized. The devices underwent advanced strain engineering involving a neutral shallow-trench-isolation gap-fill process, a stress memorization technique [13], and a tensile contact etch-stop layer. A millisecond anneal process was also employed to improve device performance.

Experimental demonstration with a mask gate length $L_{\rm mask}$ of 100 nm is presented here. In order to obtain a constant carrier mobility under different bias conditions, a sufficiently high $E_{\rm eff}$ (high $V_{\rm gs}$) is necessary to force the carrier mobility to converge toward the universal curve. When $E_{\rm eff}$ is insufficiently high, the carrier mobility does not converge even under the same $E_{\rm eff}$. The extracted $R_{\rm sd}$, as shown in the low $E_{\rm eff}$ region in Fig. 2, shows anomalous values as well as a strong dependence on the $V_{\rm bs}$ bias. This undesired result is due to the failure of the constant-mobility conditions. As we further increase $E_{\rm eff}$, the electron mobility begins to converge toward the universal curve. Consequently, the extracted $R_{\rm sd}$ values approach a constant, and no dependence on the $V_{\rm bs}$ bias can be observed, as shown in the high $E_{\rm eff}$ region in Fig. 2. In this letter, the gate current is at least six orders of magnitude lower than the drain–current under all bias conditions because the tunneling current is limited by the gate area of the short-channel device. Hence, the gate current has a negligible effect on the $R_{\rm sd}$ extraction.

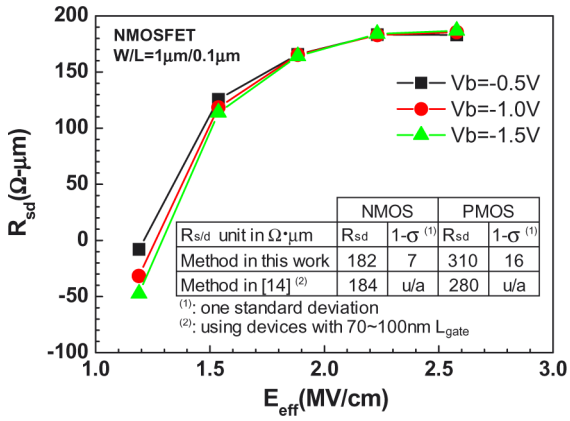

Fig. 2. Extracted $R_{\rm sd}$ as a function of $E_{\rm eff}$. Erroneous $R_{\rm sd}$ values appear in the low $E_{\rm eff}$ region because the $E_{\rm eff}$ is insufficiently high and the "constant-mobility" criterion is not satisfied. $R_{\rm sd}$ approaches a constant and exhibits no dependence on $V_{\rm bs}$ in the sufficiently high $E_{\rm eff}$ region. The inset shows the $R_{\rm sd}$ values extracted from the proposed method in this letter and the method in [14]. A good agreement is achieved.

The proposed method has also been applied to both NMOSFETs and PMOSFETs. The inset in Fig. 2 lists some of the extracted $R_{\rm sd}$ values. Also shown for comparison are those extracted from a considerable number of devices using BSIM simulation [14]. A reasonable agreement is achieved between the two methods.

In Fig. 3, an obvious degradation in driving capability is observed when external resistors are additionally connected to the device under test. The $R_{\rm sd}$ and these external resistors are extracted using the proposed method. The $R_{\rm sd}$ values faithfully reflect the presence of the external resistors, as shown in the inset of Fig. 3. Therefore, this proposed method is well qualified. A SPICE model is calibrated using the extracted $R_{\rm sd}$ in the case of "$R_{\rm ext} = 0$." The simulated data match the measurement. The quality of the SPICE model is therefore verified. Without modifying any parameters, the simulated data further match the measurement in both cases of "$2R_{\rm ext} = 102\ \Omega$" and "$2R_{\rm ext} = 200\ \Omega$." Obviously, $R_{\rm sd}$ and $R_{\rm ext}$ are additive to each other. Hence, any difference in $R_{\rm sd}$ caused by process change can be extracted by this proposed method.

Since the surface potential is modulated by $V_{\rm bs}$, the centroid of the carrier distribution (Z_c) changes accordingly [15]–[17]. Fig. 4 shows the inversion-layer carrier distribution, which is calculated using 2-D numerical simulators, namely,

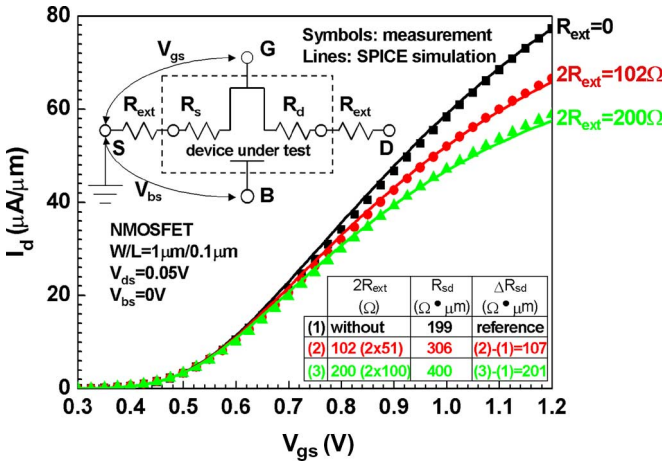

Fig. 3. Measured and simulated I_d–$V_{\rm gs}$ characteristics of a typical NMOSFET with $W_{\rm mask}/L_{\rm gate} = 1\ \mu{\rm m}/0.1\ \mu{\rm m}$ under $V_{\rm ds} = 0.05$ V. External resistors $R_{\rm ext}$ are connected to the device, as shown in the inset. The extracted $R_{\rm sd}$ values, listed in the inset, faithfully reflect the presence or absence of the $R_{\rm ext}$.

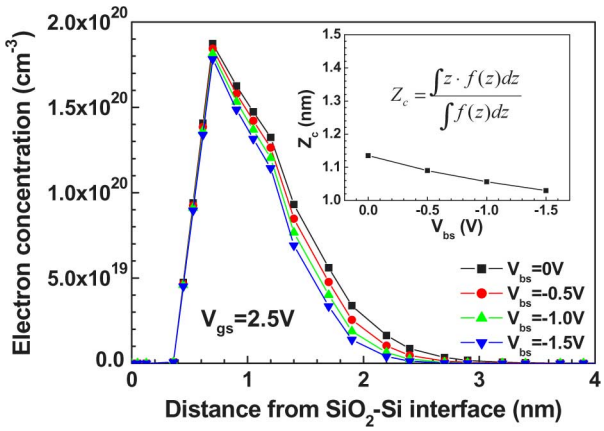

Fig. 4. Inversion-layer electron density distribution f, which is calculated using the 2-D numerical simulators, namely, TSUPREM4 and MEDICI, normal to the channel surface under various $V_{\rm bs}$ conditions. The inset shows the centroid of the carrier distribution (Z_c). When $V_{\rm bs}$ changes from 0 to -1.5 V, Z_c decreases by only $\sim$0.1 nm which is equivalent to $\sim$0.03-nm decrease in $T_{\rm ox\_inv}$. This change should have a negligible effect on the $R_{\rm sd}$ extraction proposed in this letter.

TSUPREM4 and MEDICI, normal to the channel surface. As $V_{\rm bs}$ changes from 0 to -1.5 V, Z_c decreases by $\sim$0.1 nm which is equivalent to $\sim$0.03-nm change in the inversion-oxide thickness $(T_{\rm ox\_inv})$. This difference is no more than 1.5% for the aggressively scaled oxide down to 2-nm $T_{\rm ox\_inv}$. This effect on the extracted $R_{\rm sd}$ should be negligible.

Finally, for the advanced MOSFET technology, shallow and heavily doped S/D-ext regions are widely used. The dopant concentration inside the S/D-ext is often higher than 10^{20} cm^{-3} with a sharp dopant transition ($<$ 3 nm/dec, which is not shown in this letter) toward the substrate and the surface channel regions. The modulation of carrier concentration caused by high $V_{\rm gs}$ and/or high $V_{\rm bs}$ is insignificant inside the S/D-ext, leading to an insignificant change in $R_{\rm sd}$.

V. Conclusion

The extraction of series resistance for the short-channel MOSFET, with the heavily doped S/D-ext regions, using simple dc measurements without knowing $C_{\rm ox}$, $L_{\rm eff}$, $W_{\rm eff}$, and the carrier mobility has been demonstrated. Compared with many previous methods that need several devices in the $R_{\rm sd}$ extraction, this new method requires only a single device and can eliminate the uncertainty arising from process instabilities among devices. Hence, it provides immunity against process variation, which is a major issue as the physical device dimensions shrink. These merits make the new method particularly favorable for the short-channel devices.

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