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2007 Semicond. Sci. Technol. 22 1352

(http://iopscience.iop.org/0268-1242/22/12/020)

Semicond. Sci. Technol. **22** (2007) 1352–1361 doi:10.1088/0268-1242/22/12/020

TiO_2/GeO_xN_y stacked gate dielectrics for Ge-MOSFETs

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Received 10 May 2007, in final form 11 October 2007
Published 19 November 2007
Online at stacks.iop.org/SST/22/1352

Abstract

In this work, we present the results of physical and electrical characterization of Ti-based high-*k* gate dielectrics on Ge substrates. Titanium tetrakis isopropoxide (TTIP) was used as the organometallic source for the deposition of ultra-thin TiO_2 films on p-Ge (1 0 0) at low temperature (<200 °C) by plasma enhanced chemical vapor deposition (PECVD) technique in a microwave (700 W, 2.45 GHz) plasma cavity discharge system at a pressure of ∼65 Pa. The presence of an ultra-thin lossy GeO_2 interfacial layer between the deposited high-*k* film and the substrate, results in frequency-dependent capacitance–voltage (*C*–*V*) characteristics in strong accumulation and a high interface state density ($\sim 10^{13}$ cm^{-2} eV^{-1}). To improve the electrical properties, nitrogen engineering has been employed to convert the lossy GeO_2 interfacial layer to its oxynitride, thus forming $TiO_2/GeO_xN_y/Ge$ stacked-gate structure with improved interface/electrical properties. Different N sources, such as NO, NH_3 and NO/NH_3, have been used for nitrogen engineering. XPS and Raman spectroscopy analyses have been used for surface morphological study. Electrical properties, such as gate leakage current density, interface state density, charge trapping, flatband voltage shift, etc, have been studied in detail for $TiO_2/GeO_xN_y/Ge$ MIS capacitors using the current–voltage (*I*–*V*), capacitance–voltage (*C*–*V*), conductance–voltage (*G*–*V*) and stress (both constant voltage and current) measurements. Although a significant improvement in electrical characteristics has been observed after nitridation in general, the formation of the interfacial GeO_xN_y layer, obtained from NO-plasma nitridation, is found to provide the maximum improvement among all the nitridation techniques used in this study. It is shown that the insertion of an ultra-thin oxynitride (GeO_xN_y) interfacial layer is advantageous for producing gate-quality TiO_2 high-*k* dielectric stacks on Ge substrates.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Over the past four decades, by reducing MOS transistor gate length, steady improvements in circuit performance (speed) and cost per function have been achieved. However, continued transistor downscaling will not be as straightforward in the future as it has been in the past because fundamental materials and process limits are rapidly being approached [1]. Shrinking

MOSFET beyond the 45 nm technology node and below will require innovations to circumvent the fundamental limitations. Further scaling will necessitate the introduction of high-*k* gate materials, at the expense of the channel mobility. To overcome the degradation of the mobility, advanced MOSFET devices will require high-mobility substrates (SiGe, strained-Si, Ge etc) [2]. Successful materials and process selection will require an in-depth understanding of the gate stack structures from the viewpoints of physics and chemistry as well as semiconductor manufacturing. It is important to examine combinations of novel high-mobility channel materials and high-*k* gate dielectrics in order to improve the performance. The proper choice of gate stack materials should permit control of gate leakage current density, avoid gate poly-silicon depletion in order to reduce the effective oxide thickness (EOT) of the stack and define the threshold voltage without the need for heavy channel ion implants which degrade carrier mobility of both n- and p-MOSFETs.

Historically, the first transistor operation was demonstrated on Ge. A prime candidate for high-mobility channel material would be Ge because of its mobility, as high as 1900 or 3900 $cm^2\ V^{-1}\ s^{-1}$ for holes and electrons, respectively. Also, there is a growing interest in designing and fabricating high-speed low-temperature MOSFETs for high-speed cryogenic applications such as read-out electronics for cooled infrared detectors, fast processors and low noise amplifiers. To this end, a Ge channel device structure which can be operated in the temperature range from room temperature (300 K) down to cryogenic temperature ($<T = 77$ K) while having even higher transport characteristic is the ideal solution.

Although the development of high-performance transistors in Ge wafers has been reasonably successful so far, many issues must be resolved, before it can be integrated successfully in conventional Si CMOS processing. Due to the smaller band gap and higher dielectric constant, devices suffer from large leakage currents and worse short channel effects, although smaller energy band gap allows device voltage (V_{DD}) scaling. Ultra-thin high-*k* dielectric layers are necessary for fabrication of MOSFETs on Ge substrates that may replace silicon in future transistor devices. The compatibility and fabrication of a Ge-channel MOSFET using existing Si technology is also important. On Ge, the gate dielectrics investigated so far, ZrO_2 and HfO_2, have dielectric constants in the range 20–30 and are thermodynamically stable [3].

In this paper, we have deposited ultra-thin TiO_2 films on p-Ge (1 0 0) substrates at low temperature (<200 °C) by microwave plasma enhanced chemical vapor deposition technique. The feasibility of the formation of device-quality high-*k* TiO_2 gate dielectrics is studied in bulk Ge. We have studied the effects of an oxynitride interfacial layer on electrical properties of TiO_2/Ge MIS capacitors using PECVD deposited high-*k* dielectrics. The effectiveness of different N sources, such as NO, NH_3 and NO/NH_3 for the insertion of N in gate stack structures using plasma nitridation technique has also been studied. Electrical properties, such as gate leakage current density, interface state density, charge trapping, flat band voltage shift, etc, have been studied in detail for TiO_2/GeO_xN_y/Ge MIS capacitors using the current–voltage (*I–V*), capacitance–voltage (*C–V*), conductance–voltage (*G–V*) and stress (both constant voltage and current) measurements and the results are presented.

2. Experimental section

The Ge substrate (1 0 0) used was B-doped p-type wafers with a resistivity of 25–29 Ω cm. Before the dielectric deposition on Ge substrates, it is necessary to remove the native oxide present [4]. However, the cleaning of Ge substrate is very challenging. Conventional wet cleaning, such as (H_2O_2 + HF) [5], cyclic HF (1:50 diluted HF solution) dip with DI water rinsing, ammonium hydroxide solution, etc, cannot completely remove the native GeO_2 rather, it helps to grow. Therefore, in the present experiment, we have used a dry chemical process reported for Ge-substrate cleaning [6]. Ge substrates were held in the highly concentrated HF vapor for 5–10 s prior to loading in the deposition chamber. Growth of high-*k* gate dielectric layers on hydrophobic Ge (1 0 0) requires a novel processing method. High-*k* gate dielectrics are sufficiently stable compared to GeO_2, that they may prevent formation of a low-*k* GeO_2 layer between the deposited dielectric and the Ge (1 0 0) surface which is a key requirement for use of the high-*k* dielectrics in Ge MOSFETs.

In this study, we have deposited TiO_2 films using titanium tetrakis iso-propoxides (TTIP) ($Ti(OC_3H_7)_4$), as a metal–organic precursor in a microwave (700 W, 2.45 GHz) plasma cavity discharge ($0.37 \times 0.37 \times 0.26$ m^3) system at a pressure of 66.67 Pa for 90 s. TTIP precursors were kept at 45 °C temperature. No external biasing or heating of the substrate was employed, although plasma discharge itself raised the substrate temperature to about 150 °C. A reaction stoichiometry for the formation of gaseous TiO_2 is as follows:

$$Ti(OC_3H_7)_4 \quad \Rightarrow \quad TiO_2 + 4C_3H_6 + 2H_2O\,. \qquad (1)$$

The film thickness was estimated to be ∼15.0 nm (EOT ∼3.07 nm). Before the TiO_2 deposition, a few samples were treated with NO, NH_3 and NO/NH_3 plasma for the oxynitride formation. The as-deposited film has been studied by Raman spectroscopy for chemical characterization and surface by atomic force microscopy (AFM). For electrical measurements, metal–insulator–semiconductor (MIS) capacitors were formed using the TiO_2/GeO_xN_y/Ge stacked dielectric films, by evaporating circular Al metal contacts (area: 0.196 mm^2, thickness: 100–200 nm) through a shadow mask. The *C–V*, *G–V* and *I–V* characteristics were measured using an HP-4061A semiconductor test system. Charge trapping/detrapping characteristics were studied by applying dc stresses in a constant current and voltage mode by the HP-4145B parameter analyzer.

3. Results and discussion

3.1. Chemical characterization

3.1.1. XPS analysis. The high-resolution XPS measurements were performed under UHV (below 2×10^{-9} mbar) at room temperature. All data were recorded at a 45° take-off angle which is in normal emission geometry. Excitation energy was 1486.7 eV (monochromatic Al K_α source was used for this purpose). Photoelectrons were energy separated by using a Scienta ESCA300 hemispherical analyzer with a pass energy of 50 eV and an instrumental resolution of 0.6 eV measured at full-width-at-half-maximum (FWHM) of the Ag $3d_{5/2}$ photoelectron peak. The energy position of the peaks

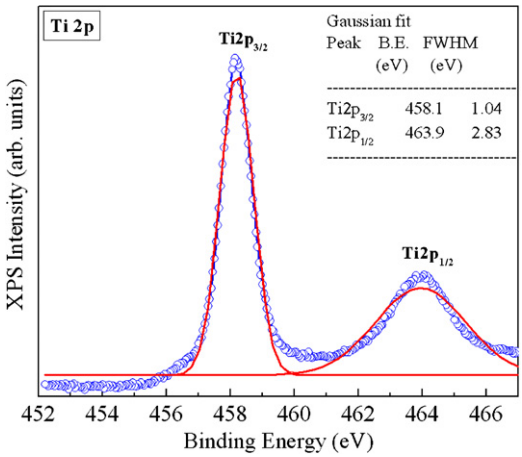

Figure 1. High-resolution deconvoluted XPS of Ti 2p spectra of deposited TiO_2 films on p-Ge (1 0 0). XPS was performed at a take-off angle of 45° between the analyzer axis and the plane of the wafer.

was determined with an accuracy of 0.1 eV. The binding energies (E_b) have been corrected for the sample-charging effect with reference to the C 1s peak (284.5 eV) observed at the surface. All the spectra were fitted with Gaussian functions and the background was removed by the Shirley background subtraction method.

The XPS chamber, equipped with an ion source, was used for *in situ* sputtering of the sample by Ar^+ to investigate the concentration profiles of various species. In order to obtain information on the composition of the layers, both in depth and from the interface transition region, depth profile spectra were taken. The sputter profiling of the films was accomplished using an argon ion beam with an energy of 3 keV, projected perpendicular to the sample surface and the sputter current maintained was maintained at ∼1.6 μA. The chamber pressure was kept at 1×10^{-6} mbar during sputtering.

In figure 1, Ti $2p_{3/2}$ and Ti $2p_{1/2}$ peaks are observed at binding energies of 458.1 eV and 463.9 eV, respectively, which represent the fully oxidized values of Ti, i.e. Ti^{4+} [7]. To analyze the chemical bonding nature and stiochiometry of deposited oxides, Ti 2p signals were further analyzed. A two-Gaussian peak (line shape function) like $f(E)$ is used to deconvolute XPS spectra of Ti 2p:

$$f(E) = y_0 + \frac{A_1}{\omega_1}\sqrt{\frac{4\ln 2}{\pi}}\exp\left[\frac{-4\ln 2(x - x_{c1})^2}{\omega_1^2}\right] + \frac{A_2}{\omega_2}\sqrt{\frac{4\ln 2}{\pi}}\exp\left[\frac{-4\ln 2(x - x_{c2})^2}{\omega_2^2}\right] \quad (2)$$

where y_0 is the offset of the function in the y-direction, A_1 and A_2 are the areas under the Gaussian peaks respectively, x_{c1} and x_{c3} are the positions of the peaks respectively, and ω_1 and ω_2 are the FWHM of the lineshape. The best fitting parameters are $y_o = 6359.31 \pm 62.23$; $x_{c1} = 458.1 \pm 0.02$ eV, $x_{c2} = 463.9 \pm 0.03$ eV; $A_1 = 25538.29 \pm 70.8$; $A_2 = 19873.73 \pm 73.9$; $\omega_1 = 1.04 \pm 0.01$ eV and $\omega_2 = 2.83 \pm 0.07$ eV.

Core-level Ge 2p and O1s X-ray photoelectron spectra as shown in figures 2(*a*) and (*b*) were taken at different etching conditions for the etch time between 15 to 35 min. It is seen that at no-etch condition, the peak intensities for O 1s at

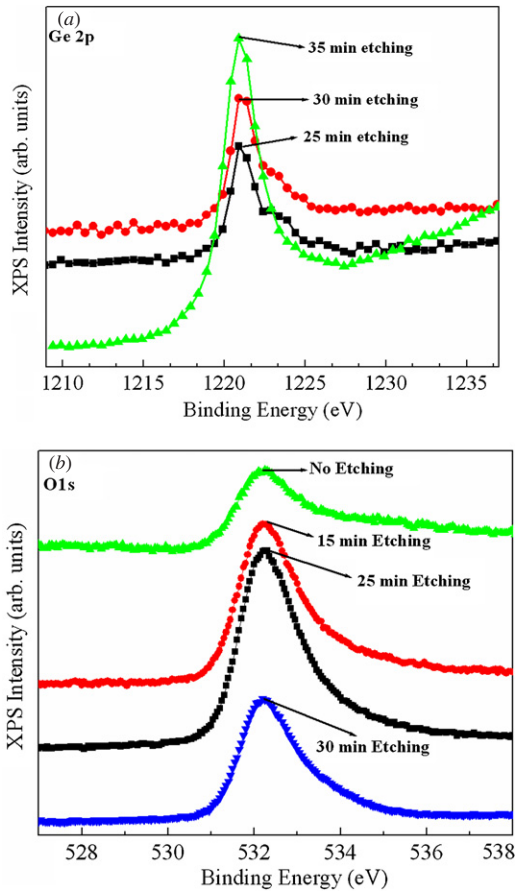

Figure 2. XPS of (*a*) Ge 2p and (*b*) O 1s spectra for different etching conditions.

532.2 eV due to O^{n+} state are much stronger than those after etching. However, the peak intensity detected at 1220.9 eV due to Ge^{n+} state increases with the etching time. Since no signal was observed for metallic Ge or Ge–Ti bond, it indicates that the dielectric film is composed of both GeO_2 and TiO_2. Similar film composition has been observed for the TiO_2 films deposited by other techniques on the Ge substrate without any interface treatment [8, 9].

The physical characterization of the oxynitride films prepared by plasma discharge was carried out to inspect the chemical bonding state of N atoms at the interface and their chemical stability. The deconvoluted N 1s spectra of NO-plasma treated oxinitide sample is shown in figure 3(*a*). Two N 1s peak associated with Ge ≡ N bond at 397.4 eV and Ge_2 = N–O at 399.4 eV are observed. But during etching, there is a significant increase in N 1s peak intensity (figure 3(*b*)) with increasing etching time, i.e., with the increasing depth toward the oxide/p-Ge interface. However, the results of the oxide composition in atomic percentage determined from the corresponding XPS intensities for NO-plasma treated nitrided sample are shown in table 1.

3.1.2. Raman spectroscopy analysis. Figure 4 shows the Raman spectra of the Ge substrate and the deposited TiO_2 films. Raman spectra were registered in a backscattering geometry using the micro-Raman Renishaw 1000 system equipped with a Leica microscope. The excitation wavelength

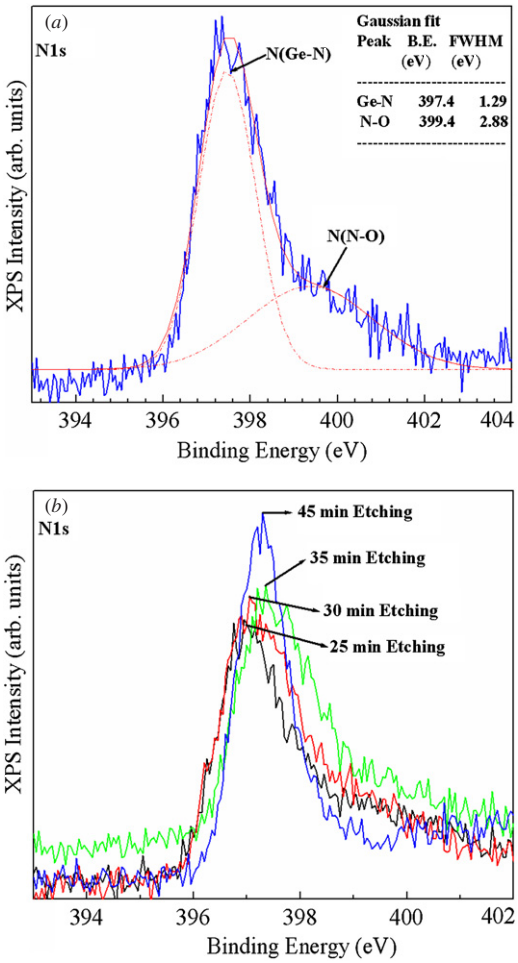

Figure 3. XPS of (*a*) deconvoluted and (*b*) comparison of several N 1s spectra for different etching conditions.

Table 1. Oxide composition obtained from the Ge 2p, N 1s, O 1s and C 1s photoelectron intensities. The first column shows the sputtering time. The second columns refer to relative atomic concentration, while the relative sub-columns indicate the percentage of each element in the oxide.

Sputtering time (min)	Relative atomic concentration (at.%)			
	%O	%N	%Ge	%C
25	51.2	16.9	27.6	2.1
30	44.1	17.4	31.4	1.4
35	41.2	19.2	32.1	1.1

was 514.5 nm from an Ar^+ ion laser with a typical laser power level of ∼180 mW. Relatively slow scan speeds were employed in order to achieve high-spectral/noise ratios. The spectra of each specimen were taken three times over the range 100–900 cm^{-1}, scanning at 1.0 cm^{-1} step size with an integration time constant of 1 s. The observed Raman peak at 301.6 cm^{-1} for Ge substrate is due to the Ge–Ge stretching mode and the peak at 518.3 cm^{-1} is due to the Ti–O stretching mode vibration. The experimental Raman peaks agree well with the results reported in [10, 11].

3.2. Electrical characterization

3.2.1. Dielectric-substrate interface analysis. The measured *C–V* characteristics (100 kHz–1 MHz) for non-nitrided and

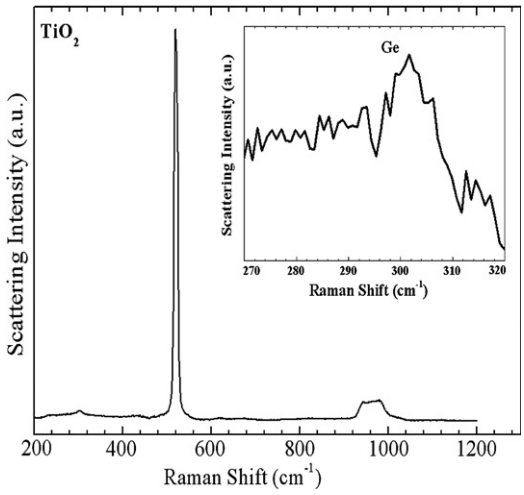

Figure 4. Raman spectra of Ge substrate and deposited-TiO_2 film.

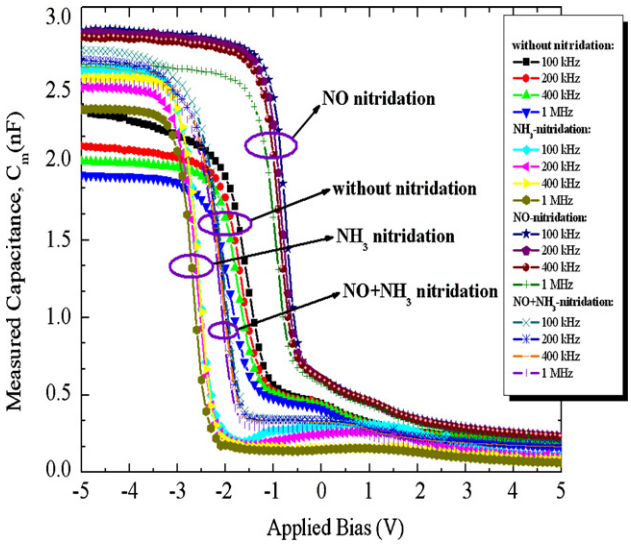

Figure 5. Measured frequency dispersion (100 kHz, 200 kHz, 400 kHz and 1 MHz) in capacitance–voltage characteristics of non-nitrided and nitrided Ge MIS capacitors.

nitrided Ge MIS capacitors, as shown in figure 5, exhibit high-frequency dispersion in the accumulation and depletion regions. It can be observed that the *C–V* dispersion in the depletion region stretches out along the voltage axis which is due to the presence of both acceptor and donor such as slow interface states in the semiconductor band gap [12, 13]. However, after nitridation under plasma discharge in several N sources, it is interesting to note that the *C–V* stretches toward more negative bias to that of the non-nitrided sample for the NO/NH_3 and NH_3-plasma treated oxynitride sample, whereas NO-plasma treated sample exhibits positive voltage shift. NH_3-plasma treated nitrided samples show significant dispersion in the inversion region as the frequency is reduced, indicating the presence of slow interface states. Similar dispersion was also observed by Dimoulas *et al* [14] in the inversion region on the p-type substrate after the Ge surface was treated with O and N beams. But no dispersion was observed in the inversion region for both non-nitrided and NO or NO/NH_3-plasma treated nitrided samples. In fact, the

high-intrinsic minority carrier concentration of Ge, i.e. n_i is mainly responsible for the observed dispersion in the inversion region. However, there is other possibility that NH_3 surface nitridation creates additional slow interface states due to H-related trapping centers, deep in bandgap that does not exist in non-nitrided or NO/NH_3-plasma treated samples [15, 16]. An increase in the accumulation capacitance of nitrided samples by a factor of ∼1.4 at high-frequency compared to non-nitrided samples implies that surface nitridation enhanced the quality of titanium oxide deposited and/or possibly helped in restricting the growth of the interface layer [17].

Furthermore, non-nitrided and NH_3-plasma nitrided samples showed dispersion in the accumulation region as a function of frequency. Normally, the measured capacitance in the accumulation region should be independent of signal frequency. Several explanations may be put forward for the observed decreasing capacitance. A possible explanation for this occurrence may be due to leakage current which decreases the total accumulation charges. But this is uncertain, as the decrease in accumulation charge causes a decrease in measured capacitance, and hence the dc leakage current should saturate. However, saturation has not been observed in dc leakage measurements.

The second possibility could be the inability of the LCR meter to accurately measure the capacitance, if the oxide conductance becomes too large. During high-frequency measurements, the impact of series resistance makes it difficult to estimate the correct effective oxide thickness (EOT). Series resistance effect is normally observed when the conductance of gate oxide becomes comparable with the conductance associated with series resistance. This will cause erroneous data from the LCR meter. Thus, a dissipation factor (D) may be used to check the accuracy of the measurement, using measured capacitance (C_m) and conductance (G_m) at a particular frequency: $D = \frac{G_m}{2\pi f C_m}$ [18]. An approximated instrumentation error for LCR meters is given as % error $= 0.1\sqrt{(1+D^2)}$. The instrumental error, in our measurements, is less than 1% across the whole applied bias range for all frequencies. Therefore, the decrease in capacitance cannot be explained as an instrumental error. The above considerations imply that C_m–f variation (not shown) can be attributed due to the presence of an ultra-thin lossy GeO_x interfacial layer. As GeO_x is filled with traps, this causes the dielectric layer to be highly frequency dependent. In order to accurately model the effect of this lossy dielectric layer, along with an ideal MOS capacitor, an equivalent circuit, as shown in figure 6(*a*), is required [19]. By comparing the imaginary and real parts of the impedance, after certain algebraic manipulations, one can obtain the corrected capacitance, C_c, and conductance, G_c, as

$$C_c = \frac{(C_e)\left(\omega^2 C_m C_e - G_m^2 - \omega^2 C_m^2\right)\left(G_m^2 + \omega^2 C_m^2\right)}{\left(\omega^2 C_e^2\right)\left[G_m(1 - R_s' G_m) - \omega^2 R_s' C_m^2\right]^2 + \left(G_m^2 + \omega^2 C_m^2 - \omega^2 C_m C_e\right)^2} \quad (3)$$

and

$$G_c = \frac{\left(\omega^2 C_e^2\right)\left(G_m^2 + \omega^2 C_m^2\right)[G_m(1 - R_s' G_m)]}{\left(\omega^2 C_e^2\right)\left[G_m(1 - R_s' G_m) - \omega^2 R_s' C_m'\right]^2 + \left(G_m^2 + \omega^2 C_m^2 - \omega^2 C_m C_e\right)^2} \quad (4)$$

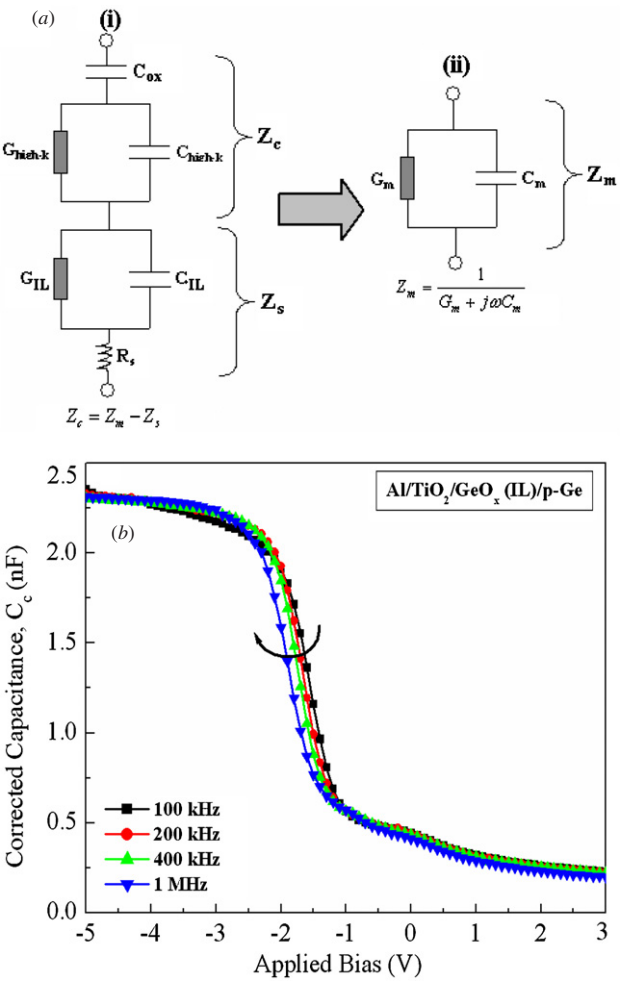

Figure 6. (*a*) Equivalent circuit model in accumulation region including the effect of thin lossy interfacial dielectric layer with complete impedance, Z and R_s, and equivalent parallel impedance, Z_{eq} and (*b*) reconstructed C–V characteristics of Al/TiO_2-IL (GeO_2)/p-Ge MIS capacitor.

where C_e is the equivalent capacitance due to presence of a lossy dielectric layer which can be expressed with G_{IL} and C_{IL} connected in parallel as

$$C_e = \frac{G_{IL}^2 + \omega^2 C_{IL}^2}{\omega^2 C_{IL}}. \quad (5)$$

Here, R_s' represents the modified series resistance due to inclusion of an interfacial dielectric layer. C_m and G_m are the measured capacitance and conductance, respectively and ω is the angular frequency. The expressions in equations (3) and (4) represent the correction formulae that are subsequently used to reconstruct the intrinsic capacitance values from the measured capacitance and conductance of lossy MOS capacitors. Figure 6(*b*) shows the corrected plot of C–V characteristics obtained after applying the above mentioned model for C_c (equation (3)) which is free from accumulation dispersion.

The study of the oxide–semiconductor interface is extremely important, since the presence of the oxide traps significantly affects the MOSFET performance. The interface state density is calculated using the technique proposed by Terman [20]. The C–V characteristic is also compared with

Table 2. A comparison of electrical parameters for several high-k dielectrics on Ge.

Insulator–semiconductor	EOT/CET (nm)	Interface state density (eV^{-1} cm^{-2})	Leakage current density (A cm^{-2} at ±1 V)	Q_f/q (cm^{-2})	Reference
ZrO_2/Ge	∼0.8	$\sim 1 \times 10^{12}$	2.3	–	[3]
HfO_2/Ge	4.5 (physical)	$\sim 5 \times 10^{12}$	$\sim 2 \times 10^{-3}$	–	[16]
GeO_xN_y/Ge	1.16–1.9	$\sim 8 \times 10^{12}$–3×10^{12}	0.65	1.0×10^{12}	[24]
HfO_xN_y/Ge	1.95	–	1.8×10^{-5}	–	[25]
Al_2O_3/Ge	∼1.7	$\sim 2 \times 10^{12}$	$\sim 2 \times 10^{-3}$	–	[26]
HfO_2/ GeO_xN_y/Ge	∼1.3	$\sim 2 \times 10^{12}$–5×10^{12}	$\sim 4 \times 10^{-3}$	–	[26]
TiO_2/GeO_2/Ge	2.8	$\sim 5.0 \times 10^{13}$	5.4×10^{-3}	1.4×10^{13}	This work
TiO_2/GeO_xN_y/Ge (NH_3 treated)	2.6	$\sim 3.9 \times 10^{13}$	1.1×10^{-6}	2.1×10^{13}	This work
TiO_2/GeO_xN_y/Ge (NO treated)	2.3	$\sim 6.2 \times 10^{12}$	1.4×10^{-5}	1.2×10^{13}	This work
TiO_2/GeO_xN_y/Ge (NO+NH_3 treated)	2.4	$\sim 2.2 \times 10^{13}$	9.3×10^{-5}	1.9×10^{13}	This work

the ideal C–V characteristics without interface states. The capacitance is not influenced by the ac voltage at a high frequency in the presence of interface states because of the time constant for trapping of interface states is very large compared to the period of ac excitation voltage, when the bias voltage variations charge or discharge these states. The charge, qD_{it} generated by interface states limit the capacitance variation with the gate voltage C (V_G), and this charge can be calculated using the additional gate voltage ΔV_g developed through the capacitance C_{ox}:

$$q D_{it} = C_{ox} \frac{d(\Delta V_g)}{d\psi_s} \tag{6}$$

where D_{it} is the interface states density, ψ_s is the surface potential and ΔV_g is the experimental voltage shift relative to the ideal high-frequency characteristics. The voltage shift is given by $\Delta V_g = (V_g)_{measured} - (V_g)_{ideal}$. However, in order to get the energy distribution of the density of interface states D_{it} ($E_c - E_{it}$), one has to transform the surface potential variations into the energy ($E_c - E_{it}$) by means of the following relation:

$$E_c - E_{it} = \frac{E_g}{2} + q(\psi_s - \phi_b) \tag{7}$$

where E_g is the energy gap and, ϕ_b is the bulk potential defined by the difference between the actual and the intrinsic Fermi levels.

Figure 7 shows the extracted D_{it} as a function of energy for both non-nitrided and nitrided samples. The energy axes (i.e., x-axes) were labeled with the convention that 0.0 V represents the midgap position (E_i); a positive potential samples the upper half of the bandgap toward the conduction band edge (E_C) and a negative value explores the lower half of the bandgap toward the valence band edge (E_V). The D_{it} level for non-nitrided sample was around 7×10^{13} cm^{-2} eV^{-1}. After surface nitridation treatment, the D_{it} level dropped approximately by a factor of 10 to roughly 6×10^{12} cm^{-2} eV^{-1} for the NO-plasma treated nitrided sample. D_{it} in nitrided samples seems to be more widely distributed in the Ge bandgap as compared to non-nitrided samples as shown in figure 7.

The interface state distribution in the non-nitrided case is due to the possible detection of fast interface states that were reduced for nitrided devices. Also, interface states in nitrided devices are located deeper in Ge bandgap than non-nitrided Ge-MIS devices. The concentration of deep interface states in nitrided devices in the bandgap is higher than that of

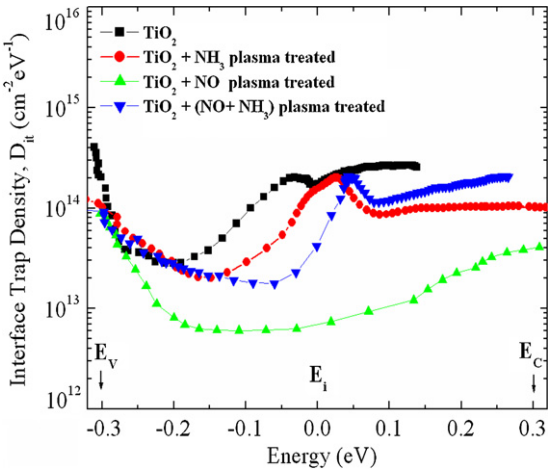

Figure 7. A comparison of energy distribution of density of interface states for both non-nitrided and nitrided samples.

the maximum D_{it} estimated for non-nitrided devices. This suggests the presence of slower interface traps in nitrided devices. It has been reported earlier that formation of GeO_xN_y instead of GeO_x improves the EOT and hysteresis because of the reduced growth of the interfacial layer (IL) with a lower dielectric constant [21]. It is also believed that nitrogen incorporation at the interface suppresses Ge diffusion into the IL and diffusion of O_2 to the Ge surface, thereby limiting the growth of GeO_x at the interface [22]. Lower EOT and a low hysteresis were observed for nitrided devices compared to non-nitrided devices. However, D_{it} behavior indicates that slow states are present in the interface layer assuming minimal contribution from Ge dangling bonds [23]. This can be attributed to either the surface preparation prior to nitridation and/or nitridation condition and temperature. The electrical properties of different deposited high-k materials on Ge are compared in table 2 [24–26].

3.2.2. Influence of charge trapping under constant current stressing. The study of traps in insulators is extremely important since the presence of the oxide traps significantly affects the MOSFET performance. Thus, the origin of oxide traps should be investigated in order to control the oxide traps. In the following, we present the charge-trapping characteristics

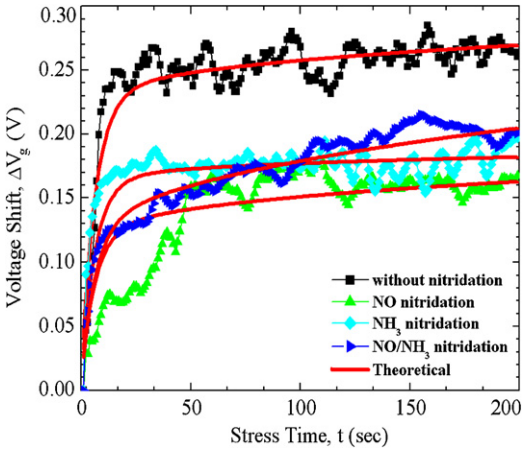

Figure 8. A comparison of stress time dependent gate voltage shift (ΔV_g) observed during constant current stressing at -10.2 mA cm^{-2} for 200 s for both nitrided and non-nitrided samples. (Solid line-fit using 12).

of microwave plasma grown high-k TiO_2 gate dielectric on p-Ge investigated by constant current stressing. The charge trapping behavior of the samples studied by continuously monitoring the change in the gate voltage (ΔV_g) required to maintain a constant current of -10.2 mA cm^{-2} under substrate injection is shown in figure 8. The stress-induced gate voltage of MIS capacitors is shifted to the positive direction for all non-nitrided and nitrided films, indicating the presence of electron traps rather than hole traps. It can be noted that the value of the positive voltage shift drastically dropped after nitridation. From this observation, it is clear that the non-nitrided sample generates traps at a faster rate than nitrided samples. The concentration of trap charges is also lower for nitrided samples. This is expected because nitrogen incorporation forms a buffer layer, which comprises of Ge≡N bonds within the first 1 nm from the interface and Ge=O–N bonds outside this region [27].

The presence of strong Ge≡N bonds in place of Ge–O bonds makes trap generation less likely in the nitrided sample. However, NH_3-plasma treated nitrided sample shows a higher level of electron trapping compared to NO or NO/NH_3-plasma treated nitrided samples. As has been stated earlier that the presence of H-related species such as Ge–H bonds can trap electrons which is responsible for higher electron trapping in the NH_3-treated sample. Furthermore, NO-plasma treated nitrided sample enhances the incorporation of N and results in a decrease of H-related bonds/traps and an increase of Ge≡N bonds, leading to lower electron trapping. This lower gate voltage shift occurs because of combined effect of reduced electron trapping and positive charge due to slow donor type states.

In order to simulate ΔV_g versus t curve, we have incorporated electron-fluence-dependent voltage equation for the electron trapping model [28]. The trapping kinetics is described by a first-order rate equation [13, 29] as

$$\frac{dN_t}{dt} = n v_t \sigma_t (N_{ot} - N_t) \tag{8}$$

where N_t is the filled trap density, N_{ot} is total trap density, n is conduction-band electron density, σ_t is the trap capture cross section and v_t is the thermal velocity of electron. Solving above equation, one can express it as follows:

$$N_t(N_{inj}) = N_{ot}[1 - e^{-\langle\sigma_t\rangle N_{inj}}] \tag{9}$$

where $\langle\sigma_t\rangle = \int_0^t \frac{J_{inj}\sigma_t v_t}{qN_{inj}v_d}\,dt$; $\langle\sigma_t\rangle$ is the average capture cross-section of oxide traps, v_d is the drift velocity of electron, J_{inj} is the constant injected current density and $N_{inj} = \int_0^t \frac{J_{inj}}{q}\,dt$ is the injected charge density. Now, applying Gauss's law and combining the flat-band voltage shift, ΔV_{fb}, and anode field shift, ΔE_a, caused by the trapped electron, one obtains electron-fluence-dependent voltage equation as

$$\Delta V_g = \sum_i \frac{qN_{ot,i}X_t}{\varepsilon_o\varepsilon_{hk}} \times \left[1 + \frac{2kT}{qE_o}\left(\frac{1}{X_t} - \frac{1}{t_{stack}}\right)\right] \cdot [1 - e^{-\langle\sigma_t\rangle_i N_{inj}}]. \tag{10}$$

Again the variation of surface potential, $\Delta\psi_s$, does not affect the capture cross-section measurement and it is also not sensitive to determine effective trap density. Hence, the above equation may be simplified as

$$\Delta V_g \cong \sum_i \frac{qN_{ot,i}X_t}{\varepsilon_o\varepsilon_{hk}}[1 - e^{-\langle\sigma_t\rangle_i N_{inj}}]. \tag{11}$$

But the above theoretical equation is not sufficient to fit experimental results as shown in figure 8 (solid line). The solid line in figure 8 is fitted to the experimental data points using the following equation:

$$\Delta V_g = A\sum_i \frac{qN_{ot,i}}{C_{ox}}[1 - e^{-\langle\sigma_t\rangle_i N_{inj}}] + \gamma t^{\delta} \tag{12}$$

(as $X_t/\varepsilon_o\varepsilon_{hk} \approx C_{ox}^{-1}$, C_{ox} being accumulation capacitance). The second term takes into account the power-law-dependent stress-induced voltage shift (SIVS) contributing to the gate voltage shift, where γ is a constant and δ is a power exponent whose best-fitted value is within 0.25–0.35.

To study trapping properties, one needs to consider two important parameters, namely, the capture cross-section, σ, and trap density, N_{ot}. Carrier injection usually induces not only the capture of injected carriers by dielectric traps but also generates interface states. Now, to distinguish the traps from one another, assuming that the differences between σ's are large enough, the following approximate relation may be obtained $\ln\left(\frac{\partial\Delta V_g}{\partial N_{inj}}\right) = \sum_i \left[\ln\left(\frac{q}{C_{ox}}N_{ot,i}(\sigma_t)_i\right) - (\sigma_t)_i N_{inj}\right]$. Thus, a plot of $\ln(\partial\Delta V_g/\partial N_{inj})$ versus N_{inj} (not shown) would provide a straight line with the slope $-\sigma_t$ and the intersection $\ln(q\sigma_t N_{ot}/C_{ox})$ in the respective region associated with each kind of traps. The extracted capture cross-section and trap density are found to be 1×10^{-19} cm^2 and 2×10^{13} cm^{-2}, respectively.

3.2.3. Influence of charge trapping under constant voltage stressing. When a stress voltage is applied across a MIS capacitor, the oxides suffer from several degradation mechanisms. Generally CVS measurements are applied to determine gate oxide reliability. A comparison of measured time-dependent current density decrease $[\Delta J_s(t, V_s) = J(t) - J(0)]$ observed during CVS (-6.0 V) for both non-nitrided and nitrided samples is shown in figure 9(*a*). All samples were stressed in the accumulation regime, which implies a minimum voltage drop over the substrate and excludes gate depletion effects. Initially, the high-k oxides have their own

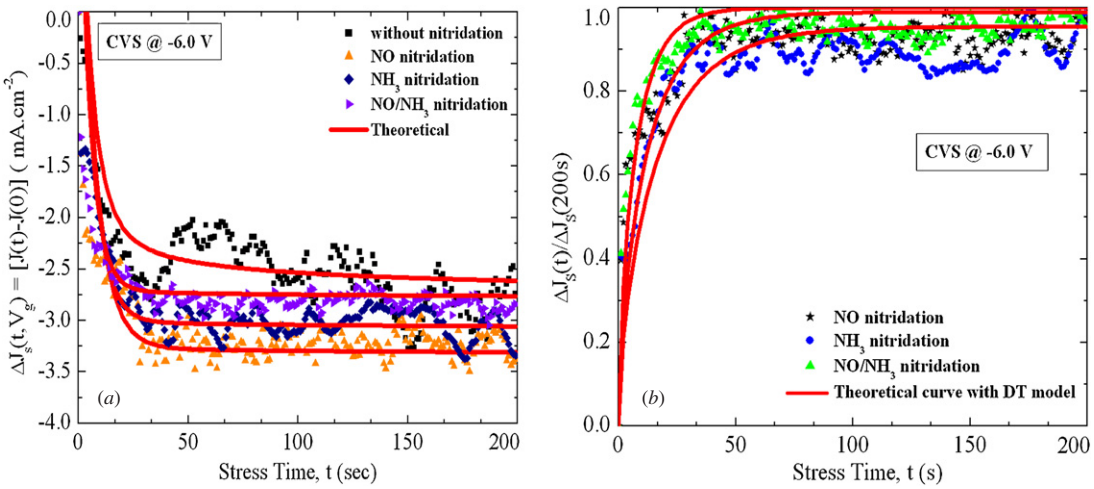

Figure 9. A comparison of stress time-dependent (*a*) current density shift, (ΔJ_s), and (*b*) normalized current density variation along with theoretical results for both non-nitrided and nitrided samples.

as-grown traps, which play an important role in the dielectric wear out.

However, as stress time progresses, the applied stress voltage also generates enormous amount of traps in the oxide layers. These traps act both as coulombic scattering centers and as pathways for increased local leakage current, usually known as stress-induced leakage current. The traps that are generated during a high-voltage stress are charged positively near the cathode and negatively near the anode due to hole tunneling into and out of the traps [30]. From figure 9(*a*), it is seen that the experimental data are best fitted (solid lines) by the following expression taking into account for both buildup of trap charges and stress-induced traps due to SILC:

$$\Delta J_s(t, V_s) = \xi(e^{-t/\tau} - 1) + \beta(V_s)t^{\gamma} \tag{13}$$

where ξ is a proportionality constant, β is related to the trap generation rate and γ is a power exponent whose value varies within $0 < \gamma < 1$.

3.2.4. CVS-induced defect density variation. As $\Delta J_s(t)$ variation in CVS measurements reflect the variation of defect density in the oxide generated during electrical stress; hence one can easily monitor the behavior of stress-generated traps into the bulk high-*k* stack. The time dependence of the CVS-induced defect density variation, ΔN_{stack}, has been modeled using the dispersive transport (DT) principle. A comparison of time-dependent current density variation $\Delta J_s(t)/\Delta J_s$ (200 s) for both non-nitrided and nitrided samples is shown in figure 9(*b*) under −6.0 V constant stress voltages (i.e. substrate injection). During CVS, holes are injected from the substrate into the gate, where they can release negatively charged species (N^- ion/trap) at the high-*k* stack/p-Ge interface. Generated N^- ion or traps then drift into the bulk stack layer via a random hopping mechanism, which is known as dispersive transport. Within this dispersive transport model, the stress-induced defect density variation can be expressed as [31]

$$\Delta N_{stack} \infty \left[1 - \int_0^{t_{GeO_x}/\mu t^{\alpha}} F_{GeO_x}(z)\,dz - \int_{t_{GeO_x}/\mu t^{\alpha}}^{t_{TiO_2}/\mu t^{\alpha}} F_{TiO_2}(z)\,dz\right] \tag{14}$$

in which a 'trial function' is used for the $F(z)$ approximation [32]:

$$F(z) = \begin{cases} 0 & \text{for} \quad z < 0, \\ (A^{\theta}/y_o)(1 + Bz)^{\alpha - \frac{1}{2}}\, e^{-z} & \text{for} \quad z > 0, \end{cases} \tag{15}$$

where $z = (y/y_o)^{\theta}$ and $\theta = (1 - \alpha)^{-1}$. The function $F(z)$ is related to the probability $P(x,t)$ of finding a transporting particle at a distance x at the time t. t_{GeOx} and t_{TiO2} are GeO_x and TiO_2 oxide thicknesses, respectively, μ is the average field dependent displacement per hop and α is an exponent characterizing the dispersiveness of the transport process. The solid line in figure 9(*b*) is the fit to the data using equation (14). The value of α is found to be within $0 < \alpha < 1$, which refers to a highly dispersive transport.

3.2.5. Leakage current behavior. A comparison of leakage current density as a function of applied bias for both non-nitrided and nitrided samples is shown in figure 10. It is seen that the leakage current density is about 0.005 A cm^{-2} for the non-nitrided sample, but it improves after nitridation. Fluctuations in leakage current around the gate voltage of −0.5 to 0 V for nitrided samples could arise from the transient charge-trapping effect. The effect of constant current stressing on leakage current characteristics of non-nitrided stacked layers with different injected fluences (−2.04 to −6.12 C cm^{-2}) is shown in figure 11(*b*). It is noted that the stress-induced leakage current increases with injected fluence, which is attributed to the generation of localized defects and positive charges as well as trap states near the injection interface. This SILC behavior can be analyzed by applying the inelastic trap assisted tunneling (ITAT) model and has been reported earlier [31]. Several tunneling models, useful for the simulation of tunneling behavior in stacked dielectric can be found in the literature. In practical applications, however, each model has its own merits and demerits. For dielectric stacks, the Tsu–Esaki model with the numeric WKB transmission coefficient [33], the Tsu–Esaki model with the transfer-matrix method [34], and the Tsu–Esaki model with the quantum transmitting boundary method [35] has been developed other than the ITAT model.

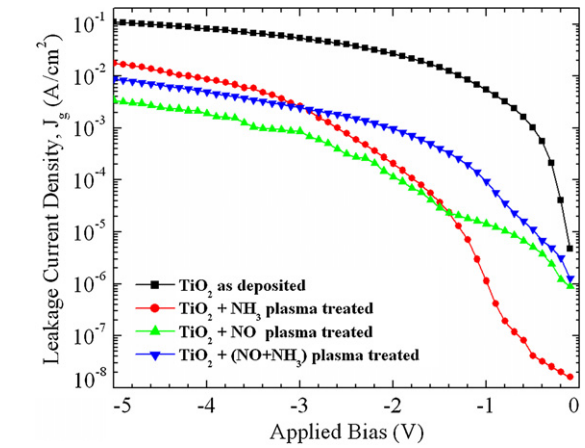

Figure 10. A comparison of leakage current characteristics for both non-nitrided and nitrided samples.

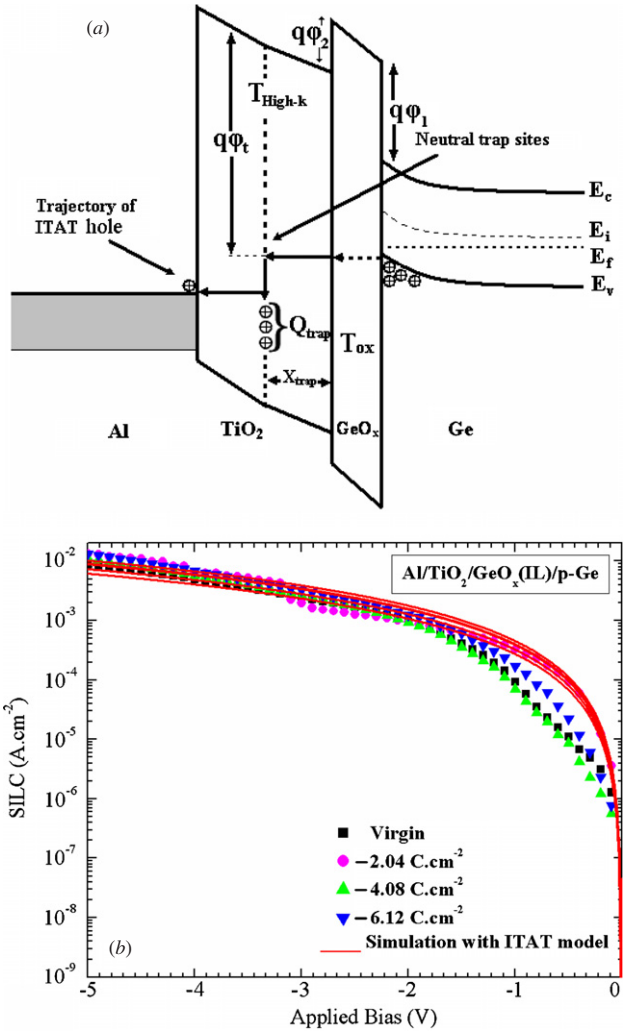

Figure 11. (*a*) Schematic energy band diagram of Al/TiO_2/GeO_x(IL)/p-Ge system illustrating the inelastic trap assisted tunneling (ITAT) mechanism in the TiO_2 layer and (*b*) *I–V* sweep before and after constant current stressing. SILC is evident across the entire voltage range. The figure also shows a good agreement between simulated and experimental SILC characteristics.

The key feature to the gate current modeling used in the above mentioned models is the apparent energy dispersion (E-k) within Franz two-band dispersion relation in the dielectric bandgap seen by the tunneling electrons. But none of these models consider the contribution of trap-assisted conduction phenomena. Also, one cannot avoid these defect/trap assisted conduction phenomena for such trappy dielectric materials. However, in the ITAT model, we have assumed that the holes first tunnel through the ultra-thin GeO_x interfacial layer (direct tunneling) and then tunnel through traps (shallow or deep) located below the valence band of the TiO_2 layer. The trajectory of tunneling holes (substrate injection) for the ITAT mechanism is schematically shown in figure 11(*a*). The traps that are captured at the above mentioned trap sites relax to a lower available energy state (deep traps). Finally the trapped holes enter the Al metal gate via a second tunneling step.

In figure 11(*a*), ϕ_1 is the hole barrier height between Ge and the GeO_x layer, ϕ_2 is the difference between Ge/GeO_x and Ge/TiO_2 barrier heights and ϕ_t is the trap energy level below the conduction band of TiO_2. X_{trap} indicates the position of the traps that participate in the tunneling process, i.e. the trapping centers with an energy level corresponding to the energy of the holes in the Ge valence band. Considering the above mentioned two-step tunneling process, the expression for SILC can be written as [31]

$$J = \frac{16.\pi q}{3.h}\sqrt{\left(\frac{m_s^*}{m_{ox}^*}\right)^5}\frac{N_t}{\sqrt{\phi_1}} \times \int_0^{X_{trap}} \frac{T_{ox}(V)T_{hk}(V,x)\sqrt{V^3}}{1+e^{qV/k_BT}}\,dx \tag{16}$$

where $qV = [\phi_1 - \phi_2 - \phi_t - qV_{ox} - (qV_{high\text{-}k}/T_{high\text{-}k}).x]$, m_s^* and m_{ox}^* are the effective masses of holes in the Ge substrate and GeO_x layer, respectively. Assuming that the expressions derived above for one-step tunneling also hold for ITAT, the tunneling probabilities for each region can be expressed within Wentzel–Kramers–Brillouin (WKB) approximation as follows:

$$T_{ox}(V) = \exp\left[\frac{-2}{\hbar}\int_0^{x_1}\sqrt{2.m_{ox}^*(E_{stack}-E_{ox}(x))}\,dx\right] \times \exp\left[\frac{-2}{\hbar}\int_{x_1}^{x_2}\sqrt{2.m_{hk}^*(E_{stack}-E_{hk}(x))}\,dx\right] \tag{17}$$

and

$$T_{hk}(V,x) = \exp\left[\frac{-2}{\hbar}\int_{x_2}^{x_3}\sqrt{2.m_{hk}^*(E_{stack}-E_{hk}(x))}\,dx\right] \tag{18}$$

where E_{ox} and E_{hk} are the energies of the valence band of GeO_x and TiO_2 layer, respectively and E_{stack} is the total potential energy in the GeO_x/TiO_2 stack layer. The simulated SILC of GeO_x/TiO_2 gate stacks, including ITAT contribution, are presented in the inset of figure 11(*b*) as a function applied bias for various injected fluences (−2.04 to −6.12 C cm^{-2}).

4. Conclusion

In conclusion, we have analyzed in detail, the effects of an oxynitride interfacial layer on electrical properties of TiO_2/GeO_xN_y/Ge MIS capacitors fabricated using PECVD

deposited high-*k* dielectrics. Usefulness of different N sources, such as NO, NH_3 and NO/NH_3 for the incorporation of N using plasma nitridation techniques has been studied. Among all the N sources used in this study, N incorporated by NO-plasma exhibit the best electrical characteristics for stacked $TiO_2/GeO_xN_y/Ge$ MIS capacitors. Judging both the electrical and physical characterization data, it may be concluded that the insertion of an ultra-thin Ge oxynitride (GeO_xN_y) interfacial layer is advantageous for producing gate-quality TiO_2 high-*k* dielectric stacks on Ge substrates for future Ge MOSFET applications. High-quality surface passivation of Ge substrates may be achieved by converting lossy GeO_2 into oxynitride by nitrogen engineering.

Acknowledgments

The authors would like to thanks Professor Fu-Ming Pan of Department of Materials Science and Engineering, National Chiao Tung University, Hsinchu 30049, Taiwan, Republic of China, for chemical characterization of the samples used in this study.

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