行政院國家科學委員會專題研究計畫 期中進度報告

次 32 奈米 CMOS 元件可靠性分析，量子結構效應，與蒙地卡羅電荷傳輸模擬(第 1 年)
期中進度報告(精簡版)

計 畫 類 別 ：個別型
計 畫 編 號 ：NSC 96-2628-E-009-165-MY3
執 行 期 間 ：96 年 08 月 01 日至 97 年 07 月 31 日
執 行 單 位 ：國立交通大學電子工程學系及電子研究所

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處 理 方 式 ：期中報告不提供公開查詢

中 華 民 國 97 年 05 月 26 日

次 32 奈米 CMOS 元件可靠性分析，量子結構效應，與蒙地卡羅電荷傳輸模擬(1/3)

Sub-32nm CMOS Device Reliability, Quantum Structure Effects and Carrier Transport Simulation by Using a Monte Carlo Method (1/3)

計畫編號：96-2628-E-009-165-MY3

執行期間：96 年 08 月 01 日 至 97 年 07 月 31 日

主持人：汪大暉 交通大學電子工程系教授

中文摘要

利用自行組裝之量測電路於高介電常數閘極介電層之研究，吾人發現有不規則之負偏壓溫度不穩定性。在某種加壓加溫之條件下，觀察到汲極電流增加之行為。且隨著時間和電壓變化時，汲極電流產生反轉之現象。吾人也發現在 p 型電晶體中加壓後之電流衰減以及 n 型電晶體中加壓後之電流回復之現象。吾人提出一物理模型—雙極性電荷捕捉，來解釋實驗現象；最後，由於雙極性電荷捕捉，吾人發現在加壓之後單一電子和電洞自高介電常數閘極介電層的缺陷中散逸之行為。同時藉由電荷幫浦實驗及載子分離等實驗來驗證物理模型之正確性。最後，評估負偏壓溫度不穩定性之電壓、溫度、及時間因素對汲極電流之影響。

Abstract

Negative bias-temperature (NBT) stress induced drain current instability in a pMOSFET with a HfSiON-SiO_2 gate stack is investigated by using a fast transient measurement technique. We find that in certain stress conditions the NBT induced current instability evolves from enhancement mode to degradation mode, giving rise to an anomalous turn-around characteristic with stress time and stress gate voltage. Persistent post-stress drain current degradation is found in a pMOSFET, as opposed to drain current recovery in its n-type MOSFET counterpart. A bipolar charge trapping model along with trap generation in a HfSiON gate dielectric is proposed to account for the observed phenomena. Post-stress single charge emissions from trap states in HfSiON are characterized. Charge pumping and carrier separation measurements are performed to support our model. The impact of NBT stress voltage, temperature and time on drain current instability mode is evaluated.

Index Terms: HfSiON, negative bias temperature instability, bipolar charge trapping, single charge emission

I. Introduction

NBT instability has been recognized as a major reliability concern in ultra-thin gate dielectric MOSFETs. It occurs in p-type devices and manifests itself as negative shifts of threshold voltage due to positive oxide charge trapping under negative gate voltage stressing. As compared to a SiO_2 gate dielectric, the NBTI in high permittivity (high-k) gate dielectric MOSFETs has been less explored. In previous

NBTI studies [1-3], a conventional "stress-and-sense" method was used, which introduces a switching delay between stress and sense up to a few seconds. For high-k gate dielectrics such as HfSiON, a significant post-stress transient effect was reported due to high-k dielectric charge trapping/detrapping. The ignorance of high-k charge trapping/detrapping in a switching delay may lead to an erroneous interpretation of measurement data and underlying physical mechanisms. Thus, to retrieve the important information between stress and sensing, a fast transient measurement technique [4,5] with a resolution of microseconds is employed in this work. By using this technique, the mode of the NBT induced drain current instability is characterized. Both current enhancement and degradation modes are observed in a HfSiON pMOSFET. A physical model based on bipolar charge trapping and trap generation in a high-k gate dielectric is proposed to explain the instability modes.

The devices used here are p-type MOSFETs with a polysilicon electrode and a HfSiON-SiO_2 gate stack. The gate length ranges from 0.08 m to 1.2 m, and the gate width ranges from 0.16 m to 10 m. The physical thickness of the high-k layer and the interfacial SiO_2 layer (IL) is 2.5nm and 1.4nm, respectively. The equivalent oxide thickness is 1.8nm. Detailed fabrication process and device characteristics were reported in [6,7]. To reduce the switching delay in characterization, our measurement system is computer-automated, including high-speed switches, an operational amplifier, and a digital oscilloscope (Fig. 1). The detailed measurement procedures were described in [4,5]. Other measurement techniques, such as charge pumping (CP) technique, single charge emission measurement and carrier separation measurement are utilized to monitor charge trapping/detrapping and trap generation.

II. NBTI Measurement Results

Fig. 2 shows the evolutions of NBT stress induced linear drain current change ($\Delta I_{d,lin}$) in control SiO_2 and HfSiON pMOSFETs by using the fast transient measurement system. The device dimension is W/L=10μm/0.2μm. The stress V_g is -2.8V, and the linear drain current ($I_{d,lin}$) is measured at V_g/V_d= -1.2V/-0.2V. As shown in the figure, $\Delta I_{d,lin}$ decreases monotonically with stress time in a SiO_2 control device, while a turn-around characteristic of $\Delta I_{d,lin}$ versus stress time is obtained in a HfSiON MOSFET. Note that one may fail to observe this anomalous turn-around behavior by using a conventional measurement setup such as Agilent 4156 due to a switching delay. Furthermore, the NBTI and its counterpart PBTI in a nMOSFET are compared in Fig. 3. The $\Delta I_{d,lin}$ in a nMOSFET (PBTI) is negative in the entire stress period and no turn-around feature like the NBTI is observed. More interestingly, the NBTI and the PBTI in HfSiON MOSFETs exhibit distinctly different post-stress drain current evolutions (Fig. 4). The PBTI exhibits a drain current recovery, as reported in literature [4]. However, the NBTI shows persistent drain current degradation after stress. The post-stress $I_{d,lin}$ degradation in a high-k pMOSFET implies trapped electron emission from a high-k gate dielectric after stressing V_g is removed. In Fig. 5 (a) and (b), NBT induced $\Delta I_{d,lin}$ at various stress V_g and temperatures are shown. The stress V_g ranges from -1.6V (result not shown in Fig. 5) to -2.8V with all other terminals grounded and the

temperature is from 25°C to 125°C. For a stress V_g weaker than -2V (selectively shown for clarity), $\Delta I_{d,lin}$ is negative (degradation mode) and decreases monotonically with stress time. The degradation aggravates with a larger stress $|V_g|$ (more negative). For a stress V_g stronger than -2V or a higher stress temperature, the drain current instability shows a different feature. The $I_{d,lin}$ initially increases with stress time (enhancement mode) and shortly evolves into degradation mode ($\Delta I_{d,lin}<0$), featuring a turn-around characteristic in Fig. 5 (a) and (b). The drain current enhancement has a positive dependence on stress $|V_g|$ and temperature. The transition time for the $I_{d,lin}$ evolving from enhancement mode to degradation mode is mostly within seconds in the bias range of interest. Fig. 6 demonstrates the dependence of $\Delta I_{d,lin}$ on stress V_g at different stress times. For t=0.1s, a lower stress $|V_g|$ (-1.4V~ -2V) induces a $I_{d,lin}$ degradation while a larger stress $|V_g|$ results in an enhancement. This trend remains for t=10s, but the turn-around $|V_g|$ is slightly increased. For a longer stress time (e.g., t=1000s), the dependence of $\Delta I_{d,lin}$ on V_g returns to a normal degradation mode as in SiO_2 gate dielectric transistors, and a larger stress $|V_g|$ results in a larger degradation [8,9]. The stress temperature dependence of $\Delta I_{d,lin}$ is shown in Fig. 7. For a short stress time (e.g., t=10s), $\Delta I_{d,lin}$ changes from negative at low temperatures to positive at high temperatures. But for a longer stress time (e.g., t=1000s), the $I_{d,lin}$ degradation increases monotonically with stress temperature. The positive temperature dependence of the $I_{d,lin}$ degradation in a high-k MOSFET can be realized due to temperature accelerated high-k/IL trap generation because of thermo-chemical reaction [10].

III. Bipolar Charge Trapping Model

In a negative V_g stress, two carrier injection processes affect I_d instability, (i) valence band electron injection from the p^+ poly-gate into high-k traps (I_d enhancement mode) and (ii) hole injection from the inverted channel into high-k/IL traps (I_d degradation mode). Thus, available trap states in a high-k dielectric, either pre-existing traps or stress generated traps, and injected carrier fluence should be considered in a NBT instability model. Fig. 8 illustrates the energy band diagrams in equilibrium (Fig. 8(a)) and in various NBT stress conditions, for example, low V_g and low temperature stress (Fig. 8(b)), low V_g and high temperature stress (Fig. 8(c)), and high V_g and low temperature stress (Fig. 8(d)). In thermal equilibrium, trap states with energy (E_t) below the Fermi level (E_F) are occupied by electrons while those above E_F are empty. The shaded area in Fig. 8 represents the occupied states in the high-k layer. When a low stress $|V_g|$/ temperature is applied (Fig. 8(b)), the empty high-k traps available for poly-gate valence electron injection are very limited due to a small band-bending (E_t) in a high-k gate dielectric. In this case, electron trapping into the high-k layer is negligible, and $I_{d,lin}$ is dominated by hole injection from the inverted channel, leading to a $I_{d,lin}$ degradation. In this regime, a larger $|V_g|$ aggravates $I_{d,lin}$ due to a larger hole injection current, which is in agreement with our measured result in Fig. 6. As stress temperature or $|V_g|$ increases, more poly-gate electrons can inject into pre-existing high-k traps either because of thermally assisted tunneling (Fig.8(c)) or because of more available

empty states due to a larger band-bending (Fig.8(d)). In these stress conditions, both electron trapping and hole trapping into the high-k layer are possible. The measurement result in Fig. 5(a) and (b) implies that electron trapping is dominant in the initial stress period and hole trapping gradually supersedes electron trapping due to new hole trap creation in the high-k and IL layers, thus resulting in a turn-around feature of the $I_{d,lin}$ evolution.

To confirm our bipolar charge trapping model for NBT instability, post-stress trapped charge emissions are characterized. The purpose of this characterization is to identify injected charge species during stress. The detail of this method was described in our previous papers for trapped electron emission from HfSiON in a nMOSFET [4] and trapped hole emission from SiO_2 in a pMOSFET [11]. Fig. 9 shows our measured I_d evolution patterns after low (-1.5V) and high (-2.2V) V_g stress, respectively. The transistors have W/L=0.16 m/0.08 m. The stress time (or exactly the charge filling time) for both cases is 0.2s, and the post-stress measurement condition is $V_g \sim V_t$ and V_d=-0.2V. In Fig. 9, trapped charge emission is manifested by a staircase-like jump in the drain current. For a pMOSFET, an upward shift (increase in $|I_d|$) corresponds to a single hole emission, and a downward shift corresponds to a single electron emission. Notably, only trapped hole emissions are found for the low V_g stress (Fig. 9(a)) while both electron and hole emissions are obtained for the high V_g stress (Fig. 9(b)). This single charge emission result provides direct evidence of bipolar charge trapping in a high V_g stress condition. It should be remarked that we did not observe any random telegraph signal at the post-stress measurement biases, indicating that the observed current jumps in Fig. 9 are attributed to injected charge emissions.

We also characterize high-k/IL trap generation for low and high V_g stress by using a charge pumping method. A two-frequency (5kHz and 1MHz) technique is used to separate IL/Si interface traps (D_{it}) from bulk high-k traps (N_{HK}) [12]. The high frequency CP current is contributed by D_{it} and the difference between the CP currents of the two frequencies reflects high-k trap density N_{HK}. Fig. 10 shows the extracted D_{it} and N_{HK} versus stress time for stress V_g=-1.5V and -2.2V. No new traps are created in a low V_g (-1.5V) stress even for a stress time of t=1000s, indicating that the $I_{d,lin}$ degradation at a low stress V_g is mainly attributed to hole trapping into pre-existing high-k traps. On the other side, both interface trap and bulk high-k trap generation is observed in a high V_g (-2.2V) stress.

In addition to available traps for electron and hole injection, another factor affecting NBT instability mode is the fluence of injected carriers during stress. A carrier separation measurement was performed to explore the effect of injected carrier fluence on I_d instability. Fig. 11 illustrates the carrier flow in a high-k pMOSFET under $-V_g$ stressing. The hole injection current from the inverted channel constitutes the source/drain current (i.e., $I_{S/D}$) and the electron injection current from the p^+ poly-gate flows to the substrate (i.e., I_{sub}). Fig. 12(a) shows the measured hole and electron currents versus stress gate voltage at T=25°C. Two points are worth noting; (i) Holes are the dominant conduction carrier at a low stress $|V_g|$. As a stress $|V_g|$ increases, an electron current

becomes dominant. Thus, electron filling effect is more significant than hole filling at a higher stress $|V_g|$. This trend is consistent with the measured result in Fig. 6, i.e, $I_{d,lin}$ degradation in a low V_g region and $I_{d,lin}$ enhancement in a high V_g region in the initial stress period.

As stress temperature increases to 100°C (Fig. 12 (b)), the electron current is enhanced to a larger extent, compared to the hole current and thus it supersedes the hole current at a smaller stress V_g. This result is in agreement with our thermally-assisted electron tunneling model in Fig. 8(c) and can well explain the increased $I_{d,lin}$ enhancement at a higher temperature in a low stress V_g region (Fig. 5(b)).

IV. Conclusion

In this work, various NBT induced drain current instability modes in HfSiON pMOSFETs are investigated. The drain current enhancement is observed in the initial stress period in certain stress conditions. Electron trapping, hole trapping and new trap generation are found to be responsible for the drain current instability modes. The impact of stress V_g, temperature and stress time on NBT instability is characterized. In high $|V_g|$ and/or high temperature stress, electron trapping into pre-existing high-k traps is dominant in the initial stress period, thus causing an I_d enhancement. As stress continues, hole injection and new hole trap creation in HK/IL layers eventually become dominant, giving rise to a turn-around characteristic of the drain current evolution with time. For low V_g stress, the I_d instability is dictated by hole injection throughout the entire stress period

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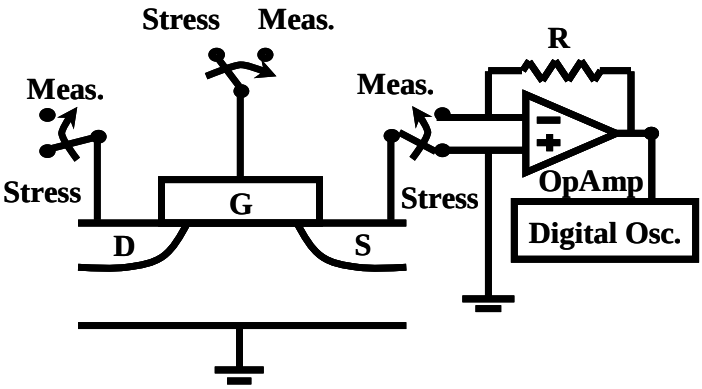


Fig. 1 Schematic diagram for the transient measurement system. The high speed switches minimize a switching delay down to microseconds between stress and drain current measurement.

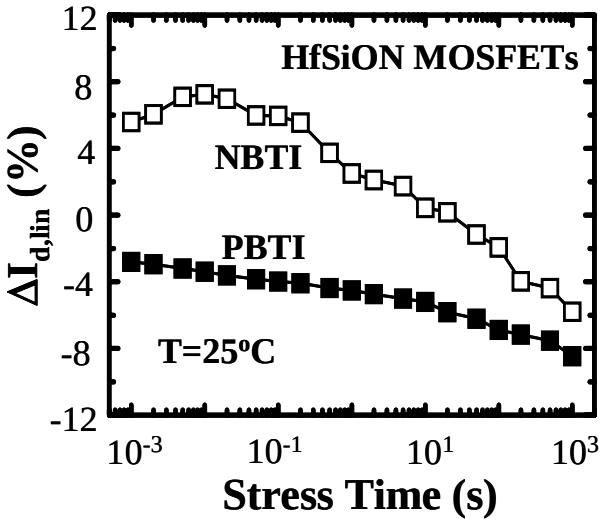


Fig. 3 Linear drain current change ($\Delta I_{d,lin}$) in a pMOSFET (NBTI) and in a nMOSFET (PBTI). The stress V_g is -2.8V for the pMOSFET and 2.2V for the nMOSFET.

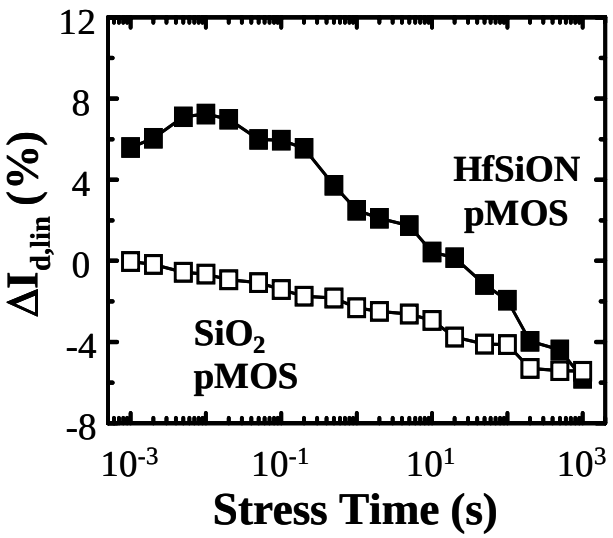


Fig. 2 NBT stress induced linear drain current change ($\Delta I_{d,lin}$) in SiO_2 and HfSiON pMOSFETs. The stress V_g is -2.8V and the linear drain current ($I_{d,lin}$) is measured at V_g/V_d=-1.2V/-0.2V.

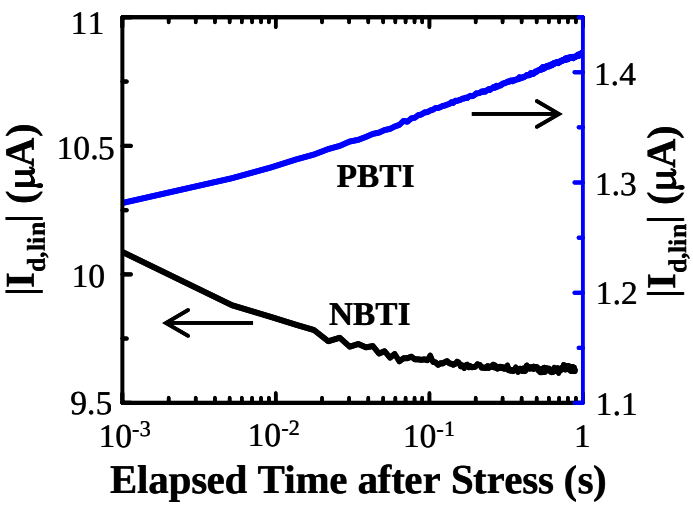
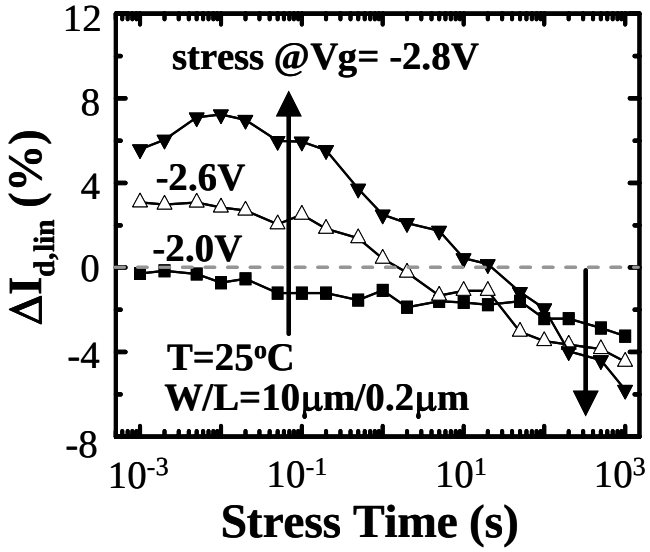


Fig. 4 $|I_{d,lin}|$ as a function of elapsed time after stress. The drain current recovery is observed in a nMOSFET, while the NBTI shows persistent post-stress current degradation.



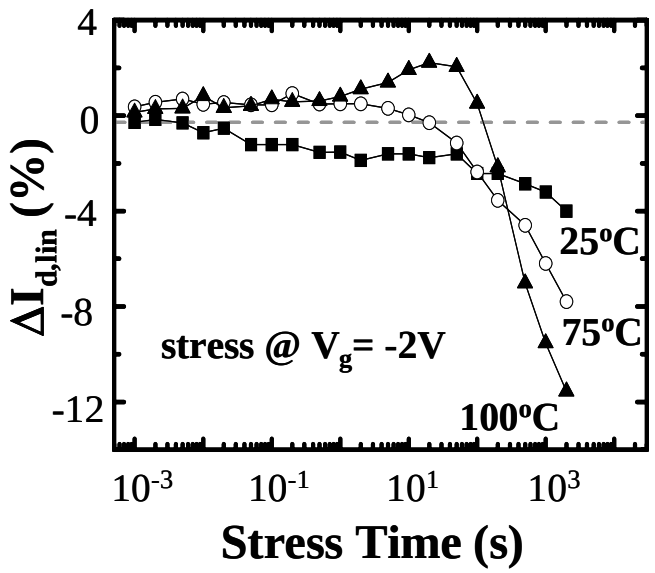


Fig. 5 NBT stress induced drain current evolution (a) for different stress V_g, and (b) for different stress temperatures. Drain current enhancement in an initial stage of stressing is observed for high stress V_g (-2.6V and -2.8V) and/or high stress temperatures.

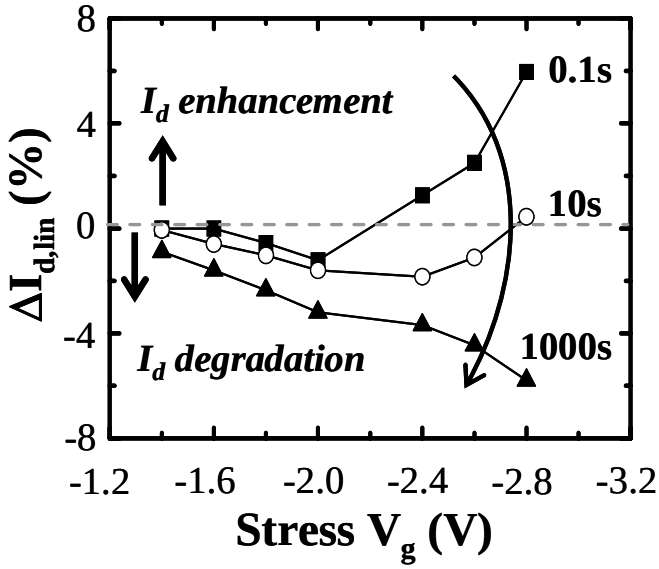


Fig. 6 Stress V_g dependence of $\Delta I_{d,lin}$ at different stress times. For a short stress time (t=0.1s and 10s), $\Delta I_{d,lin}$ can be positive or negative, depending on stress V_g. For a longer stress time (t=1000s), the dependence returns to a normal degradation mode as in SiO_2 gate dielectric transistors.

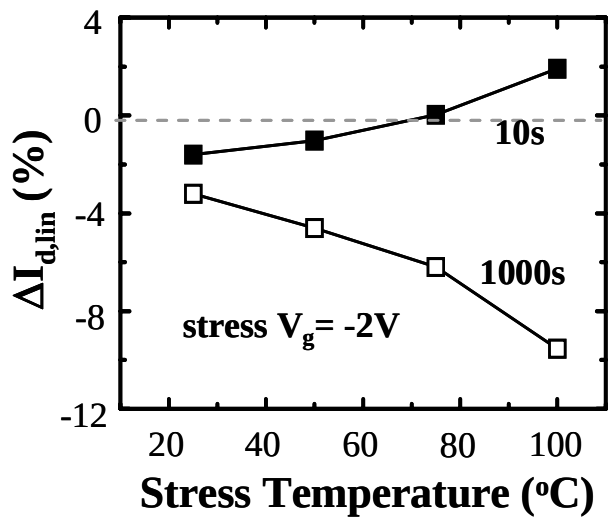


Fig. 7 Stress temperature dependence of $\Delta I_{d,lin}$.

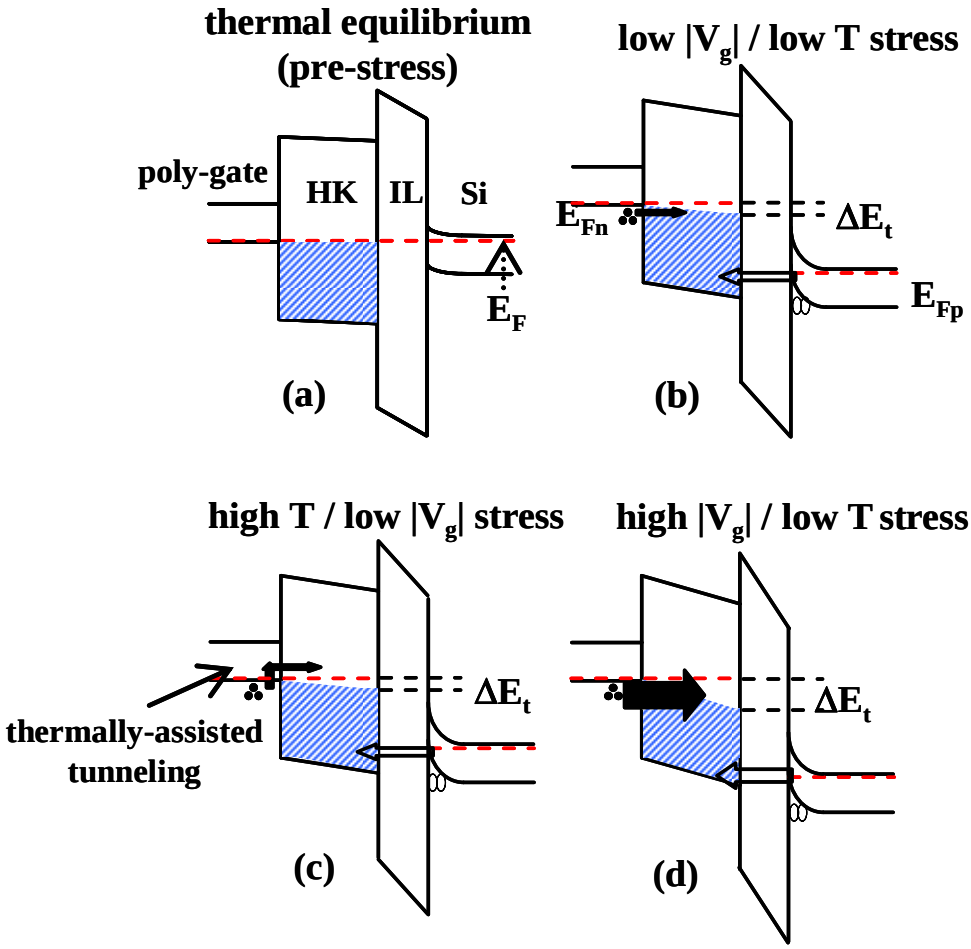


Fig. 8 Schematic representation of an energy band diagram and charge injection processes in (a) thermal equilibrium, (b) low $|V_g|$/ low T stress, (c) high T/ low $|V_g|$ stress, and (d) high $|V_g|$/ low T stress. The shaded area represents the occupied trap states in the high-k layer. Electron injection from the poly gate and hole injection from the channel are illustrated.

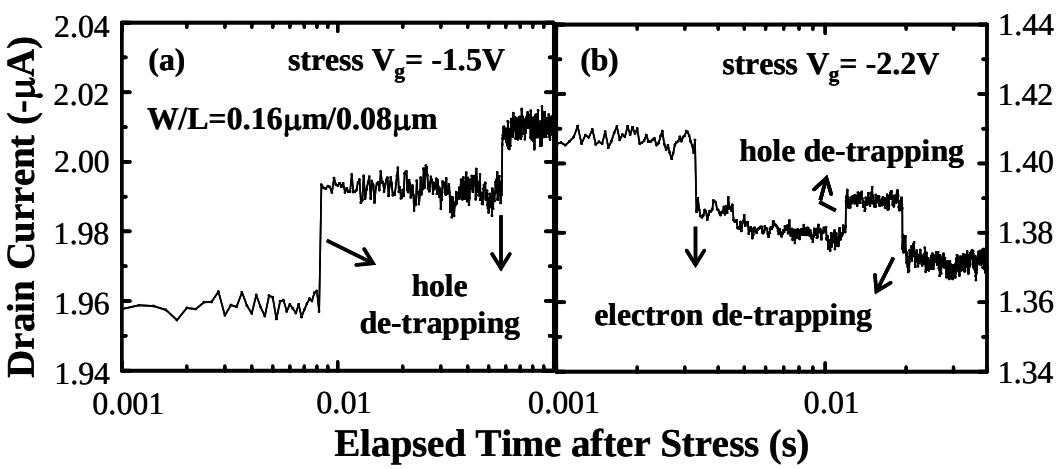


Fig. 9 Post-stress I_d evolution patterns in small-area devices after (a) a low $|V_g|$ (-1.5V) stress and (b) a high $|V_g|$ (-2.2V) stress. The post-stress measurement condition is $V_g \sim V_t$ and V_d=-0.2V.

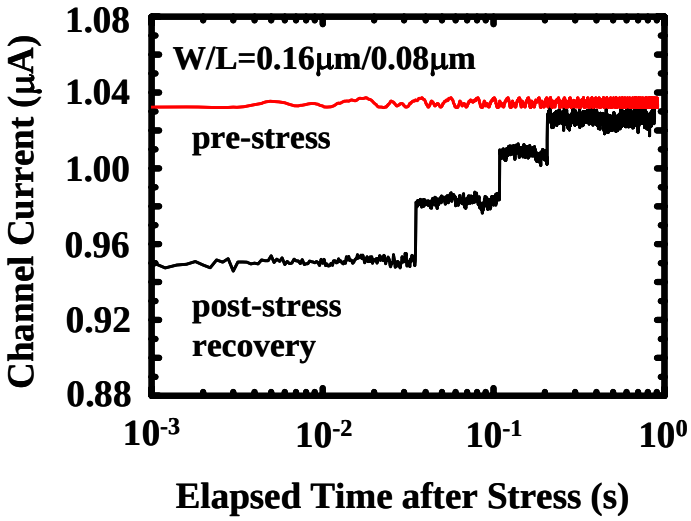


Fig. 10 Poststress I_d evolution patterns after stress at Vg = 0.7 V for 0.2 s in an nMOSFET. The poststress measurement condition is Vg/Vd =0.3 V/0.2 V.

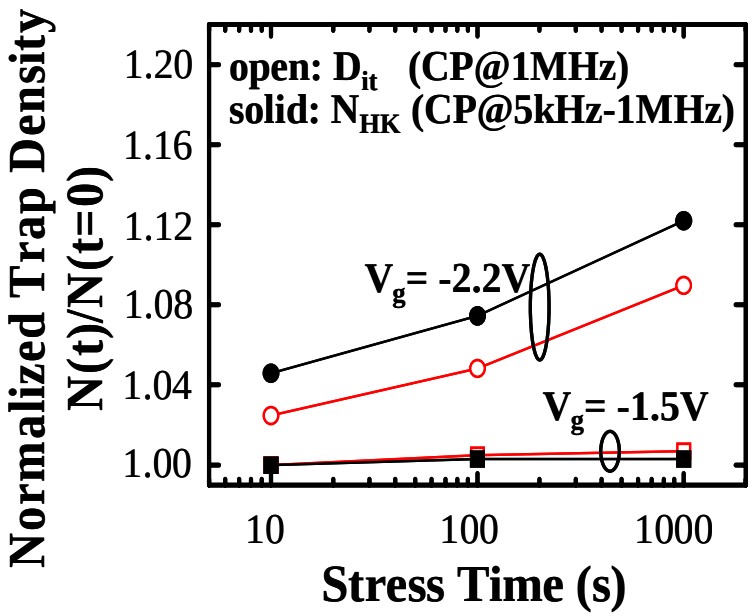


Fig. 11 Interface traps (D_{it}) and bulk high-k traps (N_{HK}) growth rates in NBT stress at Vg=-1.5V and Vg=-2.2V. A two-frequency charge pumping method is used.

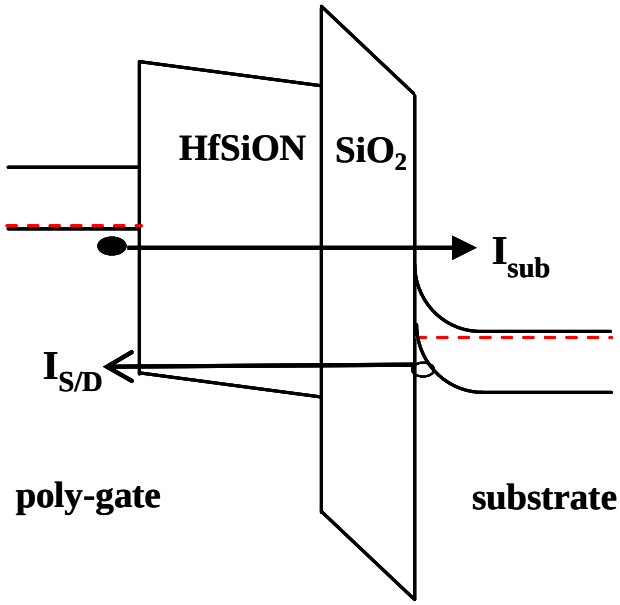


Fig. 12 Illustration of carrier flow in a high-k pMOSFET under $-V_g$ stressing. I_{sub} denotes the electron injection current from the p^+ poly-gate to substrate, and $I_{S/D}$ stands for hole injection current from the inverted channel.

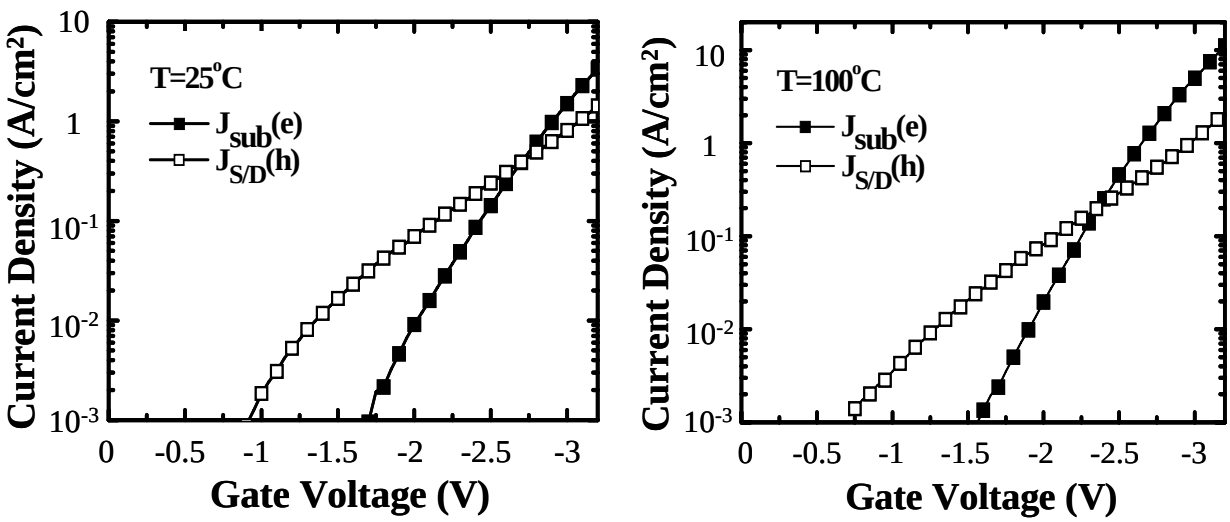


Fig. 13 Gate voltage dependence of hole injection current ($I_{S/D}$) and electron injection current (I_{sub}) in a high-k pMOSFET, measured at (a) T=25°C and (b) T=100°C.