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摘　　要

本研究報告為蒙地卡羅模擬(Monte Carlo simulation)於先進互補式金氧半電晶體(advanced CMOS)之應用。此外，高介電閘極氧化層(high-*k*)之可靠性議題，如電壓溫度引致不穩定(BTI)之研究，亦有所探討。

第一章探討對於鍺通道雙閘極電晶體，量子效應對電洞遷移率之影響。低電場之電洞遷移率是透過蒙地卡羅方法求得。模擬結果得知，對於 (100) /[110] 「矽」通道，電洞遷移率隨著通道厚度變薄而減少。此模擬結果與實驗相符合。然而對於(100)/[100]「鍺」通道，電洞遷移率在某個通道厚度下具有最大值。此現象乃因「次能帶內」散射與「次能帶間」散射交互作用下所產生。在(110)/[-110]「鍺」通道方向上，亦可發現相同情形。此外，吾人發現當單軸壓縮應力施於(100)/[110]或(110)/[-110]鍺通道上時，電洞遷移率將可進一步提昇。

在第二章，吾人利用電腦自動化量測電路系統，研究 HfSiON pMOSFETs 中負電壓溫度所引致之不穩定性。實驗結果顯示，在某特定加壓條件下，負電壓溫度加壓所引致之汲極電流，將從增益模式逐

漸演變成退化模式，隨著加壓時間或加壓電壓之呈現奇特的「轉彎現象」(turn around)。此外，對於 pMOSFET 元件加壓後，汲極電流呈現退化行為。然而，對於 nMOSFET 元件加壓後，汲極電流呈現恢復行為。吾人提出一「雙極電荷捕捉模型」成功解釋奇特的「轉彎現象」，並以單電荷散逸量測、電荷幫浦法以及載子分離量測，驗證所提出之物理模型。

在第三章，吾人利用特殊結構研究自我加熱效應所引發的暫態電子效應。同時，利用二維元件模擬驗證實驗結果，並用來分析交流頻率與元件退化之間的關聯性。研究結果發現，熱載子效應在交流偏壓下的電流退化，將比直流偏壓下的電流更為嚴重，其原因在於自我加熱效應的消失將造成熱載子的增加。

ABSTRACT

This report will focus on the Monte Caro simulation and its applications to advanced CMOS devices. The reliability issue, negative bias temperature instability (NBTI) in advanced gate dielectric (high-*k*), is studied as well.

The quantum confinement effects on hole mobility in Ge-channel double gate MOSFETs are studied in Chapter 1. The low-field hole mobility is calculated by a Monte Carlo simulation. Our simulation result shows that the hole mobility in a (100)/[110] silicon well decreases with a decreasing well thickness, which is in agreement with the experimental result. The hole mobility in a Ge-channel pMOSFET, however, exhibits a peak in a sub-20 nm well because of the interplay between intrasubband and intersubband scatterings. The peak mobility in (110)/[-110] channel direction can be also achieved. Moreover, we find that the hole mobility can be further improved when the uniaxial compressive stress is applied to (100)/[110] or (110)/[-110] channel direction.

The characteristic of bipolar charge trapping induced anomalous NBTI in HfSiON gate dielectric pMOSFETs is demonstrated in Chapter 2 by using a fast transient measurement technique. Our study shows that in certain stress conditions, the NBT-induced current instability evolves from enhancement mode to degradation mode, giving rise to an

anomalous turn-around characteristic with stress time and stress gate voltage. Persistent post-stress drain current degradation is found in a pMOSFET, as opposed to drain current recovery in its n-type MOSFET counterpart. A bipolar charge trapping model along with trap generation in a HfSiON gate dielectric is proposed to account for the observed phenomena. Post-stress single charge emissions from trap states in HfSiON are characterized. Charge pumping and carrier separation measurements are performed to support our model.

Self-heating induced transient hot carrier effects are investigated in Chapter 3 by using the metal-contact structure. The AC stress-frequency dependence of device degradation is characterized and evaluated by a two-dimensional numerical simulation. Our result shows that drain current degradation in AC stress is more serious than in DC stress because of the reduction of self-heating effect.

Chapter 1

Study of Quantum Confinement Effects on Hole Mobility in Silicon and Germanium Double Gate MOSFETs

1.1 Preface

Double-gate (DG) metal-oxide-semiconductor field-effect-transistors (MOSFETs) and fin field-effect-transistor have been considered as promising alternatives to bulk MOSFETs in 22nm technology node and beyond due to their immunity to short channel effects. Recently, advanced channel materials with higher carrier mobility than bulk Si, such as Ge, and III-V materials, have attracted much attention. Experimental works have shown the possibility that the inversion carrier mobility can be further improved in quantum structure MOSFETs by a subband modulation [1][2]. However, there has been little work on Ge-channel DG-pMOSFETs addressing valence subband and substrate/channel orientation effects on hole mobility.

In this work, we analyze quantum confinement effects on hole mobility as a function of a body thickness in Si- and Ge-channel DG-pMOSFETs. The low-field hole mobility is calculated by a Monte Carlo method [3]. The role of quantum confinement effects in a Ge-channel is compared with a Si-channel with a valence subband calculation. The impact of substrate orientation on hole mobility is also evaluated. Furthermore, the effect of uniaxial compressive stress is discussed.

1.2 Valence Band Structure in Strained Bulk Materials

Various methods have been developed to calculate a band structure in

semiconductors, including the pseudo-potential method [4], the k · p method [5], the tight binding method [6], and the bond orbital model method [7]. In this work, the Luttinger-Kohn model [8] under the framework of k · p method is employed to calculate the valence band structure. This method has the following merits. First, the Luttinger-Kohn model is suitable for diamond and zinc blende structure semiconductors, whose band gap is much larger than the split-off energy [9]. Second, due to the warping of valence bands, the Luttiner-Kohn model rather than the effective-mass approximation is commonly used to obtain an accurate valence band structure. Third, the strain effects can be easily taken into account when the Bir-Pikus Hamiltonian [10] is incorporated into the Luttinger Hamiltonian. For the k · p method in the Luttinger-Kohn model (see Fig. 1.1), the heavy-hole, the light-hole and split-off bands in double degeneracy are considered and are called class A. The rest of the bands are defined as class B. The effects of bands in class B on those in class A are also considered.

Based on the theory of Luttinger-Kohn and Bir-Pikus, the valence band structure of a strained bulk material can be expressed in Equation (1.1) [11],

$$H = H_k + H_\varepsilon \tag{1.1}$$

where H_k is the unstrained Hamiltonian (Luttinger Hamiltonian) and H_ε is the strained Hamiltonian (Bir-Pikus Hamiltonian). Thus, the total Hamiltonian H can be expressed as the 6×6 Hamiltonian in the envelope function space (Equation (1.2)).

$$H=-\begin{bmatrix} P+Q & -S & R & 0 & -\frac{1}{\sqrt{2}}S & \sqrt{2}R \\ -S^{+} & P-Q & 0 & R & -\sqrt{2}Q & \sqrt{\frac{3}{2}}S \\ R^{+} & 0 & P-Q & S & \sqrt{\frac{3}{2}}S^{+} & \sqrt{2}Q \\ 0 & R^{+} & S^{+} & P+Q & -\sqrt{2}R^{+} & -\frac{1}{\sqrt{2}}S^{+} \\ -\frac{1}{\sqrt{2}}S^{+} & -\sqrt{2}Q^{+} & \sqrt{\frac{3}{2}}S & -\sqrt{2}R & P+\lambda & 0 \\ \sqrt{2}R^{+} & \sqrt{\frac{3}{2}}S^{+} & \sqrt{2}Q^{+} & -\frac{1}{\sqrt{2}}S & 0 & P+\lambda \end{bmatrix} \begin{matrix} \left|\frac{3}{2},\frac{3}{2}\right\rangle \\ \left|\frac{3}{2},\frac{1}{2}\right\rangle \\ \left|\frac{3}{2},-\frac{1}{2}\right\rangle \\ \left|\frac{3}{2},-\frac{3}{2}\right\rangle \\ \left|\frac{1}{2},\frac{1}{2}\right\rangle \\ \left|\frac{1}{2},-\frac{1}{2}\right\rangle \end{matrix} \tag{1.2}$$

where $P=P_k+P_\varepsilon$, $Q=Q_k+Q_\varepsilon$, $R=R_k+R_\varepsilon$, $S=S_k+S_\varepsilon$. The symbol λ represents the split-off energy. The symbol $^+$ represents the operation of the complex conjugate. The basis function $\left|J,m_J\right\rangle$ represents the Bloch wave function at the zone center, consisting of heavy hole states $\left|\frac{3}{2},\pm\frac{3}{2}\right\rangle$, light hole states $\left|\frac{3}{2},\pm\frac{1}{2}\right\rangle$, and split-off states $\left|\frac{1}{2},\pm\frac{1}{2}\right\rangle$, which takes into account two spin states..

$$P_k=(\frac{\hbar^2}{2m_0})\gamma_1(k_x{}^2+k_y{}^2+k_z{}^2) \tag{1.3a}$$

$$Q_k=(\frac{\hbar^2}{2m_0})\gamma_2(k_x{}^2+k_y{}^2-2k_z{}^2) \tag{1.3b}$$

$$R_k=(\frac{\hbar^2}{2m_0})\sqrt{3}[-\gamma_2\ (k_x{}^2-k_y{}^2)+2i\gamma_3k_xk_y] \tag{1.3c}$$

$$S_k=(\frac{\hbar^2}{2m_0})2\sqrt{3}\gamma_3(k_x-ik_y)k_z \tag{1.3d}$$

$$P_\varepsilon=-a_v(\varepsilon_{xx}+\varepsilon_{yy}+\varepsilon_{zz}) \tag{1.4a}$$

$$Q_\varepsilon=-\frac{b}{2}(\varepsilon_{xx}+\varepsilon_{yy}-2\varepsilon_{zz}) \tag{1.4b}$$

$$R_\varepsilon=-\frac{\sqrt{3}}{2}b(\varepsilon_{xx}-\varepsilon_{yy})-id\varepsilon_{xy} \tag{1.4c}$$

$$S_{\varepsilon} = -d(\varepsilon_{zx} - i\varepsilon_{yz}) \tag{1.4d}$$

γ_1, γ_2, and γ_3 are the Luttinger parameters. m_0 is the mass of free electron. k_x, k_y, and k_z are the wave vector in x, y and z direction, respectively. a_v, b and d are the Bir-Pikus deformation potentials for the valence bands. According to [12], the strain tensor (ε) is related to the stress tensor (σ) by the elastic compliance constant (S_{ij}) or elastic stiffness constant (C_{ij}) matrix.

$$\varepsilon = S \bullet \sigma \tag{1.5}$$

$$\sigma = C \bullet \varepsilon \tag{1.6}$$

The elastic compliance constant or elastic stiffness constant matrix relates the six strain components to the six stress components. As a result, the matrix, S or C, has 36 coefficients. However, due to the cubic symmetry in Si or Ge, only the three independent coefficients are needed. Thus, the strain-stress relation can be expressed as Equations (1.7) and (1.8) [13].

$$\begin{bmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{zz} \\ 2\varepsilon_{yz} \\ 2\varepsilon_{xz} \\ 2\varepsilon_{xy} \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} & S_{12} & 0 & 0 & 0 \\ S_{12} & S_{11} & S_{12} & 0 & 0 & 0 \\ S_{12} & S_{12} & S_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & S_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & S_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & S_{44} \end{bmatrix} \begin{bmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \sigma_{yz} \\ \sigma_{xz} \\ \sigma_{xy} \end{bmatrix} \tag{1.7}$$

$$\begin{bmatrix}\sigma_{xx}\\ \sigma_{yy}\\ \sigma_{zz}\\ \sigma_{yz}\\ \sigma_{xz}\\ \sigma_{xy}\end{bmatrix}=\begin{bmatrix}C_{11} & C_{12} & C_{12} & 0 & 0 & 0\\ C_{12} & C_{11} & C_{12} & 0 & 0 & 0\\ C_{12} & C_{12} & C_{11} & 0 & 0 & 0\\ 0 & 0 & 0 & C_{44} & 0 & 0\\ 0 & 0 & 0 & 0 & C_{44} & 0\\ 0 & 0 & 0 & 0 & 0 & C_{44}\end{bmatrix}\begin{bmatrix}\varepsilon_{xx}\\ \varepsilon_{yy}\\ \varepsilon_{zz}\\ 2\varepsilon_{yz}\\ 2\varepsilon_{xz}\\ 2\varepsilon_{xy}\end{bmatrix} \tag{1.8}$$

where the elastic compliance constant and elastic stiffness constant can be related by

$$C_{11}-C_{12}=(S_{11}-S_{12})^{-1} \tag{1.9a}$$

$$C_{11}+C_{12}=(S_{11}+2S_{12})^{-1} \tag{1.9b}$$

$$C_{44}=1/S_{44} \tag{1.9c}$$

Moreover, we can express Equation (1.7) into Equation (1.10).

$$\begin{bmatrix}\varepsilon_{xx}\\ \varepsilon_{yy}\\ \varepsilon_{zz}\\ 2\varepsilon_{yz}\\ 2\varepsilon_{xz}\\ 2\varepsilon_{xy}\end{bmatrix}=\begin{bmatrix}S_{11}\sigma_{xx}+S_{12}\sigma_{yy}+S_{12}\sigma_{zz}\\ S_{12}\sigma_{xx}+S_{11}\sigma_{yy}+S_{12}\sigma_{zz}\\ S_{12}\sigma_{xx}+S_{12}\sigma_{yy}+S_{11}\sigma_{zz}\\ S_{44}\sigma_{yz}\\ S_{44}\sigma_{xz}\\ S_{44}\sigma_{xy}\end{bmatrix} \tag{1.10}$$

For instance, it is believed that the [110] channel direction is the primarily used channel direction in strained-Si technologies because of its largest hole piezoresistance coefficient for longitudinal compressive stress on both (100) and (110) substrates [15]. The [ ] and ( ) are the notations of channel direction and substrate orientation, respectively. As an uniaxial stress is applied to the (100)/[110] direction,

the unit vector along the [110] direction is $[\frac{1}{\sqrt{2}},\frac{1}{\sqrt{2}},0]$. Thus, we have $\sigma_{xx}=\frac{1}{2}\sigma$, $\sigma_{yy}=\frac{1}{2}\sigma$, $\sigma_{zz}=0$, $\sigma_{yz}=0$, $\sigma_{xz}=0$, and $\sigma_{xy}=\frac{1}{2}\sigma$, where σ is positive for a tensile stress and is negative for a compressive stress. As a consequence, according to Equation (1.10), $\varepsilon_{xx}=\frac{1}{2}(S_{11}+S_{12})\cdot\sigma$, $\varepsilon_{yy}=\frac{1}{2}(S_{11}+S_{12})\cdot\sigma$, $\varepsilon_{zz}=S_{12}\cdot\sigma$, $\varepsilon_{yz}=0$, $\varepsilon_{xz}=0$, $\varepsilon_{xy}=\frac{1}{4}S_{44}\cdot\sigma$. Then, these strain components are introduced into Equation (1.2) to consider the stress effect.

When dealing with the substrate orientation other than the (100) direction, an appropriate rotation matrix is employed [16]. We must transform the crystallographic coordinate system (*x,y,z*) into the new coordinate system (*x',y',z'*), where *z'* is also the new growth direction. For example, when the (110) substrate is considered, the new coordinate system (*x',y',z'*) is thus given by Equation (1.11). The corresponding Luttinger Hamiltonian components are written as Equation (1.12).

$$k_x^{'}=-k_z \tag{1.11a}$$

$$k_y^{'}=\frac{1}{\sqrt{2}}(-k_x+k_y) \tag{1.11b}$$

$$k_z^{'}=\frac{1}{\sqrt{2}}(k_x+k_y) \tag{1.11c}$$

$$P_k=(\frac{\hbar^2}{2m_0})\gamma_1(k_x^{'2}+k_y^{'2}+k_z^{'2}) \tag{1.12a}$$

$$Q_k=(\frac{\hbar^2}{2m_0})\gamma_2(-2k_x^{'2}+k_y^{'2}+k_z^{'2}) \tag{1.12b}$$

$$R_k=(\frac{\hbar^2}{2m_0})\sqrt{3}[2\gamma_2k_y^{'}k_z^{'}+i\gamma_3(-k_y^{'2}+k_z^{'2})] \tag{1.12c}$$

$$S_k=(\frac{\hbar^2}{2m_0})\sqrt{6}\gamma_3(k_x^{'}k_y^{'}-k_x^{'}k_z^{'}+ik_x^{'}k_y^{'}+ik_x^{'}k_z^{'}) \tag{1.12d}$$

1.3 Valence Subband Structure in pMOSFETs

1.3.1 Schrodinger Equation with a Six-band Luttinger Hamiltonian

The valence subbands in an inversion layer can be solved by obtaining the self-consistent solution to the Poisson and Schrödinger equations under the framework of a six-band Luttinger Hamiltonian, instead of using the effective mass approximation. In the simulation, we take the coordinate z to be the direction perpendicular to the semiconductor and gate dielectric interface. The Schrödinger equation can be expressed as Equation (1.13).

$$\left[H(k_x,k_y,k_z)+V(z)I_{6\times6}\right]\varphi_{n,k_x,k_y}(z)=E_n\cdot\varphi_{n,k_x,k_y}(z) \tag{1.13}$$

where H is the 6×6 Hamiltonian with or without strain Hamiltonian. $\varphi_{n,kx,ky}(z)$ is a 6×1 vector containing the components of the basis function $\left|J,m_J\right\rangle$, I_{6x6} is the identity matrix of order 6, $V(z)$ is the potential energy, and E_n is the n-th subband energy. From Equations (1.3)-(1.4), we know that H is a second-order polynomial in k_z. Thus H can be expressed in Equation (1.14) [17].

$$H=H^{(2)}\cdot k_z^2+H^{(1)}\cdot k_z+H^{(0)} \tag{1.14}$$

Since the z direction is the confinement direction, the quantum number k_z is then represented by $-i\frac{d}{dz}$.

$$\left[-H^{(2)}\frac{d^2}{dz^2}-iH^{(1)}\frac{d}{dz}+H^{(0)}+V(z)I_{6\times6}\right]\cdot\varphi_{n,k_x,k_y}(z)=E_n\cdot\varphi_{n,k_x,k_y}(z) \tag{1.15}$$

When the three-point finite-difference method is employed, Equation (1.15) becomes

$$H_{i,i} = H^{(2)}(\frac{1}{h_{i-1}} + \frac{1}{h_i}) \cdot (\frac{2}{h_{i-1} + h_i}) + H^{(0)} + V(z) \tag{1.16a}$$

$$H_{i,i-1} = -H^{(2)}(\frac{1}{h_{i-1}}) \cdot (\frac{2}{h_{i-1} + h_i}) + \frac{iH^{(1)}}{2} \cdot (\frac{2}{h_{i-1} + h_i}) \tag{1.16b}$$

$$H_{i,i+1} = -H^{(2)}(\frac{1}{h_i}) \cdot (\frac{2}{h_{i-1} + h_i}) - \frac{iH^{(1)}}{2} \cdot (\frac{2}{h_{i-1} + h_i}) \tag{1.16c}$$

where the index i represents each mesh point and h_i stands for the mesh size between adjacent mesh points x_i and x_{i+1}. Equation (1.16) produces an asymmetric tri-diagonal matrix if mesh spacing is non-uniform, which will result in a complex eigenvalue. In order to obtain a real-valued eigenvalue, a diagonal matrix, L, is used, as reported in literature [18].

$$L_i^2 = (h_{i-1} + h_i) \Big/ 2 \tag{1.17}$$

When we set $B = L^2 \bullet H$, then B is a Hermitian matrix because of $B_{i,i+1}=B_{i+1,i}$. By using the relation $B = L^2 \bullet H$, we can show that

$$(L^{-1}BL^{-1})L\varphi = L^{-1}LLH\varphi = (E_n)L\varphi \tag{1.18}$$

Thus, instead of solving Equation (1.16) directly, one can solve Equation (1.18) to obtain the eigenvalue E_n corresponding to the eigen-function Φ, which ensures the real-valued eigenvalues.

$$(L^{-1}BL^{-1})\Phi = (E_n)\Phi \qquad \text{where} \quad \varphi = L^{-1}\Phi \tag{1.19}$$

1.3.2 Poisson Equation

The one dimensional Poisson equation taking position dependence of dielectric constant into consideration is given by

$$\nabla \cdot (\varepsilon(z) \cdot \nabla \phi(z)) = -q \cdot (p(z) - n(z) - N_A^-(z) + N_D^+(z)) \tag{1.20}$$

where q represents elementary charge, $\varepsilon(z)$ is the position-dependent dielectric constant, and $\phi(z)$ is the electrostatic potential. Complete ionization at 300K is assumed in the simulation. The finite difference method is employed for the discretization of the Poisson equation. In a gate dielectric region, we have

$$\nabla^2 \phi(z) = 0 \tag{1.21a}$$

$$\phi_i = \frac{1}{c_1}\left(\frac{1}{x_i}\phi_{i+1} - \frac{1}{x_{i-1}}\phi_{i-1}\right) \tag{1.21b}$$

where $c_1 = \left(\frac{1}{x_i} + \frac{1}{x_{i-1}}\right)$.

In the gate dielectric and semiconductor interface, discretization of Equation (1.20) can be achieved by using the linearization scheme. The simplest way is to let $\phi^{k+1} = \phi^k + \delta$, where δ is small. As a result, we have

$$\varepsilon \nabla \cdot \nabla \delta - \frac{q}{V_T}(n+p) \cdot \delta = q(n - p + N_A^- - N_D^+) - \varepsilon \nabla \cdot \nabla \phi^k \tag{1.22}$$

where $V_T = kT/q$. After applying the finite-difference method, we have

$$\frac{\varepsilon_1 \dfrac{\delta_{i+1}-\delta_i}{x_i} - \varepsilon_2 \dfrac{\delta_i - \delta_{i-1}}{x_{i-1}}}{\frac{1}{2}(x_i + x_{i-1})} - \frac{q}{V_T}(n+p)\delta_i = q(n - p + N_A^- - N_D^+) - \frac{\varepsilon_1 \dfrac{\phi_{i+1}-\phi_i}{x_i} - \varepsilon_2 \dfrac{\phi_i - \phi_{i-1}}{x_{i-1}}}{\frac{1}{2}(x_i + x_{i-1})} \tag{1.23}$$

Equation (1.23) can be written in a simple form, that is

$$b_{i-1}\delta_{i-1} - \delta_i + a_{i+1}\delta_{i+1} = -c_i \tag{1.24}$$

$$a_{i+1} = \frac{1}{x_i\left(\dfrac{1}{x_i} + \dfrac{\Gamma}{x_{i-1}} + \dfrac{q}{\varepsilon_1}\dfrac{1}{V_T}(n+p)e_i\right)} \tag{1.25a}$$

$$b_{i-1} = \frac{\Gamma}{x_{i-1}\left(\dfrac{1}{x_i} + \dfrac{\Gamma}{x_{i-1}} + \dfrac{q}{\varepsilon_1}\dfrac{1}{V_T}(n+p)e_i\right)} \tag{1.25b}$$

$$c_i = \frac{\dfrac{1}{x_i}(\phi_{i+1} - \phi_i) + \dfrac{\Gamma}{x_{i-1}}(\phi_{i-1} - \phi_i) + \dfrac{q}{\varepsilon_1}(p - n + N_D^+ - N_A^-)e_i}{\dfrac{1}{x_i} + \dfrac{\Gamma}{x_{i-1}} + \dfrac{q}{\varepsilon_1}\dfrac{1}{V_T}(n+p)e_i} \tag{1.25c}$$

$$e_i = \tfrac{1}{2}(x_i + x_{i-1}) \tag{1.25d}$$

$$\Gamma = \frac{\varepsilon_2}{\varepsilon_1} \tag{1.25e}$$

In a semiconductor region, the discretization scheme is similar to Equation (1.23), but the value Γ is equal to 1.

1.3.3 Self-consistent Solution to Poisson and Schrödinger Equations

The simulation flow of the coupled self-consistent Poisson and Schrödinger equations is described in Fig. 1.2. The classical potential is first obtained by solving the Poisson equation where the carrier concentrations are computed by a Fermi integral. Then, the potential energy takes into account the potential due to the free charges and ionized impurities, due to the image force from different dielectric

constant between the gate dielectric and semiconductor, and due to the many-body corrections (exchange and correlation effects) [18]. We assume that the image force cancels many-body corrections in a bulk inversion layer, as reported in literature [19]. As a consequence, the potential energy includes the contribution only from the first term in our simulation. Then, with the subband energies and wave-functions obtained from the Schrödinger equation, the two-dimensional carrier concentrations can be updated. Note that we assume the wave-function penetration into the gate dielectric is zero. The subsequent iteration will yield the final self-consistent solution when the error criteria are met.

1.4 Monte Carlo Model

Material parameters of Si and Ge, including Luttinger parameters, deformation potentials, and elastic constants used in the simulation, are given in Table 1.1 [20]-[22]. Relevant scattering mechanisms, including acoustic phonon scattering and optical phonon scattering, and surface roughness scattering, are considered in the simulation [23]-26]. The scattering-matrix elements are approximated, such that phonon scattering can be considered as velocity randomizing. For an acoustic phonon, the scattering rate can be expressed as

$$S_{ac}^{m} = \frac{2\pi k_B T \Xi^2}{\hbar \rho u_l^2} \sum_n D_n(E) \cdot H_{mn}(k_{\|}, k_{\|}^{'}) \tag{1.26}$$

where Ξ is the effective acoustic deformation potential, k_B is a Boltzmann constant, T is lattice temperature, $\hbar$ is a reduced Planck constant, ρ is the material density, u_l is the longitudinal sound velocity, $D_n(E)$ is the two-dimensional density of hole states in n-th subband, and $H_{mn}(k_{\|}, k_{\|}^{'})$ is the overlap factor. We ignore the k-dependence of

the wave-functions because of relatively small errors [23]. Thus,

$$H_{mn} = \int_0^w dz \left| \varphi_{m,0}(z) \cdot \varphi_{n,0}^{\dagger}(z) \right|^2 \tag{1.27}$$

On the other hand, the optical phonon scattering rate can be expressed as

$$S_{op}^{m} = \frac{\pi (D_t K)_{op}^2}{\rho \omega_{op}} \sum_n H_{mn}(k_{\|}, k_{\|}^{'}) \cdot D_n(E \mp \hbar\omega_{op}) \cdot \frac{1 - f_0(E \mp \hbar\omega_{op})}{1 - f_0(E)} \cdot (n_{op} + \frac{1}{2} \pm \frac{1}{2}) \tag{1.28}$$

where D_tK is the average optical deformation potential, ω_{op} is the optical phonon frequency, n_{op} is the Bose-Einstein distribution, and f_0 is the Fermi-Dirac distribution. The + and – represents the absorption and emission rates. Furthermore, the formulation of the surface roughness scattering rate can be found in [23][26] and is briefly describe in Equation (1.29).

$$S_{sr} = \frac{q^2 E_{\text{eff}}^2 m_{\text{DOS}}^{\text{2D}}}{2\pi\hbar^3} \int_0^{2\pi} S(Q)(1 - \cos(\theta)) d\theta \tag{1.29a}$$

$$S(Q) = \pi \cdot \Lambda^2 \Delta^2 \Big/ \left[1 + (Q^2 \Lambda^2 / 2) \right]^3 \tag{1.29b}$$

$$Q = \left| k_i - k_f \right| \tag{1.29c}$$

where E_{eff} is the transverse effective electric field, $m_{\text{DOS}}^{\text{2D}}$ is the density-of-state effective mass, $S(Q)$ is the power spectrum of the roughness at the interface, Q is the magnitude of wave-vector change. Λ is the correlation length and Δ is the average step height. Table 1.1 shows the scattering parameters of Si and Ge, which are calibrated from a conventional Si MOSFET and from a SiGe-on-insulator device,

respectively [25].

In the numerical implementation of the valence subband structure in a Monte Carlo simulation, a tabular form of the *E-k* relationship is established. Only eigenvalues for $k_{||} < 0.6\pi/a$, which significantly contribute to the low-field channel mobility, are evaluated [26]. A flowchart of the Monte Carlo simulation can be referred to [3]. In the simulation, a single hole is simulated under an external electric field. It travels freely between two successive scatterings. The free-flight time is determined by using a fixed time technique. During the free flight, the hole is accelerated by the field and its momentum and energy are updated according to the tabular form of the *E-k* relationship. If a scattering happens, a random number, 0~1, is then generated to decide the responsible scattering mechanism and subband index. Then, the new hole state is chosen according to the sorted *E-k* relationship. This procedure is continued until the mobility fluctuation due to the statistical error is less than 0.5%.

1.5 Hole Mobility in silicon and germanium double-gate MOSFETs

1.5.1 Subband Structures in (100) Si- and Ge-channels

Fig 1.3 shows the simulated device configuration. The inversion hole density, p_{inv}, is set to be $4\times10^{12}cm^{-2}$. The 2D hole density of a 15nm Ge-channel is drawn. The wave-functions of a 10nm Si-channel and a 15nm Ge-channel are also depicted in Fig. 1.4. In Fig. 1.4, the first subband of Si-channel is the heavy hole subband, which is defined from the characteristics of the six basis functions $\left|J,m_J\right\rangle$ at the zone center (i.e. *k=0*). For example, HH1 denotes the first heavy-hole subband, in which the two heavy hole states, $\left|\frac{3}{2},\frac{3}{2}\right\rangle$ or $\left|\frac{3}{2},-\frac{3}{2}\right\rangle$, are dominant (see Fig. 1.4). Likewise, LH1 is the first light-hole subband. The lowest two subbands in a (100) Si-channel are HH1

and LH1, respectively, due to the high degree of degeneracy of heavy and light holes in Si [2]. On the other hand, the lowest two subbands in a (100) Ge-channel are HH1 and HH2. The calculated 2D hole density of state (DOS) in a Ge-channel is shown in Fig. 1.5. It is obvious that the 2D DOS is not stair-like owing to the valence band-mixing effect.

1.5.2 Hole Mobility in Si- and Ge-channels

Fig. 1.6 compares the hole mobility as a function of a body thickness in (100)/[110] Si- and Ge-channel DG-pMOSFETs. The choice of the [110] channel in Si is because it has a larger stress effect [26]. The experimental result for Si-channels is also shown for comparison [1]. The p_{inv} is set to be $4\times10^{12}cm^{-2}$. The simulated hole mobility in a Si-channel decreases monotonically with a body thickness, which is consistent with the experimental data. Unlike a Si-channel, the hole mobility in a Ge-channel shows a turn-around characteristic with a body thickness. When a body thickness reduces, the hole mobility increases gradually to a maximum around T_{Ge}=16nm, and then decreases drastically. Note that in the window of inversion hole density and body thickness considered in this work, where the transverse effective electric field is about 0.12 MV/cm in a Ge-channel, the surface roughness scattering has a minor effect on the hole mobility in a Ge-channel. The same conclusion can be found in [27]. Therefore, surface roughness scattering should not affect the existence of a mobility peak in a Ge-channel. Moreover, the calculated hole mobility at T_{Ge}=28nm is about 617 cm^2/Vs, which deviates from the bulk value of Ge. This is due to larger phonon deformation potentials in a MOSFET than in a bulk material, resulting from stress at gate dielectric and semiconductor interface [28].

The turn-around behavior of the hole mobility in a Ge-channel can be explained in the two following aspects: overlap integral and energy separation between

subbands. As a body thickness decreases, the energy difference, ΔE, between the first subband (heavy hole band) and the second subband (heavy hole band) increases owing to quantum confinement effects, as shown in Fig. 1.4 and Fig. 1.7. Because of less chance to be scattered to the second subband, inversion holes have a larger mobility owing to a smaller inter-subband scattering rate. On the other side, the intra-subband scattering rate increases due to an increase of an overlap integral. The confinement effect on the overlap integral can be understood from the illustration in Fig. 1.8. When a smaller body thickness is considered, the wave-function has a wider distribution in momentum space due to the uncertainty principle. For a fixed phonon momentum in the quantized direction q_z, only the shaded region in Fig. 1.8 contributes to the overlap integral. A broader distribution in momentum space results in a larger overlap factor (Fig. 1.7) and thus a larger intra-subband scattering rate. The interplay between inter-subband and intra-subband scatterings opens a window of a body thickness where the scattering rates can be minimized, giving rise to a peak in hole mobility, as shown in Fig. 1.6. Unlike a Ge-channel, the lowest two subbands in a (100)/[110] Si-channel are heavy-hole and light-hole bands (see Fig. 1.4), respectively, due to the high degree of degeneracy of heavy and light holes in Si [2]. For a decreasing well thickness, the larger energy separation reduces hole population in the light-hole subband and leads to a decrease of hole mobility.

1.5.3 Substrate Orientation Effect

Moreover, the substrate orientation effect in Ge-channels is evaluated. The same scattering parameters of surface roughness scattering for (100) and (110) substrates are assumed. The hole mobility in (100)/[110] and (110)/[-110] directions versus body thickness is shown in Fig. 1.9. Three points are worth noting. First, quantum confinement induced mobility enhancement is again observed in (110) substrate.

Second, the (110) substrate shows an anisotropy of energy dispersion, such that the (110)/[-110] channel direction exhibits a highest mobility, and then the (110)/[00-1] (result not shown in Fig. 1.9). The higher mobility in (110)/[-110] than in (100)/[110] is attributed to a lower conductivity effective mass. Third, the peak mobility in (110)/[-110] occurs at a smaller body thickness. This reason is that a smaller energy difference between the lowest two subbands is obtained in Ge (110) substrate (see the inset in Fig. 1.9).

1.5.4 Uniaxial Compressive Stress Effect

Finally, the effect of uniaxial compressive stress on Ge hole mobility is shown in Fig. 1.10. Note that the channel direction is also the uniaxial stress direction. The normalized hole mobility in both (100)/[110] and (110)/[-110] channel directions is evaluated in 0.3GPa uniaxial compressive stress. Generally, the uniaxial compressive stress removes the heavy hole and light hole degeneracy and alters the warping of the valence bands. As a result, the effective mass becomes anisotropic with applied stress. The constant energy contours of the first subband for (100) and (110) substrates are depicted in the figure. In Fig. 1.10, at a large body thickness, the stress induced hole mobility enhancement in (100)/[110] and (110)/[-110] channel directions is comparable due to the same bulk piezoresistance coefficients [29]. For a smaller body thickness, the quantum confinement effect plays a role and the energy difference from the uniaxial compressive stress and surface field is additive, which is responsible for the slight shift of the peak mobility.

1.6 Summary

The effects of channel/substrate orientation and uniaxial compressive stress on hole mobility versus body thickness in Ge-channel DG-pMOSFETs are investigated.

The peak mobility in both (100)/[110] and (110)/[-110] channel directions can be achieved at a certain body thickness due to the interplay between inter-subband and intra-subband scatterings. Furthermore, it is found that the hole mobility can be further improved when the uniaxial compressive stress is applied to (100)/[110] or (110)/[-110] channel direction. These findings would play a significant role for the design of the Ge-channel DG-pMOSFETs.

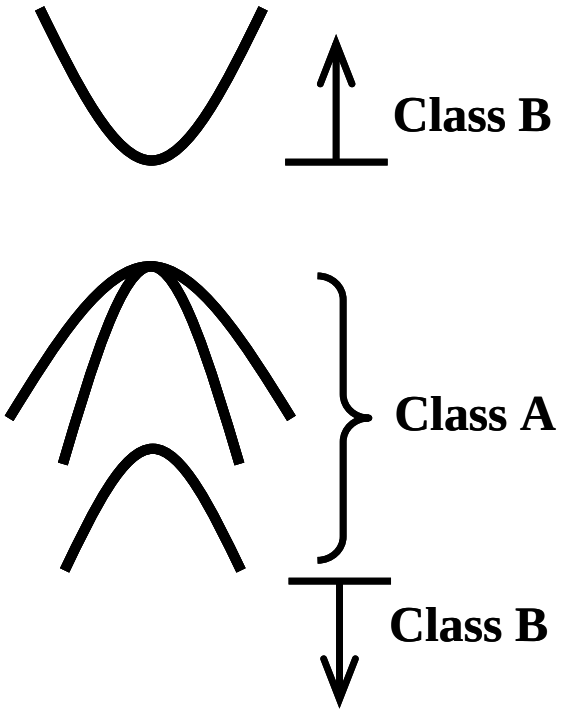

Fig. 1.1 k · p method in the Luttinger-Kohn model. The heavy-hole, the light-hole and split-off bands in double degeneracy are considered and are called class A. The rest of the bands are defined as class B.

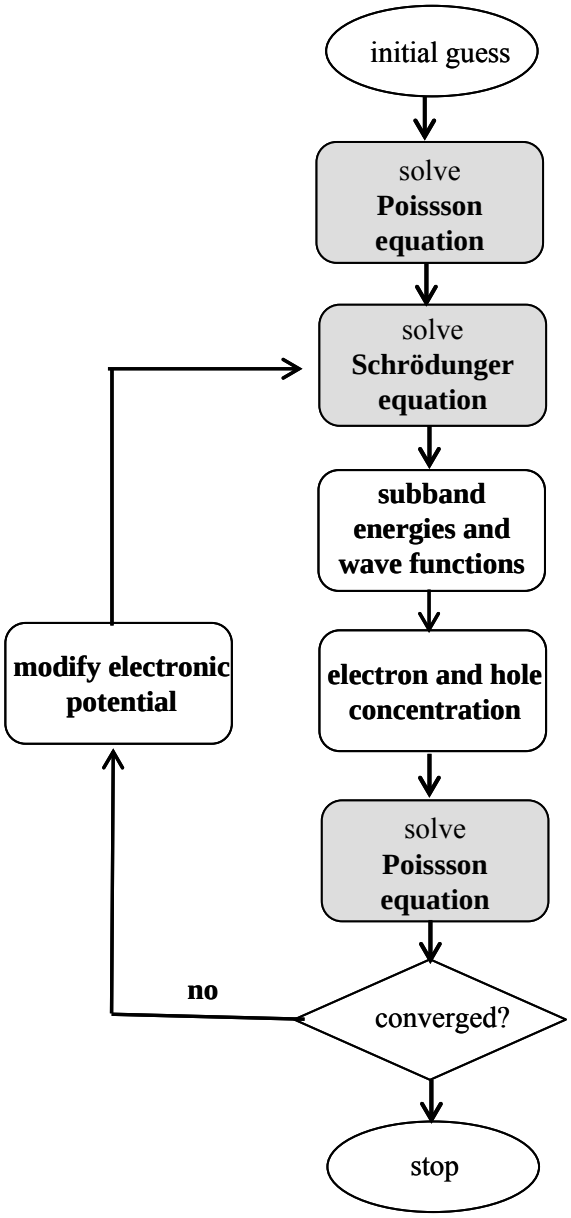

Fig. 1.2 The simulation flow for the self-consistent solution to Poisson and Schrödinger equations.

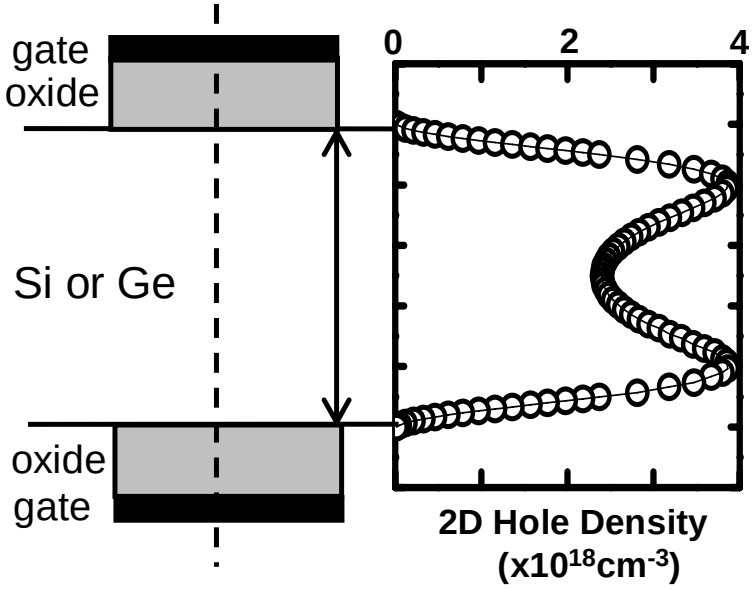

Fig. 1.3 The device configuration and 2D hole density in a (100) Ge-channel.

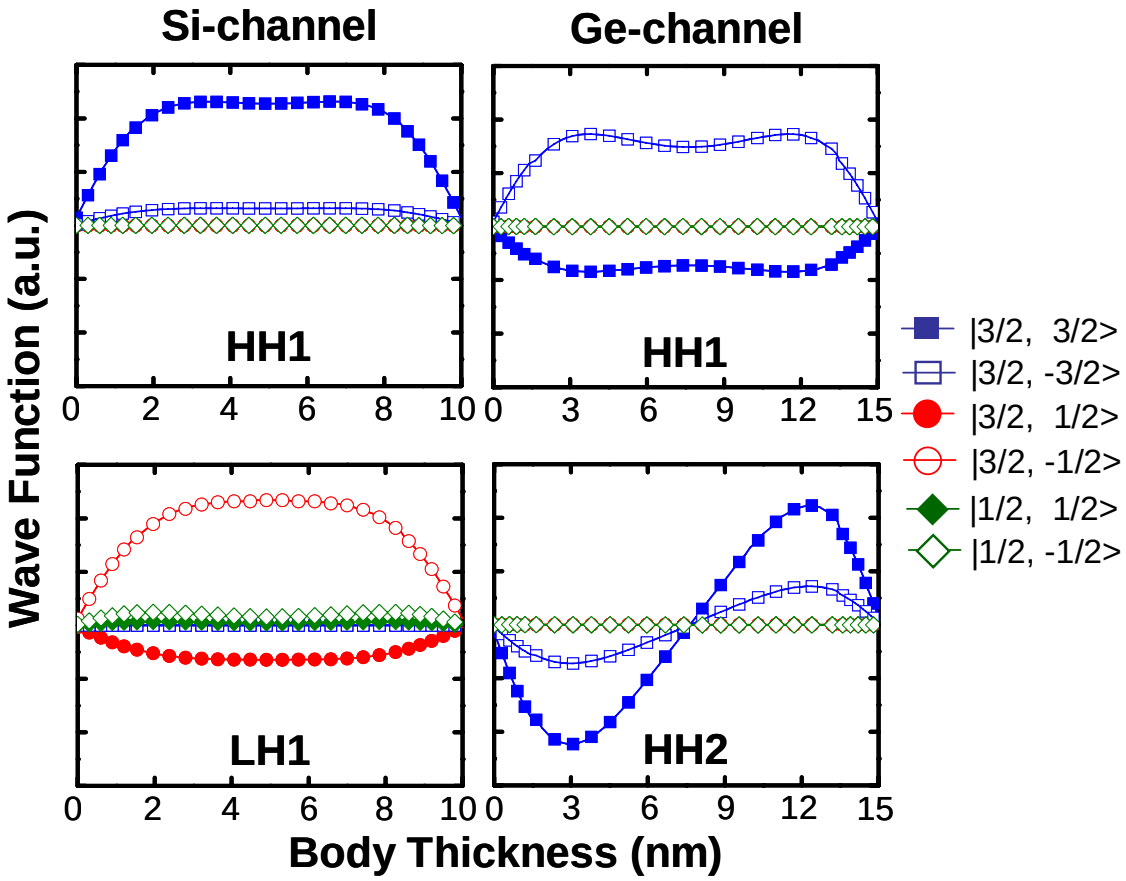

Fig. 1.4 The wave-functions at the zone center of the lowest two subbands in a Si-channel and Ge-channel

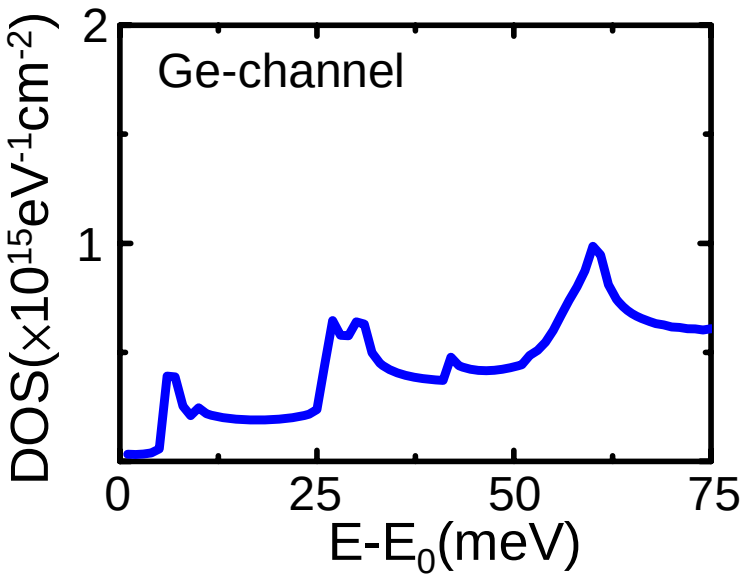

Fig. 1.5 The 2D hole density of state in a Ge-channel.

Table 1.1. The relevant material parameters and scattering parameters used in the Monte Carlo simulation for both Si and Ge. The γ_1, γ_2 and γ_3 are Luttinger parameters. The a_v, b, and d are the Bir-Pikus deformation potentials. The C_{11} and C_{12} are elastic constants. The Ξ and D_tK are the average acoustic and optical deformation potential, respectively. The $\hbar\omega$ is the phonon energy. The Δ is the average step height and the Λ is the correlation length.

	Material paramters							
	γ_1	γ_2	γ_3	a_v (eV)	b (eV)	d (eV)	C_{11} (dyn/cm^2)	C_{12} (dyn/cm^2)
Si	**4.285**	**0.339**	**1.446**					
Ge	**13.38**	**4.24**	**5.69**	**2.0**	**-2.2**	**-4.4**	**1.2853×10^{12}**	**4.826×10^{11}**

	Scattering paramters				
	Ξ (eV)	D_tK (10^{8}eV/cm)	$\hbar\omega$ (meV)	Δ (nm)	Λ (nm)
Si	**9.2**	**13**	**62**	**0.32**	**3.0**
Ge	**11**	**6**	**38**	**0.368**	**3.0**

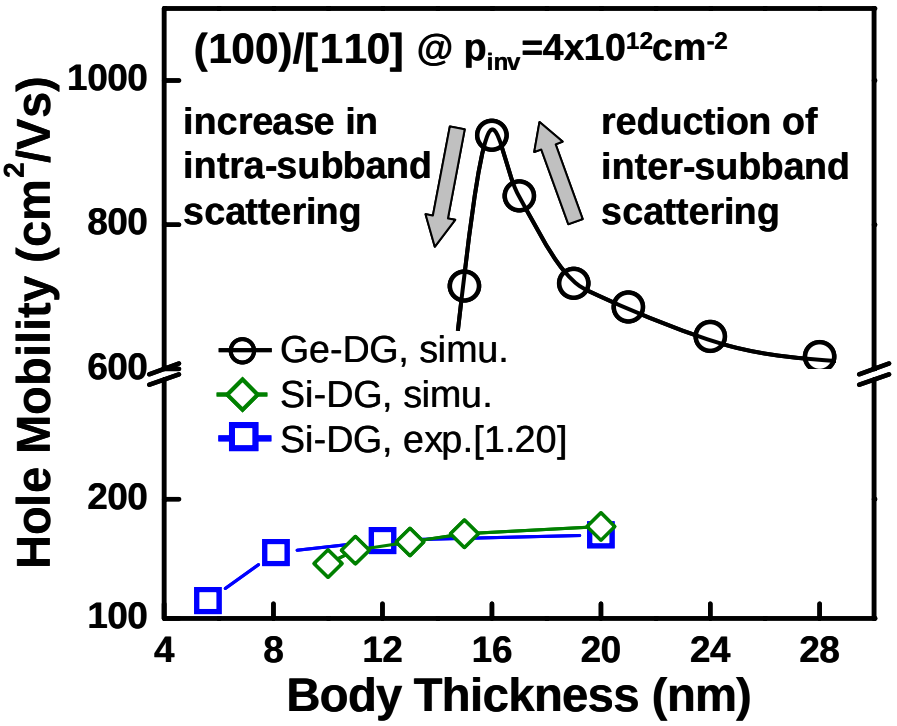

Fig. 1.6 Simulated hole mobility as a function of a body thickness in (100)/[110] Si- and Ge-channel DG-pMOSFETs. The experimental result for Si-channels is plotted for comparison.

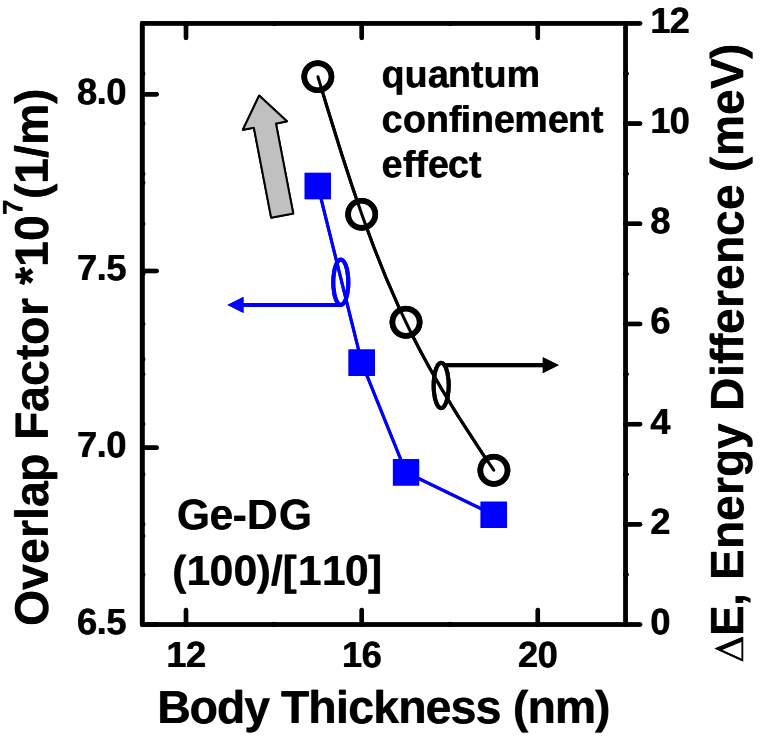

Fig. 1.7 The body thickness dependence of an overlap factor and an energy difference between the lowest two subbands in (100)/[110] Ge-channel DG-pMOSFETs.

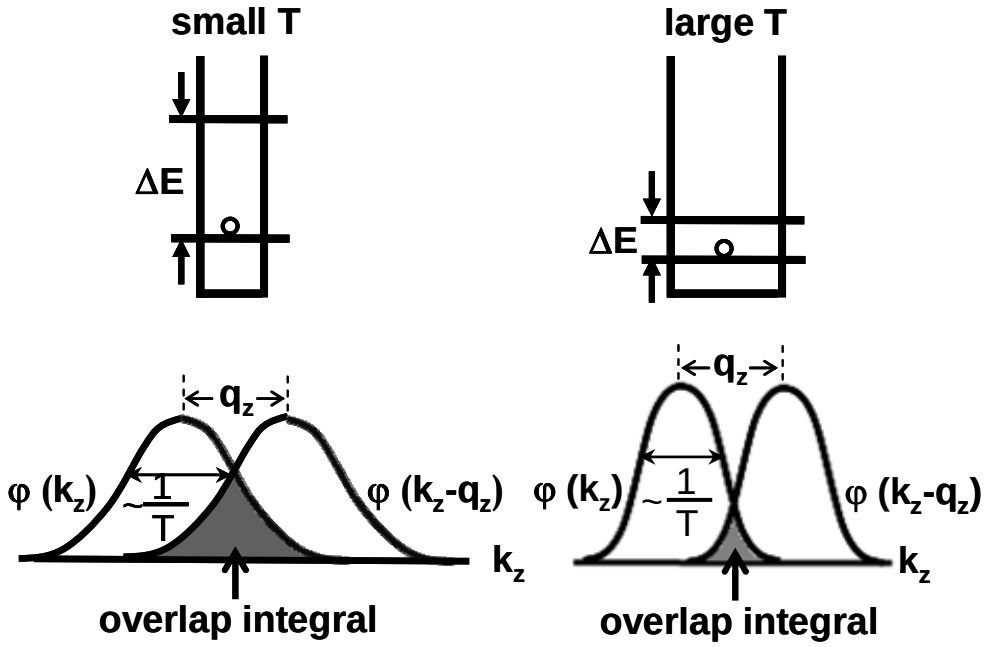

Fig. 1.8 Illustration of the body thickness dependence of valence subband energy and overlap factor. The shaded region corresponds to an overlap integral. A narrower quantum well has a larger energy separation between subbands and a larger overlap factor.

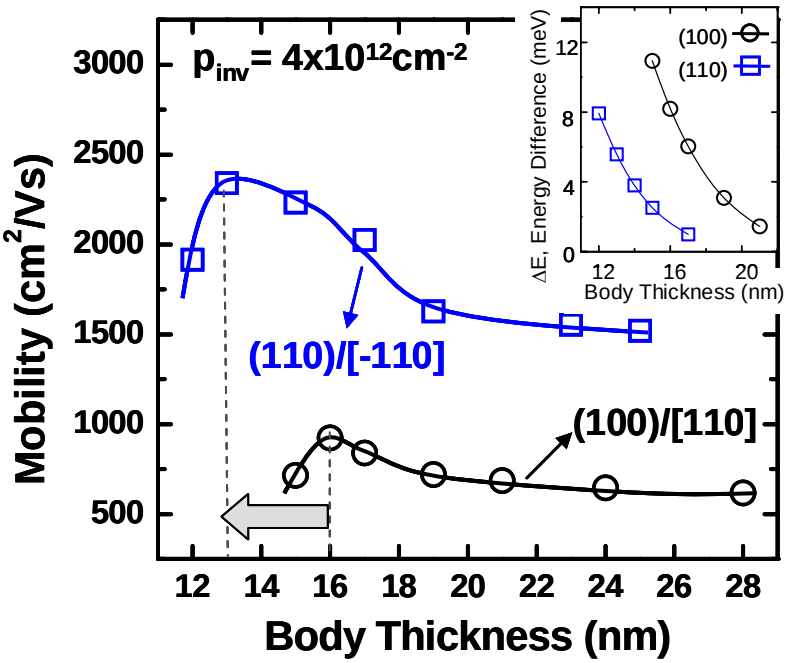

Fig. 1.9 Comparisons of the hole mobility and subband energy difference in (100)/[110] and (110)/[-110] Ge-channels.

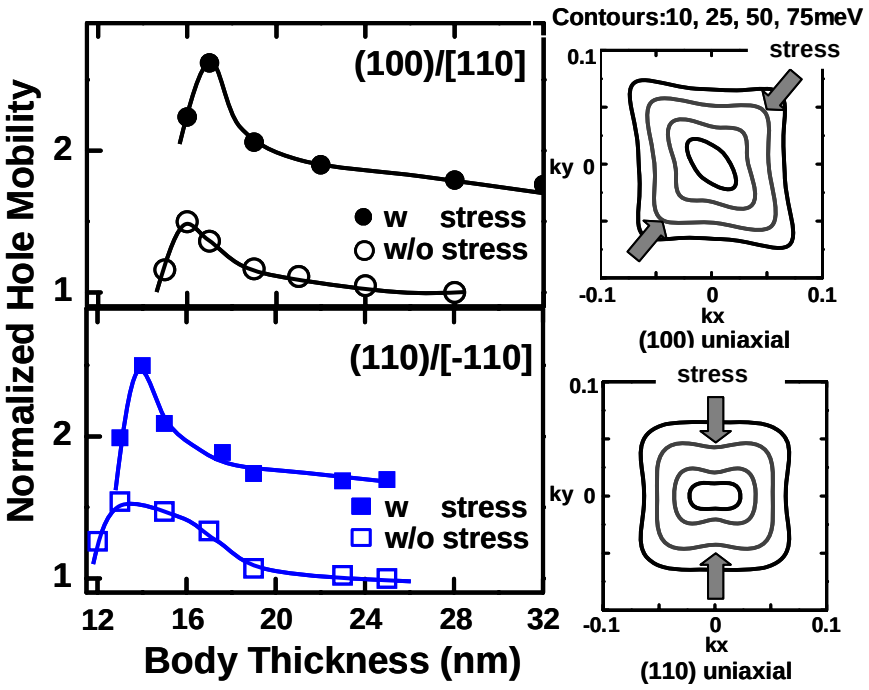

Fig. 1.10 Ge hole mobility as a function of a body thickness in (100)/[110] and (110)/[-110] channel directions with and without an uniaxial compressive stress of 0.3GPa. The mobility is normalized to the one without stress effect. The constant energy contours in (100) and (110) substrates are also plotted.

Chapter 2

Bipolar Charge Trapping Induced Anomalous Negative Bias-Temperature Instability in HfSiON Gate Dielectric pMOSFETs

2.1 Preface

Negative bias temperature (NBT) instability has been recognized as a major reliability concern in ultra-thin gate dielectric MOSFETs. It occurs in p-type devices and manifests itself as negative shifts of threshold voltage due to positive oxide charge trapping and interface generation under a negative gate voltage stress. Compared to a SiO_2 gate dielectric, the NBT instability (NBTI) in high permittivity (high-*k*) gate dielectric pMOSFETs has been less explored.

In previous NBTI studies [30]-[32], a conventional "stress-and-sense" method was used, which introduces a switching delay between stress and sense of up to a few seconds. For high-*k* gate dielectrics such as HfSiON, a significant post-stress transient effect was reported due to high-*k* dielectric charge trapping/detrapping. The ignorance of high-*k* charge trapping/detrapping in a switching delay may lead to an erroneous interpretation of measurement data and underlying physical mechanisms. Thus, to retrieve the important information between stress and sense, a fast transient measurement technique [33][34] with a resolution of microseconds is employed. By using this technique, the mode of the NBT-induced drain current instability is characterized. Both current enhancement and degradation modes are observed in a HfSiON pMOSFET [35]. A physical model based on bipolar charge trapping and trap

generation in a high-*k* gate dielectric is proposed to explain the instability modes.

The devices used here are p-type MOSFETs with a polysilicon electrode and a HfSiON-SiO_2 gate stack. The gate length ranges from 0.08μm to 1.2μm, and the gate width ranges from 0.16μm to 10μm. The physical thickness of the high-*k* layer and the interfacial SiO_2 layer (IL) is 2.5nm and 1.4nm, respectively. The equivalent oxide thickness is 1.8nm. Detailed fabrication process and device characteristics were reported in [36][37]. To reduce the switching delay in characterization, our measurement system is computer-automated, including high-speed switches, an operational amplifier, and a digital oscilloscope, as shown in Fig. 2.1. The high speed switches minimize a switching delay down to microseconds between stress and drain current measurement. The detailed measurement procedures were described in [33][34]. Other measurement techniques, such as charge pumping (CP) technique, single charge emission measurement and carrier separation measurement are utilized to monitor charge trapping/detrapping and trap generation.

In this work, the negative bias temperature induced drain current instability is first characterized in control SiO_2 pMOSFETs. The BTI in HfSiON nMOSFETs and pMOSFETs are also shown for a comparative study. Then, the dependence of stress time, gate voltage and temperature on drain current instability in HfSiON pMOSFETs is investigated. We propose a bipolar charge trapping model along with trap generation to explain the observed phenomena. Finally, three characterization methods, single charge emission, charge pumping and carrier separation measurement are utilized to justify the model.

2.2 Anomalous Turn-around in Linear Drain Current Evolutions

The V_g/V_d waveforms in the transient measurement are depicted in Fig. 2.2 during stress phase and measurement phase. Fig. 2.3 shows the evolutions of NBT

stress-induced linear drain current change ($\Delta I_{d,lin}$) in control SiO_2 and HfSiON pMOSFETs. The device dimension is W/L=10μm/0.2μm. The stress V_g is -2.8V, and the linear drain current ($I_{d,lin}$) is measured at V_g/V_d= -1.2V/-0.2V. As shown in the figure, $\Delta I_{d,lin}$ decreases monotonically with stress time in a SiO_2 control device, while a turn-around characteristic of $\Delta I_{d,lin}$ versus stress time is obtained in a HfSiON pMOSFET. Note that one may fail to observe this anomalous turn-around behavior by using a conventional measurement setup such as Agilent 4156 due to a switching delay of up to a few seconds. Furthermore, the NBTI and its counterpart PBTI in a nMOSFET are compared in Fig. 2.4. The stress V_g is -2.8V for the pMOSFET and 2.2V for the nMOSFET. As shown in the figure, the $\Delta I_{d,lin}$ in a nMOSFET (PBTI) is negative in the entire stress period and no turn-around feature like the NBTI is observed. More interestingly, the NBTI and the PBTI in HfSiON MOSFETs exhibit distinctly different post-stress drain current evolutions in Fig. 2.5. The PBTI exhibits a drain current recovery, as reported in literature [33]. However, the NBTI shows persistent drain current degradation after stress. The post-stress $I_{d,lin}$ degradation in a high-*k* pMOSFET implies trapped electron emission from a high-*k* gate dielectric after stressing V_g is removed.

In Fig. 2.6 and Fig. 2.7, NBT induced $\Delta I_{d,lin}$ at various stress V_g and temperatures are shown, respectively. The stress V_g ranges from -1.6V (result not shown in Fig.2.6) to -2.8V with all other terminals grounded and the temperature is from 25°C to 125°C. For a stress V_g weaker than -2V (selectively shown for clarity), $\Delta I_{d,lin}$ is negative (degradation mode) and decreases monotonically with stress time. The degradation aggravates with a larger stress $|V_g|$ (more negative). For a stress V_g stronger than -2V or a higher stress temperature, the drain current instability shows a different feature. The $I_{d,lin}$ initially increases with stress time (enhancement mode) and shortly evolves into degradation mode ($\Delta I_{d,lin}<0$), featuring a turn-around characteristic. The drain

current enhancement has a positive dependence on stress $|V_g|$ and temperature. The transition time for the $I_{d,lin}$ evolving from enhancement mode to degradation mode is mostly within seconds in the bias range of interest. Fig. 2.8 demonstrates the dependence of $\Delta I_{d,lin}$ on stress V_g at different stress times. For t=0.1s, a lower stress $|V_g|$ (-1.4V~ -2V) induces a $I_{d,lin}$ degradation while a larger stress $|V_g|$ results in an enhancement. This trend remains for t=10s, but the turn-around $|V_g|$ is slightly increased. For a longer stress time (e.g., t=1000s), the dependence of $\Delta I_{d,lin}$ on V_g returns to a normal degradation mode as in SiO_2 gate dielectric transistors, and a larger stress $|V_g|$ results in a larger degradation [38][39]. The stress temperature dependence of $\Delta I_{d,lin}$ is shown in Fig. 2.9. For a short stress time (e.g., t=10s), $\Delta I_{d,lin}$ changes from negative at low temperatures to positive at high temperatures. But for a longer stress time (e.g., t=1000s), the $I_{d,lin}$ degradation increases monotonically with stress temperature. The positive temperature dependence of the $I_{d,lin}$ degradation in a high-*k* MOSFET can be realized due to temperature accelerated high-*k*/IL trap generation because of thermo-chemical reaction [40].

2.3 Bipolar Charge Trapping Model

In a negative V_g stress, two carrier injection processes affect I_d instability, (i) valence band electron injection from the p^+ poly-gate into high-*k* traps (I_d enhancement mode) and (ii) hole injection from the inverted channel into high-*k*/IL traps (I_d degradation mode). Therefore, available trap states in a high-*k* dielectric, either pre-existing traps or stress generated traps, and injected carrier fluence should be considered in a NBT instability model. Fig. 2.10 illustrates the energy band diagrams in equilibrium (Fig. 2.10(a)) and in various NBT stress conditions, for example, low V_g and low temperature stress (Fig. 2.10(b)), low V_g and high temperature stress (Fig. 2.10(c)), and high V_g and low temperature stress (Fig.

2.10(d)). In thermal equilibrium, trap states with energy (E_t) below the Fermi level (E_F) are occupied by electrons while those above E_F are empty. The shaded area in Fig. 2.10 represents the occupied states in the high-*k* layer. When a low stress $|V_g|$/ temperature is applied (Fig. 2.10(b)), the empty high-*k* traps available for poly-gate valence electron injection are very limited due to a small band-bending (ΔE_t) in a high-*k* gate dielectric. In this case, electron trapping into the high-*k* layer is negligible, and $\Delta I_{d,lin}$ is dominated by hole injection from the inverted channel, leading to a $I_{d,lin}$ degradation. In this regime, a larger $|V_g|$ aggravates $\Delta I_{d,lin}$ due to a larger hole injection current, which is in agreement with our measured result in Fig. 2.8. As stress temperature or $|V_g|$ increases, more poly-gate electrons can inject into pre-existing high-*k* traps either because of thermally assisted tunneling (Fig. 2.10(c)) or because of more available empty states due to a larger band-bending (Fig. 2.10(d)). In these stress conditions, both electron trapping and hole trapping into the high-k layer are possible. The measurement result in Fig. 2.6 and Fig. 2.7 implies that electron trapping is dominant in the initial stress period and hole trapping gradually supersedes electron trapping due to new hole trap creation in the high-*k* and IL layers, thus resulting in a turn-around feature of the $I_{d,lin}$ evolution.

2.4 Single Charge Emission and Charge Pumping

To confirm our bipolar charge trapping model for NBT instability, post-stress trapped charge emissions are characterized. The purpose of this characterization is to identify injected charge species during stress. The detail of this method was described in our previous papers for trapped electron emission from HfSiON in a nMOSFET [33] and trapped hole emission from SiO_2 in a pMOSFET [41]. Fig. 2.11 shows our measured post-stress I_d evolution patterns in small area devices after low (-1.5V) and high (-2.2V) V_g stress, respectively. The transistors have W/L=0.16μm/0.08μm. The

waveforms are shown in Fig. 2.12. The stress time (or exactly the charge filling time) for both cases is 0.2s, and the post-stress measurement condition is V_g~V_t to magnify the effect of single charge on drain current and V_d= -0.2V. In Fig. 2.11, trapped charge emission is manifested by a staircase-like jump in the drain current. For a pMOSFET, an upward shift (increase in $|I_d|$) corresponds to a single hole emission, and a downward shift corresponds to a single electron emission. Notably, only trapped hole emissions are found for the low V_g stress (Fig. 2.11(a)) while both electron and hole emissions are obtained for the high V_g stress (Fig. 2.11(b)). This single charge emission result provides direct evidence of bipolar charge trapping in a high V_g stress condition. Fig. 2.13 shows the single charge emission induced current jumps in a post-PBT stress nMOSFET. Only three trapped electrons are observed and the post-stress drain current exhibits full recovery. It should be remarked that we did not observe any random telegraph signal at the post-stress measurement biases, indicating that the observed current jumps in Fig. 2.11 are attributed to injected charge emissions.

We also characterize high-*k*/IL trap generation for low and high V_g stress by using a charge pumping method. A two-frequency (5kHz and 1MHz) technique is used to separate IL/Si interface traps (D_{it}) from bulk high-*k* traps (N_{HK}) [42]. The characterization procedure is described in Fig. 2.14. The high frequency CP current is contributed by D_{it} and the difference between the CP currents of the two frequencies reflects high-*k* trap density N_{HK}.

$$N_{HK} = \frac{1}{WLq}\left[\frac{(I_{CP}@5kHz)}{5kHz} - \frac{(I_{CP}@1MHz)}{1MHz}\right]$$

Fig. 2.15 shows the extracted D_{it} and N_{HK} versus stress time for stress V_g=-1.5V

and -2.2V. No new traps are created in a low V_g (-1.5V) stress even for a stress time of t=1000s, indicating that the $I_{d,lin}$ degradation at a low stress V_g is mainly attributed to hole trapping into pre-existing high-*k* traps. On the other side, both interface trap and bulk high-*k* trap generation is observed in a high V_g (-2.2V) stress.

2.5 Carrier Separation Measurement

In addition to available traps for electron and hole injection, another factor affecting NBT instability mode is the fluence of injected carriers during stress. A carrier separation measurement was performed to explore the effect of injected carrier fluence on I_d instability. Fig. 2.16 illustrates the carrier separation measurement and the carrier flow in a high-*k* pMOSFET under $-V_g$ stressing. The hole injection current from the inverted channel constitutes the source/drain current (i.e., $I_{S/D}$) and the electron injection current from the p^+ poly-gate flows to the substrate (i.e., I_{sub}). Both can be measured separately through the connected source and drain measurement configuration. Fig. 2.17(a) shows the measured hole and electron currents versus stress gate voltage at T=25°C. One point is worth noting. Holes are the dominant conduction carrier at a low stress $|V_g|$. As a stress $|V_g|$ increases, an electron current becomes dominant. Thus, electron filling effect is more significant than hole filling at a higher stress $|V_g|$. This trend is consistent with the measured result in Fig. 2.8, i.e, $I_{d,lin}$ degradation in a low V_g region and $I_{d,lin}$ enhancement in a high V_g region in the initial stress period.

As stress temperature increases to 100°C (Fig. 2.17 (b)), the electron current is enhanced to a larger extent, compared to the hole current and thus it supersedes the hole current at a smaller stress V_g. This result is in agreement with our thermally-assisted electron tunneling model in Fig. 2.10(c) and can well explain the increased $I_{d,lin}$ enhancement at a higher temperature in a low stress V_g region (Fig.

2.7).

2.6 Summary

Various NBT induced drain current instability modes in a pMOSFET with a HfSiON-SiO_2 gate stack are investigated by using a fast transient measurement method. The drain current enhancement is observed in the initial stress period in a high stress V_g or at a high temperature. Electron trapping, hole trapping and new trap generation are found to be responsible for the drain current instability modes. The impact of stress V_g, temperature and stress time on NBT instability is characterized. The drain current instability modes are summarized in Table 2.1. In high $|V_g|$ and/or high temperature stress, electron trapping into pre-existing high-*k* traps is dominant in the initial stress period, thus causing an I_d enhancement. As stress continues, hole injection and new hole trap creation in HK/IL layers eventually become dominant, giving rise to a turn-around characteristic of the drain current evolution with time. For low V_g stress, the I_d instability is dictated by hole injection throughout the entire stress period, and thus $\Delta I_{d,lin}$ decreases monotonically with stress time. In order to extrapolate a reliable NBTI lifetime, the above mechanisms should be carefully considered in a voltage-accelerated stress.

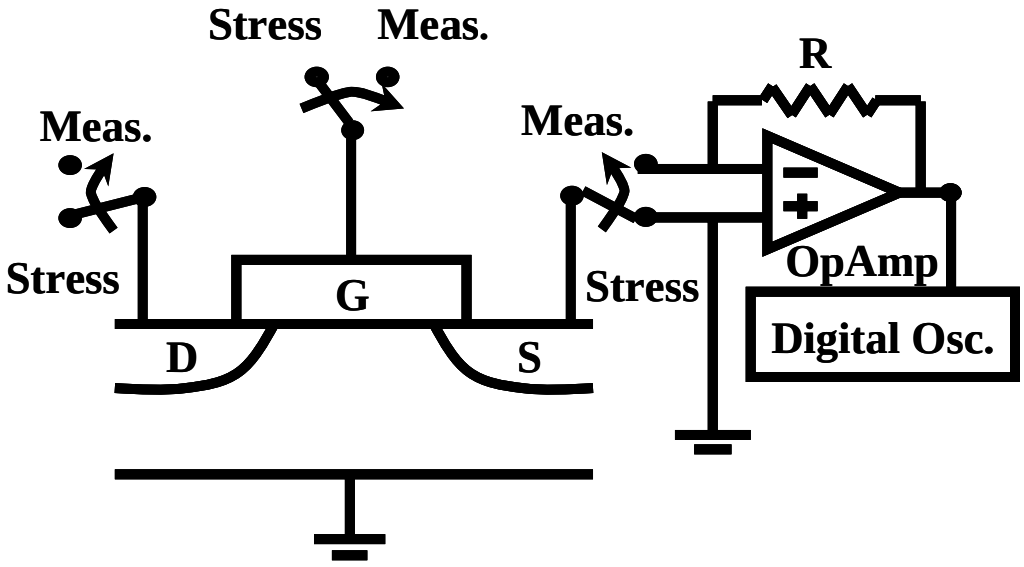

Fig. 2.1 Schematic diagram for the transient measurement system. The high speed switches minimize a switching delay down to microseconds between stress and drain current measurement.

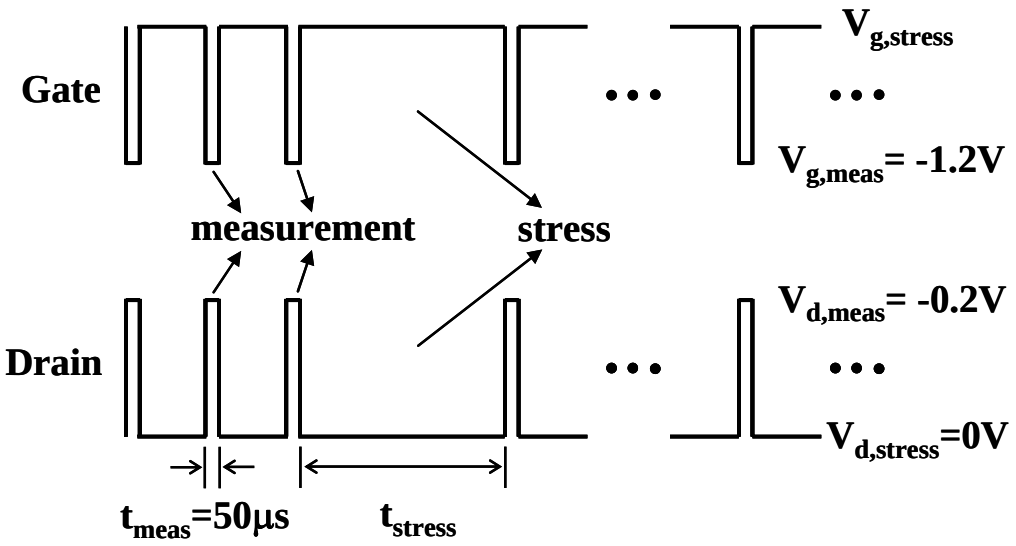

Fig. 2.2 The waveforms applied to the gate and drain in the transient measurement.

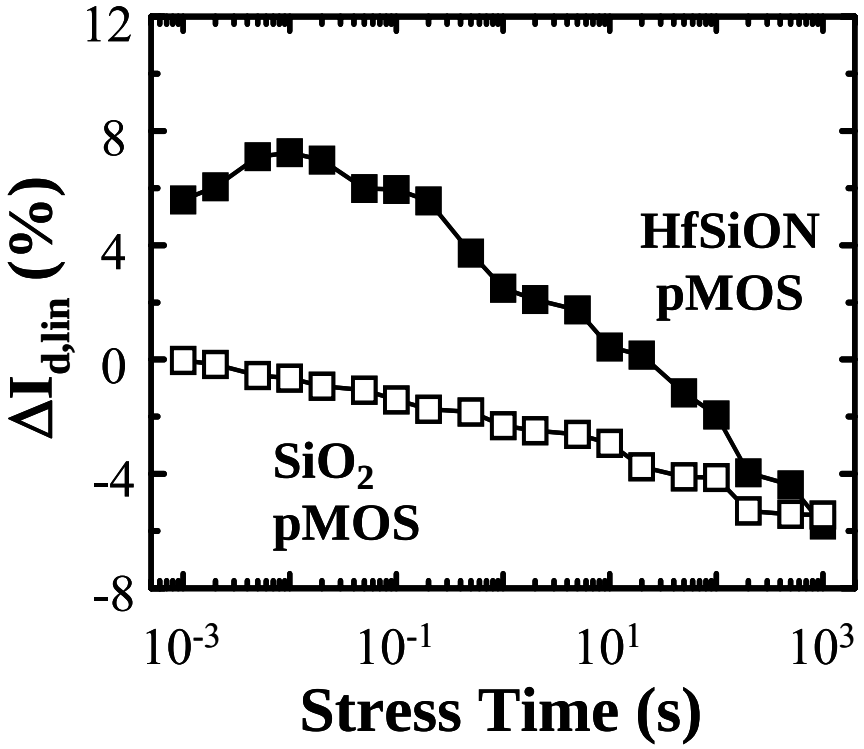

Fig. 2.3 NBT stress induced linear drain current change ($\Delta I_{d,lin}$) in SiO_2 and HfSiON pMOSFETs. The stress V_g is -2.8V and the linear drain current ($I_{d,lin}$) is measured at V_g/V_d=-1.2V/-0.2V.

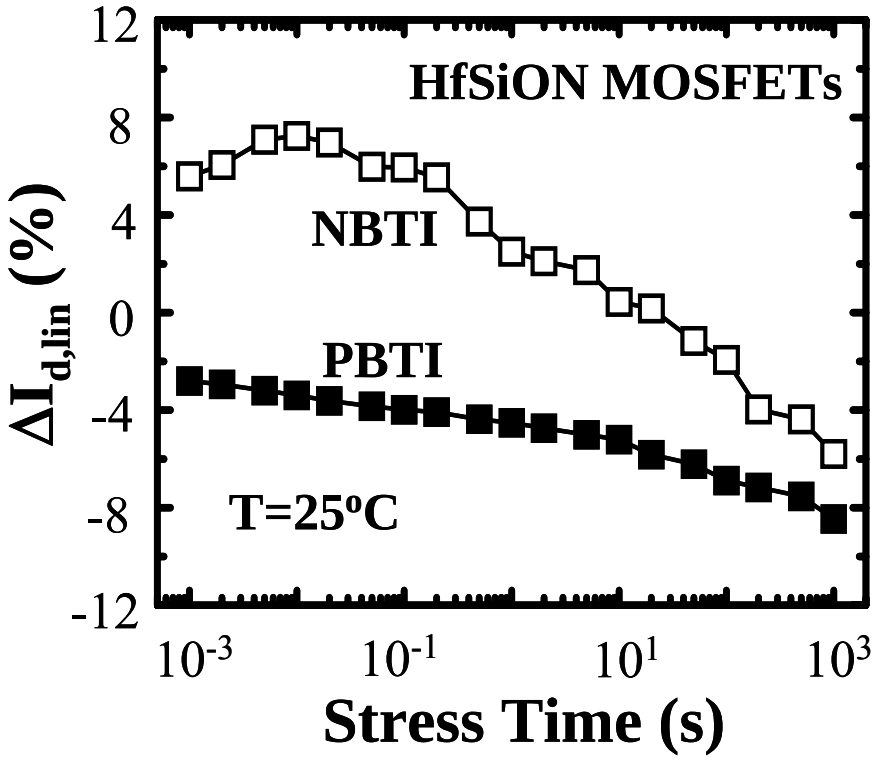

Fig. 2.4 Linear drain current change ($\Delta I_{d,lin}$) in a pMOSFET (NBTI) and in a nMOSFET (PBTI). The stress V_g is -2.8V for the pMOSFET and 2.2V for the nMOSFET.

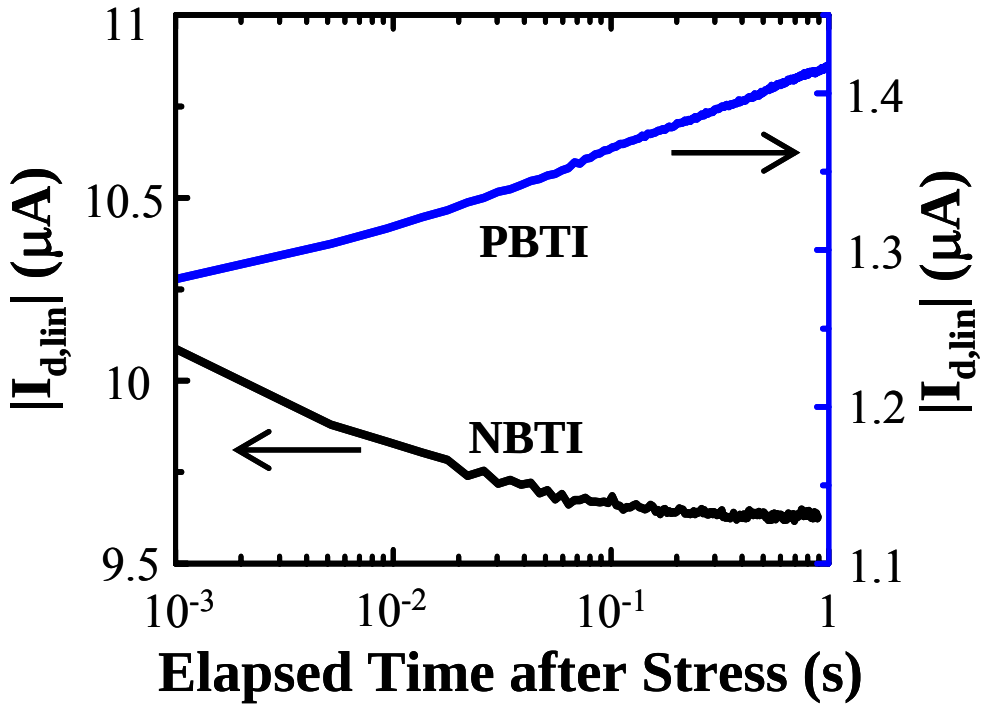

Fig. 2.5 $|I_{d,lin}|$ as a function of elapsed time after stress. The drain current recovery is observed in a nMOSFET, while the NBTI shows persistent post-stress current degradation.

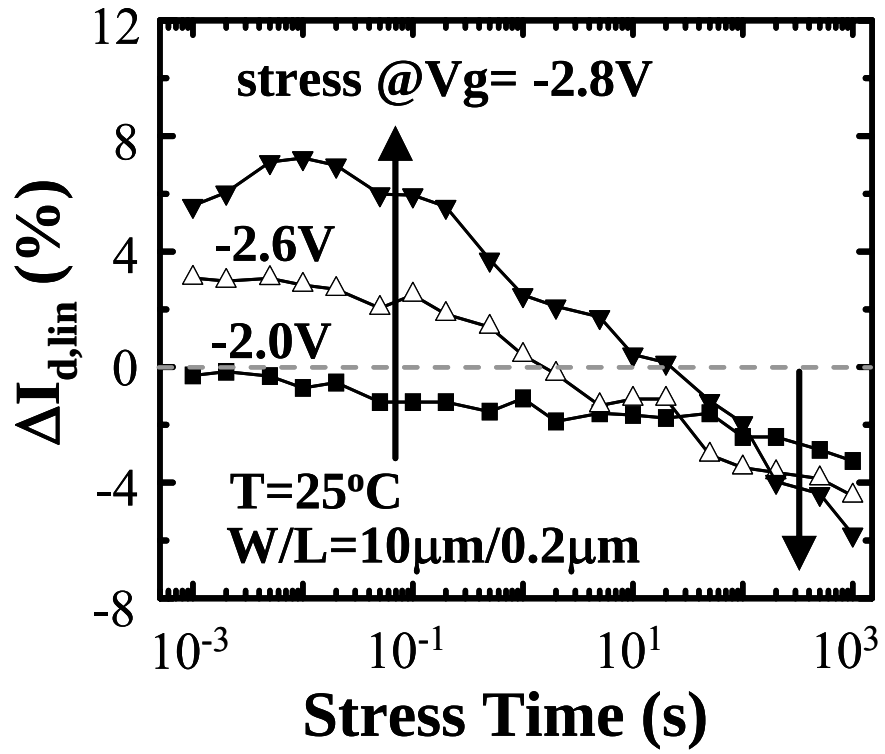

Fig. 2.6 NBT stress induced drain current evolution for different stress V_g. Drain current enhancement in an initial stage of stressing is observed for high stress V_g (-2.6V and -2.8V).

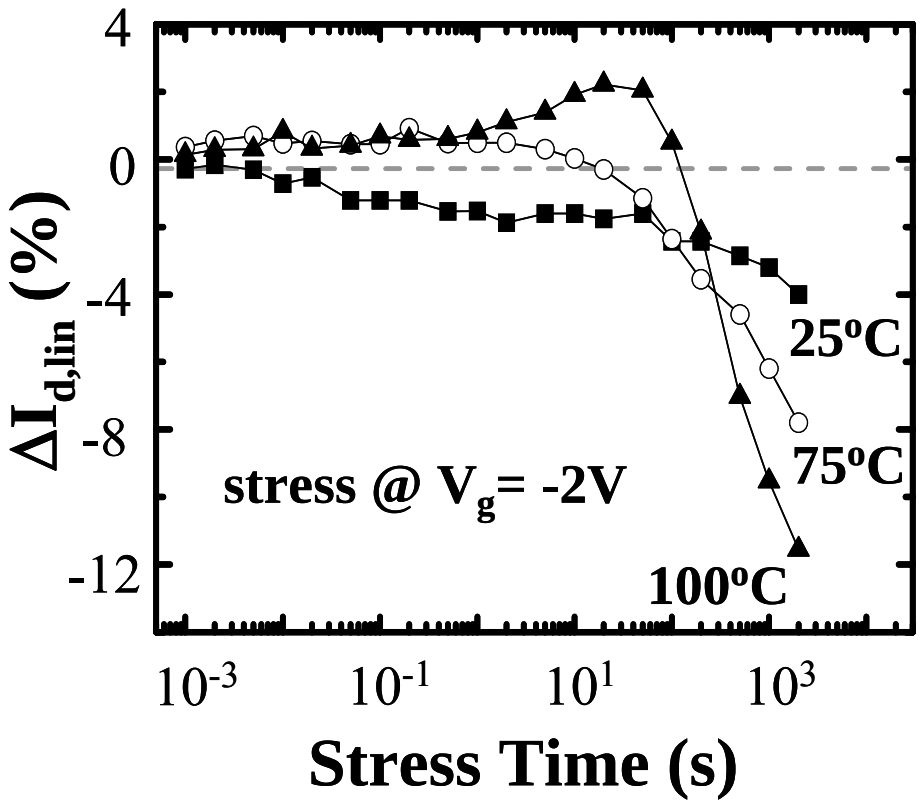

Fig. 2.7 NBT stress induced drain current evolution for different stress temperatures. Drain current enhancement in an initial stage of stressing is observed for high stress temperatures.

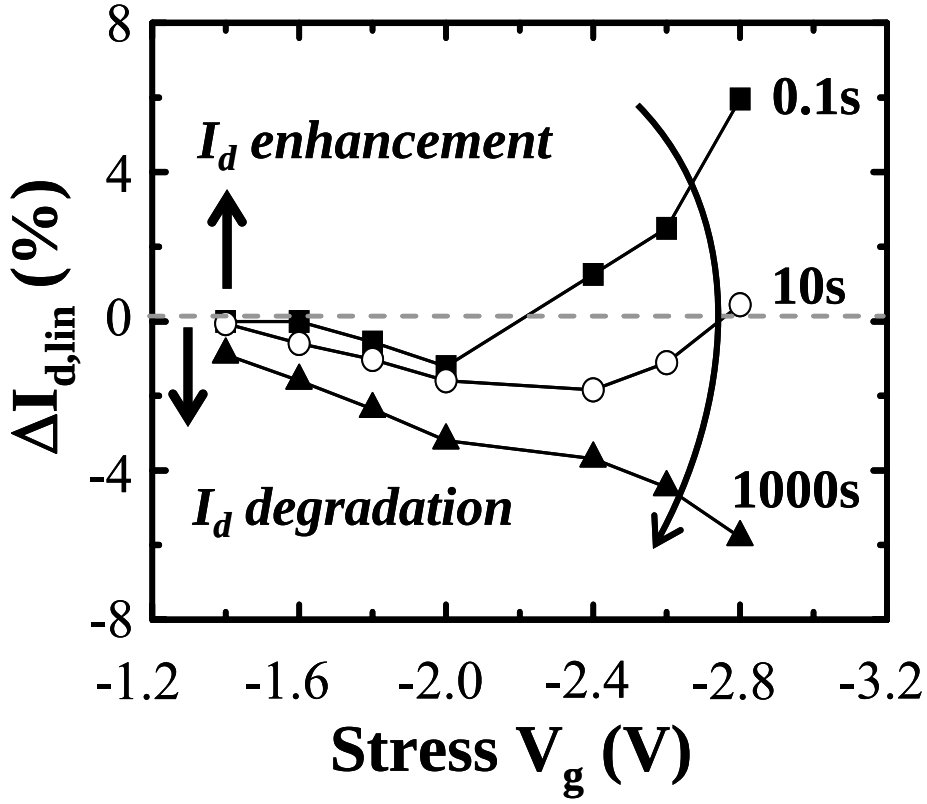

Fig. 2.8 Stress V_g dependence of $\Delta I_{d,lin}$ at different stress times. For a short stress time (t=0.1s and 10s), $\Delta I_{d,lin}$ can be positive or negative, depending on stress V_g. For a longer stress time (t=1000s), the dependence returns to a normal degradation mode as in SiO_2 gate dielectric transistors.

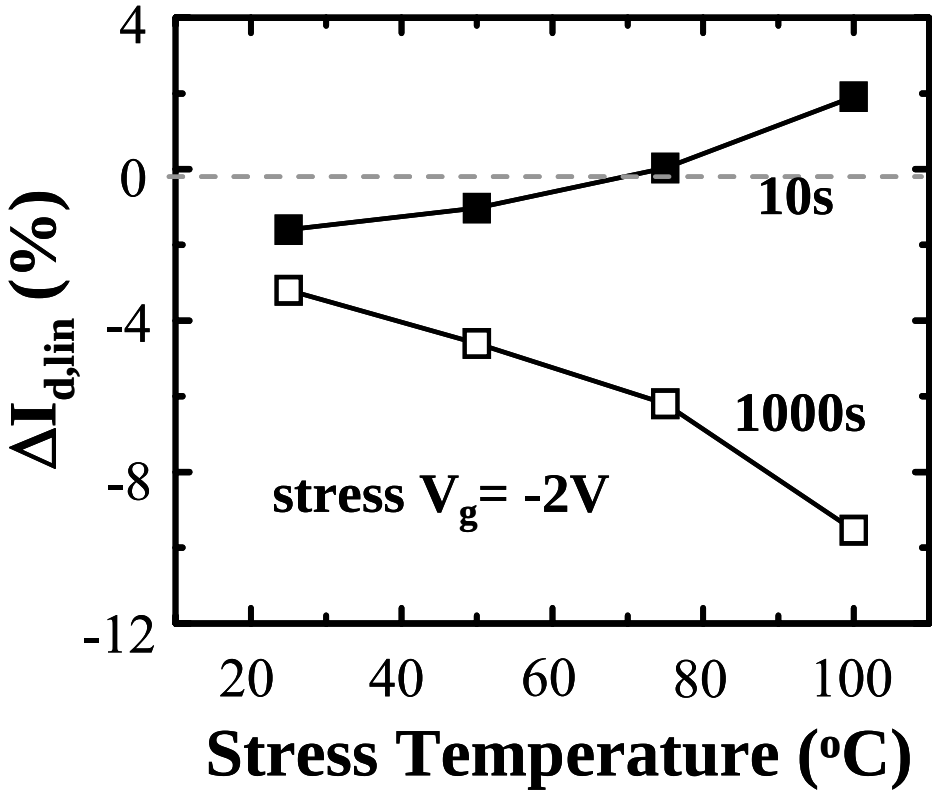

Fig. 2.9 Stress temperature dependence of $\Delta I_{d,lin}$.

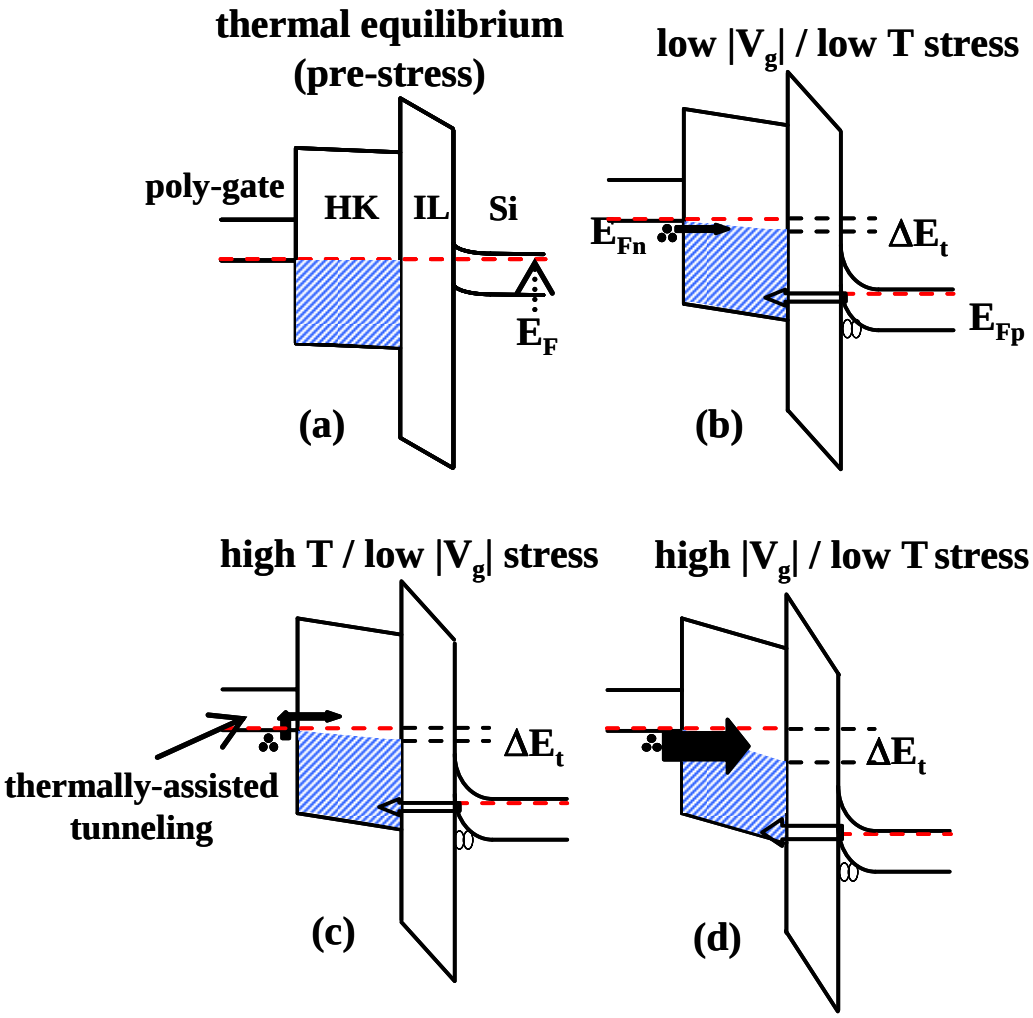

Fig. 2.10 Schematic representation of an energy band diagram and charge injection processes in (a) thermal equilibrium, (b) low $|V_g|$/ low T stress, (c) high T/ low $|V_g|$ stress, and (d) high $|V_g|$/ low T stress. The shaded area represents the occupied trap states in the high-*k* layer. Electron injection from the poly gate and hole injection from the channel are illustrated.

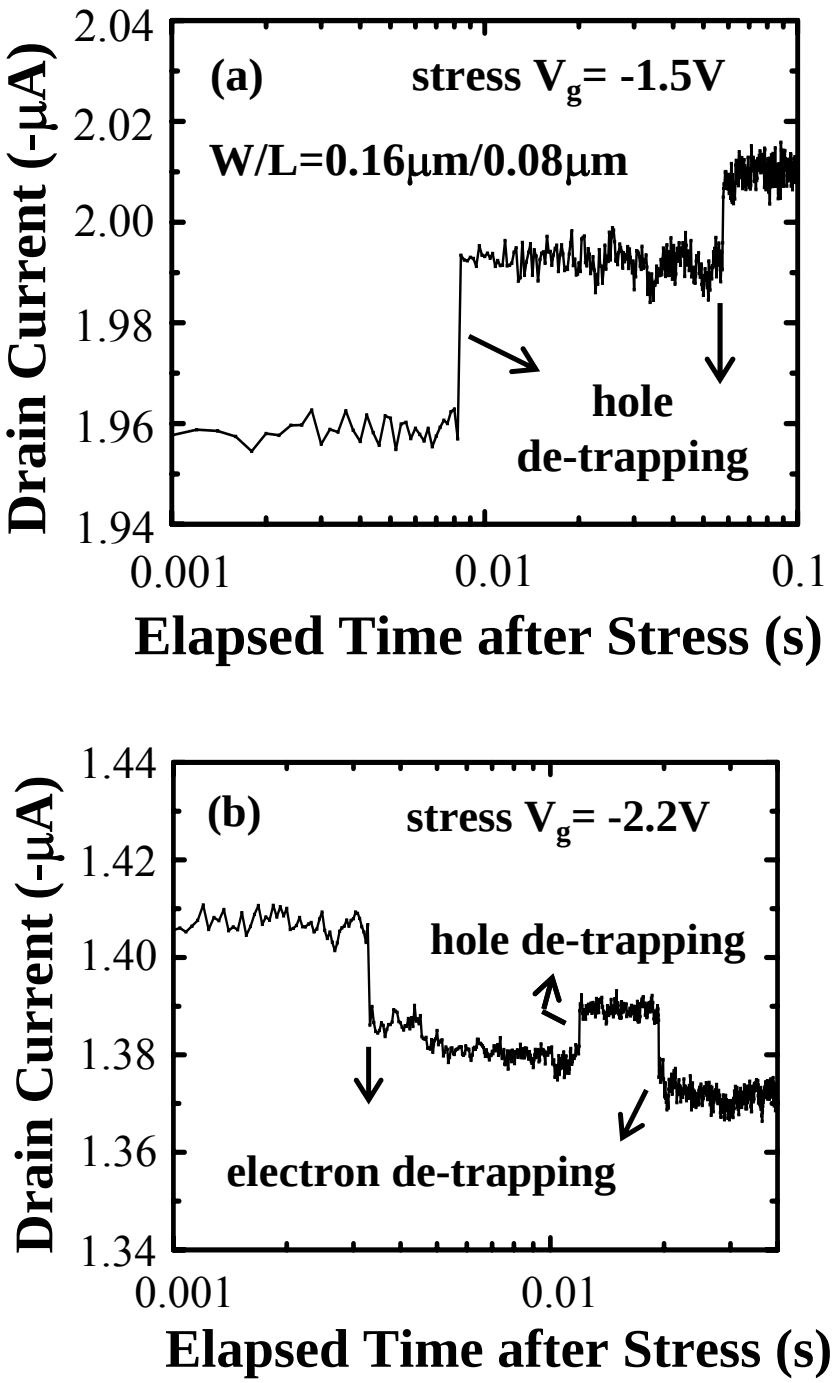

Fig. 2.11 Post-stress I_d evolution patterns in small-area devices after (a) a low $|V_g|$ (-1.5V) stress and (b) a high $|V_g|$ (-2.2V) stress. The post-stress measurement condition is $V_g \sim V_t$ and V_d=-0.2V.

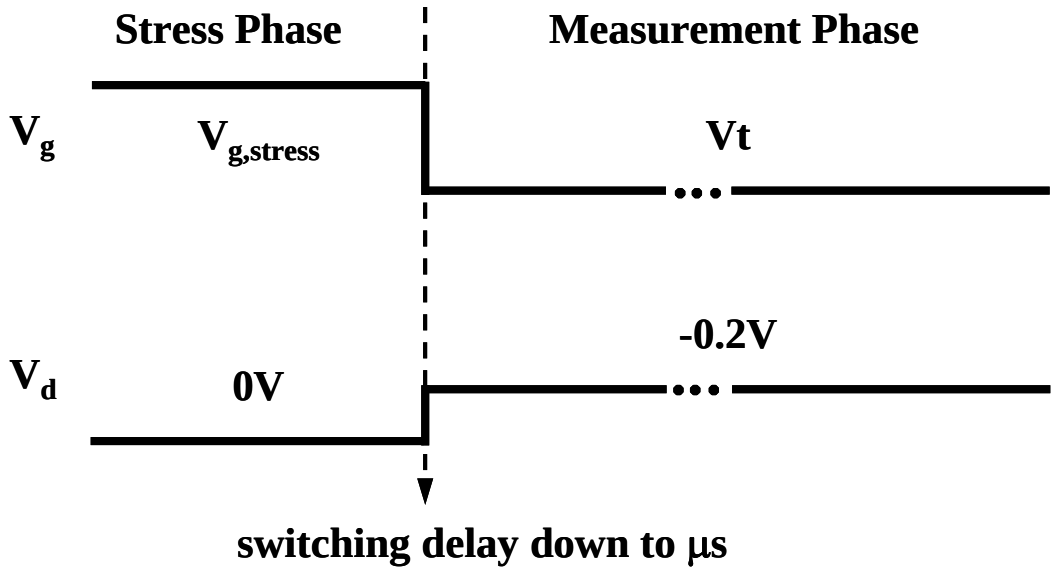

Fig. 2.12 The waveforms used in Fig. 2.11 applied to the gate and drain during stress phase and measurement phase.

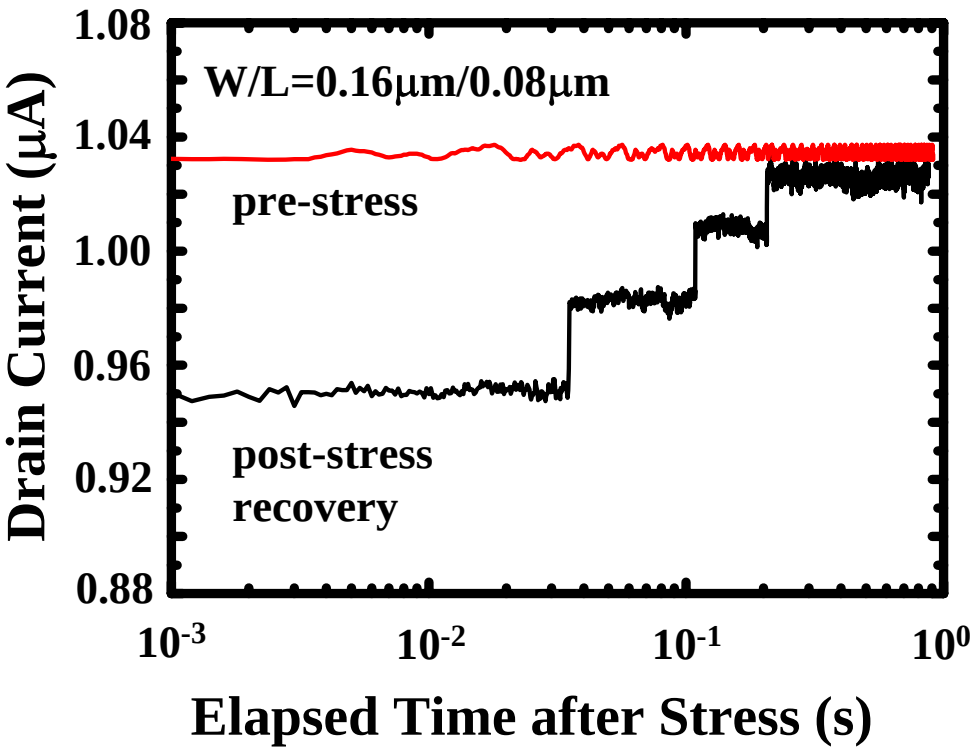

Fig. 2.13 Post-stress I_d evolution patterns after stress at V_g=0.7V for 0.2s in a nMOSFET. The post-stress measurement condition is V_g/V_d=0.3V/0.2V.

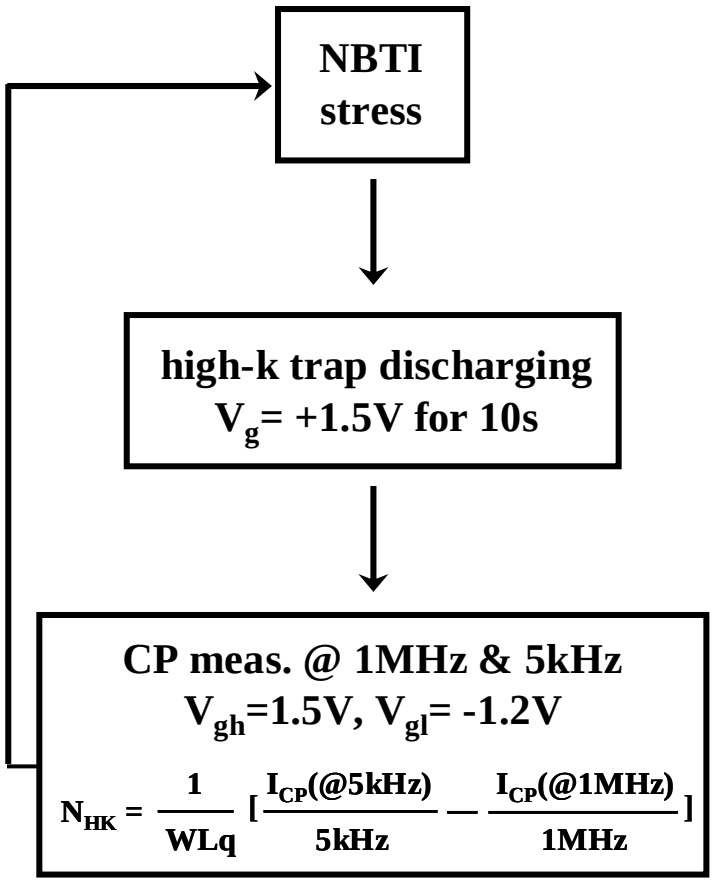

Fig. 2.14 The characterization procedures of two-frequency charge pumping technique for high-*k* trap density extraction.

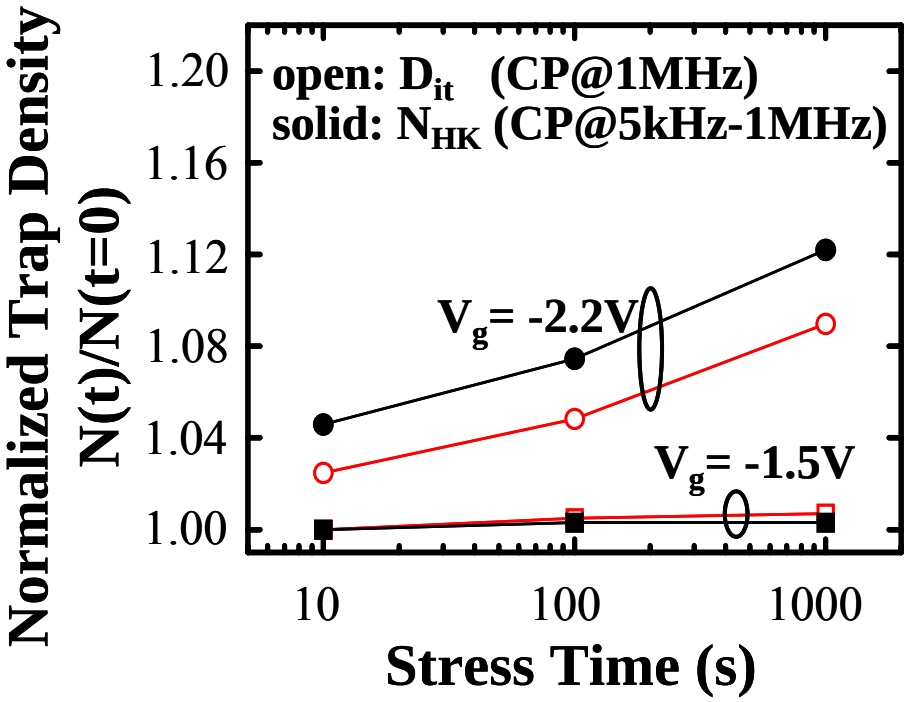

Fig. 2.15 Interface traps (D_{it}) and bulk high-*k* traps (N_{HK}) growth rates in NBT stress at Vg=-1.5V and Vg=-2.2V.

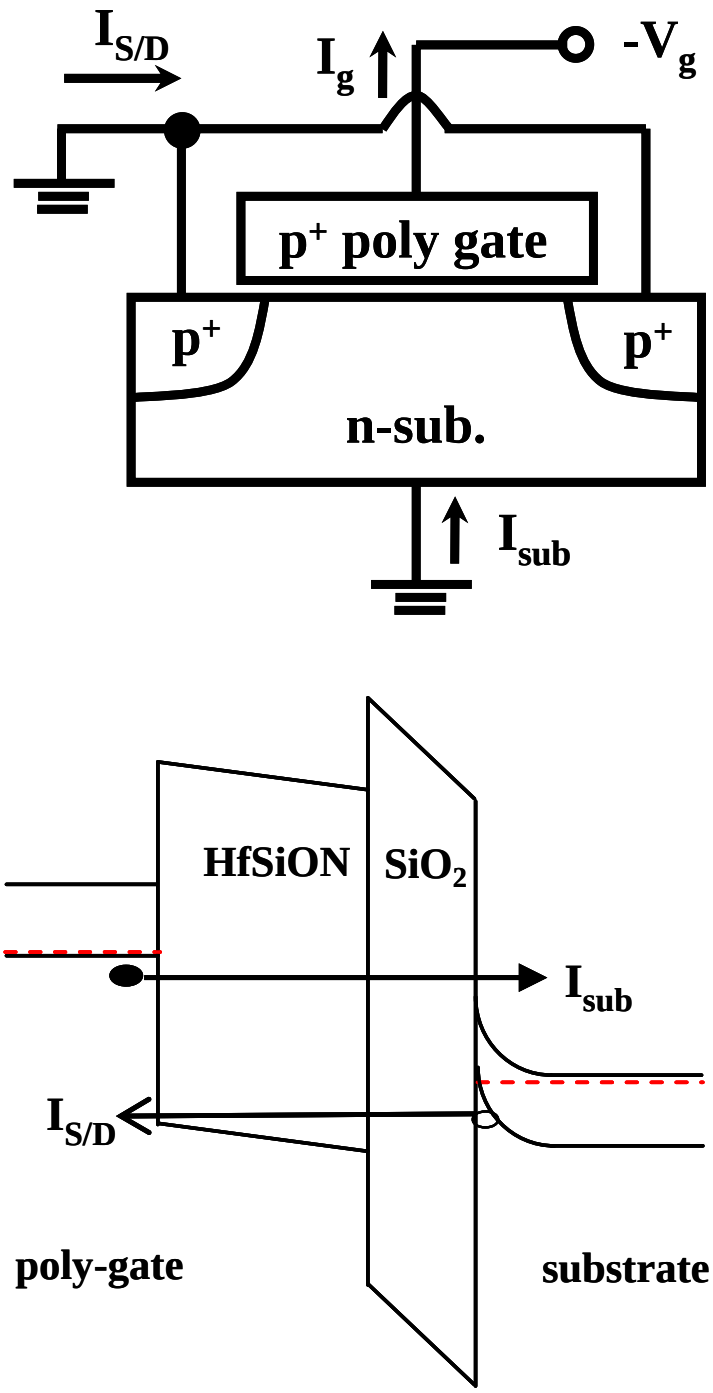

Fig. 2.16 Illustration of charge separation measurement and carrier flow in a high-*k* pMOSFET under $-V_g$ stressing. I_{sub} denotes the electron injection current from the p^+ poly-gate to substrate, and $I_{S/D}$ stands for hole injection current from the inverted channel. Both can be measured separately through the connected source and drain measurement configuration.

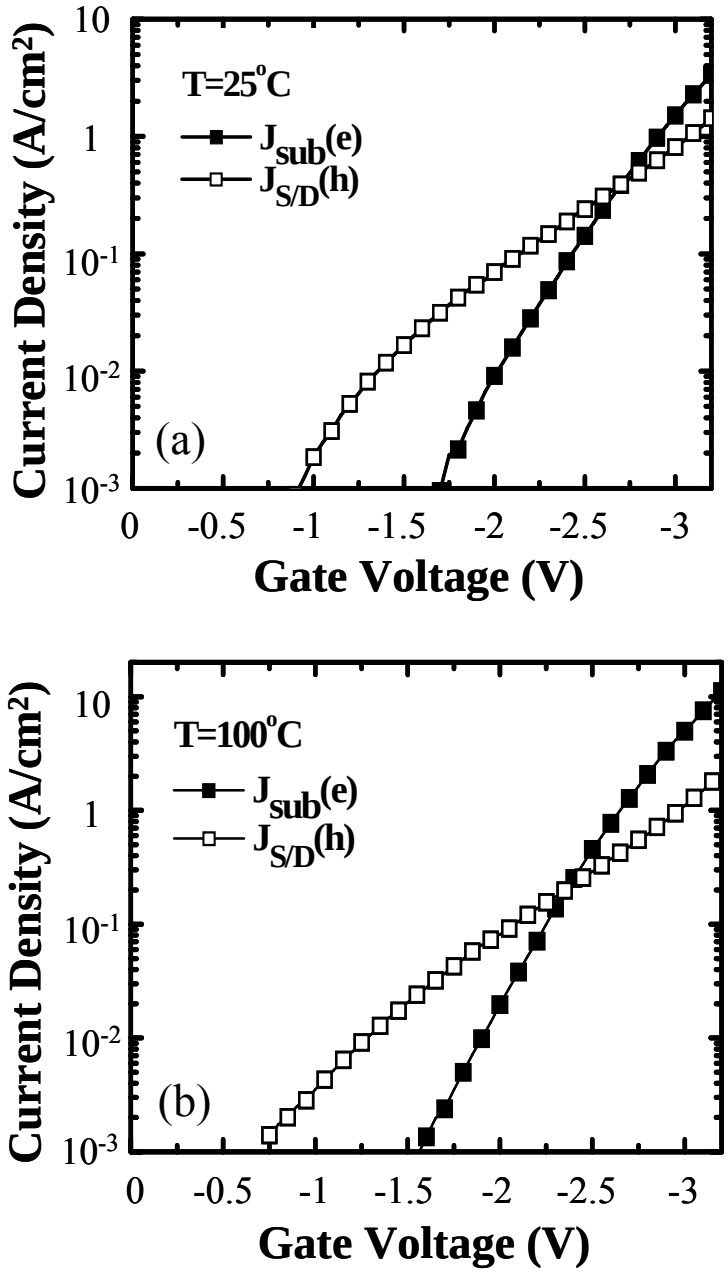

Fig. 2.17 Gate voltage dependence of hole injection current ($I_{S/D}$) and electron injection current (I_{sub}) in a high-*k* pMOSFET, measured at (a) T=25°C and (b) T=100°C.

Table 2.1 Summary of NBT stress caused drain current instability and responsible mechanisms.

Stress $\lvert V_g \rvert$ and T / Stress Time	low $\lvert V_g \rvert$	high $\lvert V_g \rvert$	high temperature
short	1.Hole trapping into HK traps 2.I_D degradation	1.Electron trapping into HK traps 2.Hole trapping into HK traps 3.I_D enhancement	1.Electron trapping into HK traps via thermally assisted tunneling 2.Hole trapping into HK 3.I_D enhancement
long	1.Hole trapping 2.HK/IL degradation 3.I_D degradation	1.Electron/ hole trapping 2.HK/IL degradation 3.I_D degradation	1.Electron/ hole trapping 2.Accelerated HK/IL degradation 3.I_D degradation

Chapter 3

Impact of Self-Heating Effect on Hot Carrier Degradation in High-Voltage LDMOS

3.1 Preface

Laterally diffused MOS (LDMOS) transistors have been widely utilized in today's high-voltage/high-current drivers and RF power amplifiers [43][44]. Due to large power consumption, self-heating effect (SHE) is significant in a LDMOS. In this paper, we will study SHE on hot carrier degradation in DC and AC stress modes. To this purpose, we fabricate a special LDMOS structure, which incorporates a metal contact in the bird's beak region. Thus, we can probe an internal voltage (V_I) transient due to SHE directly. Fig. 3.1 illustrates the device structure. Three regions of a LDMOS are indicated in the figure, including a channel region, an accumulation region and a field-oxide region. The contact is arranged in the accumulation region that the internal voltage V_I can be used as a monitor for hot carrier effects in the channel. The contact area is small enough that the device electrical characteristics are not affected.

The device was processed in a 0.18μm CMOS technology with a gate oxide thickness of 100nm and a channel length of 3μm. The operation voltages are V_g=40V and V_d=40V. To eliminate SHE in measurement, a fast transient measurement setup including a digital oscilloscope is built, as shown in Fig. 3.2. Linear drain current (I_{dlin}@V_g/V_d=40V/0.1V) is measured to monitor device degradation under AC/DC stress. A three-region charge pumping technique [45][46] is used to locate hot carrier damage area in the device and to identify the type of generated oxide traps.

Two-dimensional device simulation is performed to calculate a temperature distribution and corresponding hot carrier effects.

3.2 Self-Heating Characterization

Fig. 3.3(a) shows a normalized drain current (I_d/W) versus V_d in small and large gate width devices in DC (Agilent 4156) measurement. The I_d/W in a linear region is nearly the same, indicating no process variations in these two devices. However, the larger width device exhibits a smaller I_d/W in the saturation region because of larger power consumption and thus a larger SHE. The reduction of the saturation current is attributed to self-heating induced mobility degradation [47][48]. Fig. 3.3(b) compares the I_d/W from a DC and from a fast transient measurement for the large width device. A larger I_d/W is noticed in the transient measurement because of the elimination of SHE. In addition, SHE is manifested in the internal voltage measurement results by Agilent 4156 and by the fast transient setup (Fig. 3.4). The larger V_I in a non-SHE condition is attributed to a higher mobility in accumulation region, thus resulting in a smaller drift region resistance. A larger internal voltage in non-SHE condition implies a stronger hot carrier stress in the channel region.

3.3 Degradation Characteristics in AC/DC Stress

Two stress modes (max. I_B, and max. I_g) are chosen in the study of hot carrier degradation in n-LDMOS. The I_g-V_g and I_B-V_g of a n-LDMOS are shown in Fig. 3.5. Fig. 3.6 shows AC and DC stress induced I_{dlin} degradations in the above two stress modes. Max. I_B stress shows a slight difference in I_{dlin} degradation between AC and DC stresses, implying that SHE is not important at a lower stress V_g. However, in maximum I_g stress, AC stress shows much more I_{dlin} degradation than DC stress. Moreover, strong stress-frequency (Fig. 3.7(a)) and duty cycle (Fig. 3.7(b))

dependence is observed. In Fig. 3.7(a), the I_{dlin} degradation increases with frequency and then becomes saturated. A corner frequency is found to be f1=20 kHZ at a duty cycle=10%. In Fig. 3.8, we plot I_{dlin} degradation versus pulse duration, i.e., duty cycle/frequency, in AC stress. A corner time of ~5μs is obtained, suggesting that SHE becomes important as pulse duration is longer than ~5μs.

Fig. 3.9 shows a V_I transient in a pulsed gate and DC drain voltage condition. The V_I decreases with time due to SHE and the onset time of SHE is extracted to be around 5μs. This result is consistent with the findings from AC stress induced degradation (Fig. 3.8).

3.4 Discussion

A charge pumping measurement (I_{cp}) result is shown in Fig. 3.10. A distinguished three-stage feature in I_{cp} $-V_{gL}$ is observed, corresponding to the three regions of a LDMOS respectively. By comparing the pre-stress and post-stress I_{cp} in each stage, we are able to separate interface trap (N_{it}) and fixed oxide charge (Q_{ox}) creation in each region of the device. The result in Fig. 3.10 reveals that AC stress generates more N_{it} in the channel region and more Q_{ox} in the accumulation region. The larger trap generation rate in AC stress results from a smaller temperature rise and thus a larger stress gate current (Fig. 3.11). The self-heating induced temperature change in a LDMOS is simulated by a two-dimensional numerical device simulation (Fig. 3.12). The ambient temperature in the simulation is 300K. In Fig. 3.12, the drift region shows a higher temperature change than channel region, implying a larger mobility degradation and thus a higher drift region resistance. The SHE is stronger at a higher V_g. The simulation also reveals a higher V_I in a non-SHE condition (Fig. 3.13). Good agreement between measurement and simulation is obtained in Fig. 3.13. Because of a larger V_I in the non-SHE condition, the simulated impact ionization rate

is stronger in the non-SHE condition (Fig. 3.14). This feature also confirms our charge-pumping results in Fig. 3.10 and concludes a more serious I_{dlin} degradation rate in AC stress (Fig. 3.15).

3.5 Summary

Transient self-heating effect in AC hot carrier stress in LDMOS has been studied by measuring an internal voltage. The extracted self-heating time is around 5μs. The AC stress at maximum I_g yields the worst hot carrier degradation because of the elimination of self-heating effect.

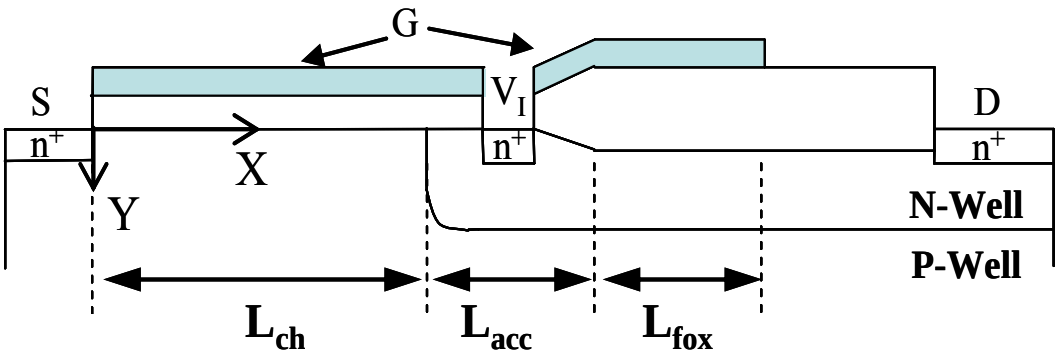

Fig. 3.1: Cross-section of a novel LDMOS structure. The metal contact (V_I) is arranged in the accumulation region with a n^+ implant. Three regions are indicated, including channel region (L_{ch}), accumulation region (L_{acc}), and field-oxide region (L_{fox}).

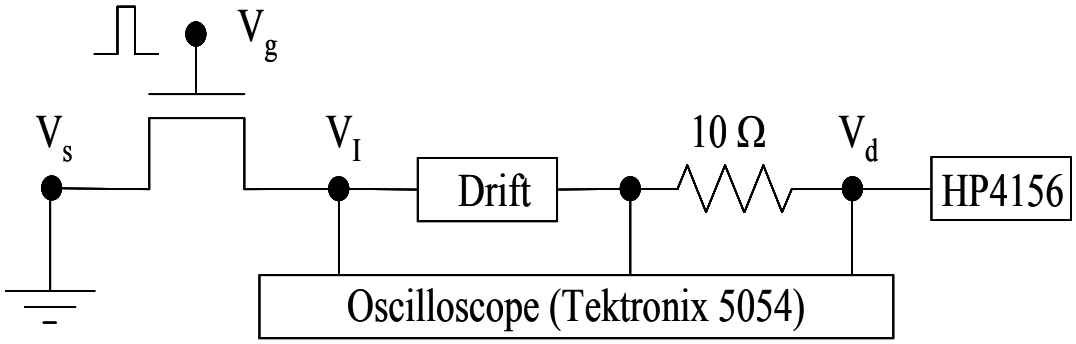

Fig. 3.2: Fast transient measurement setup for drain current and internal voltage (V_I) characterization. The external resistance (10Ω) is negligible compared to a total device resistance (~40V/10mA~4kΩ). A gate pulse and constant V_d are applied.

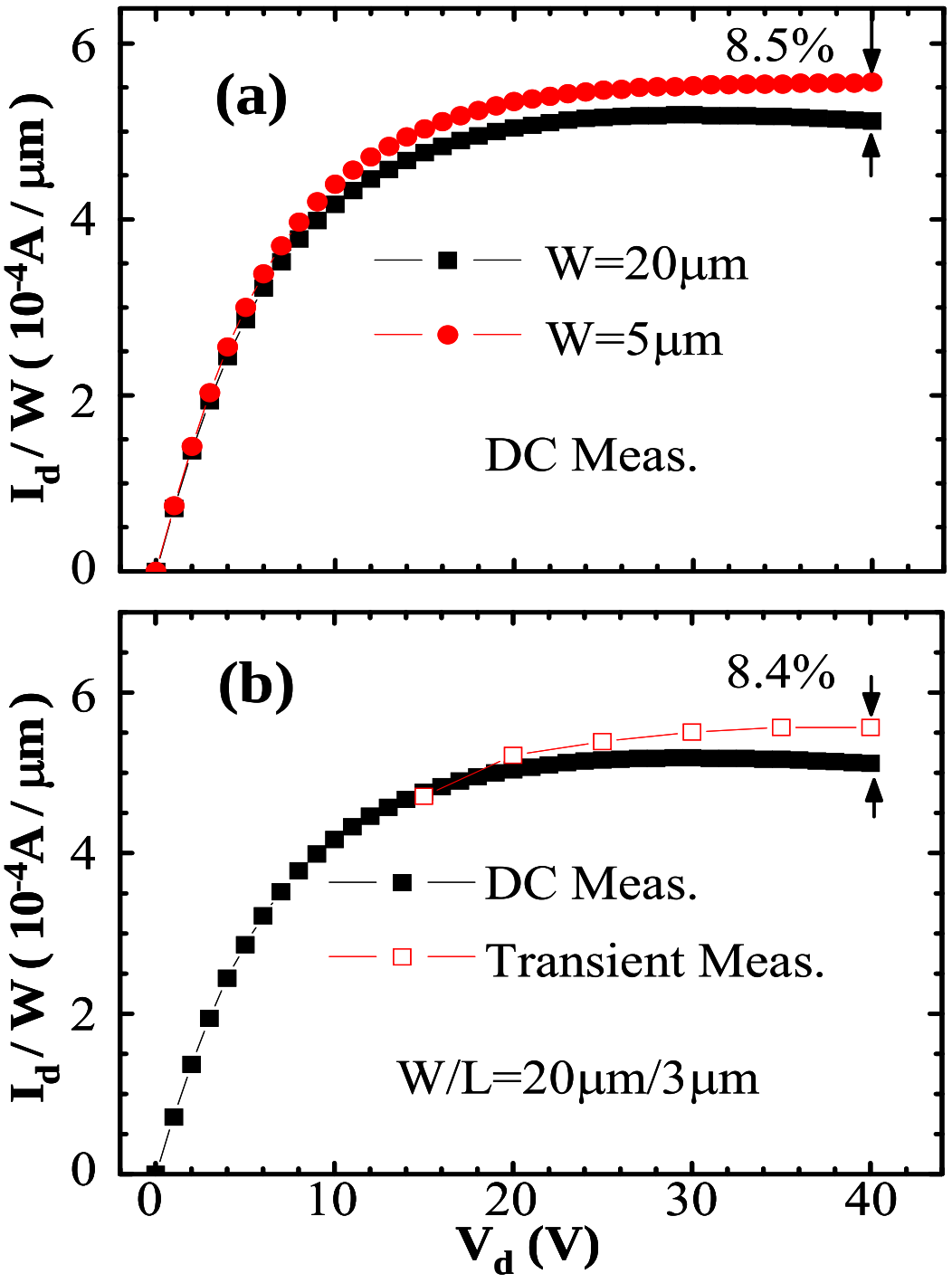

Fig. 3.3: (a) Normalized drain current (I_d/W) versus drain voltage in small and large gate width devices in DC measurement (Agilent 4156). (b) The I_d/W from a DC and a fast transient measurement for the large width device.

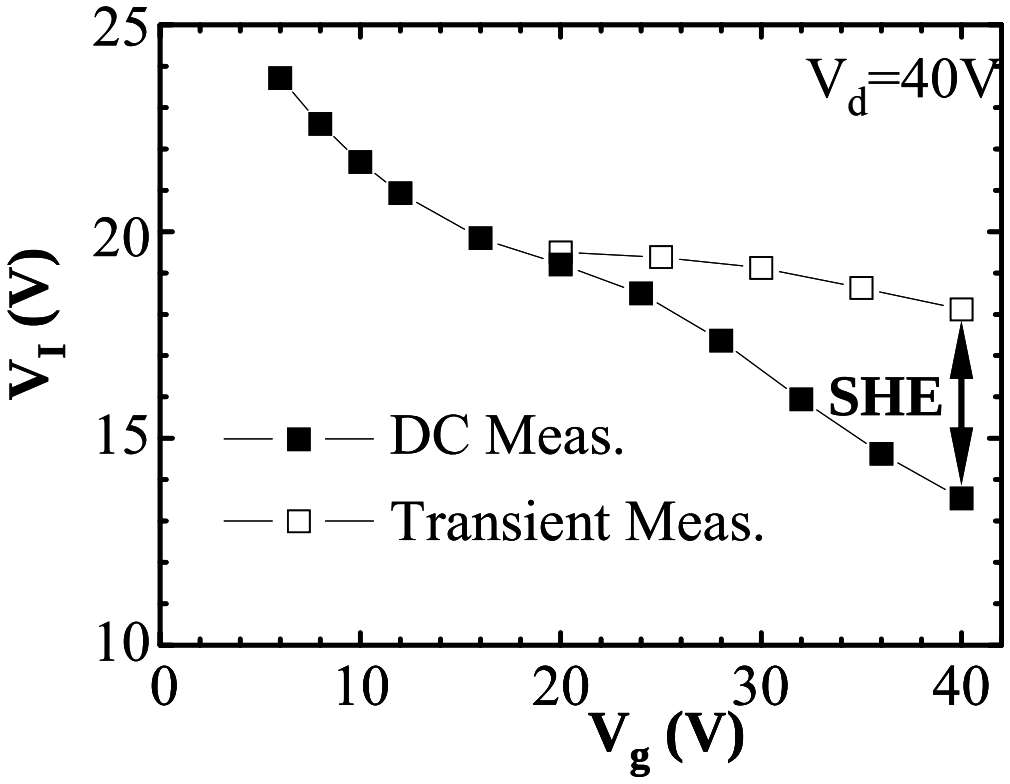

Fig. 3.4: Internal voltage versus gate voltage measured by Agilent 4156 and by a transient measurement setup.

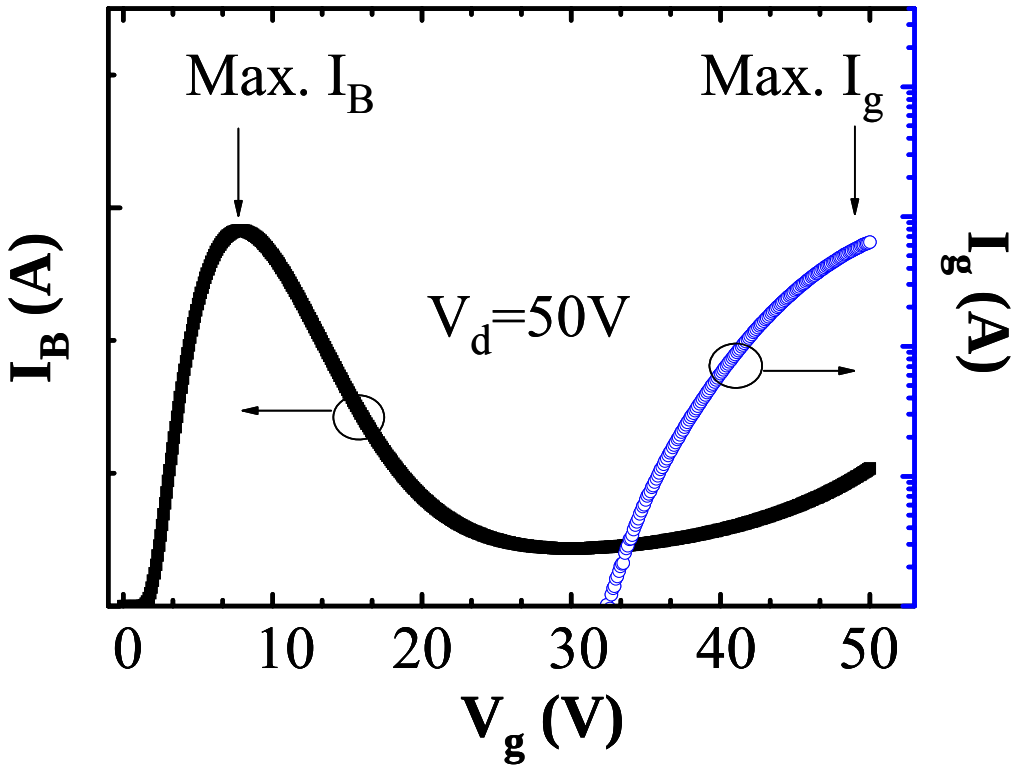

Fig. 3.5: Substrate current and gate current versus gate voltage in a LDMOS. Two hot carrier stress modes are shown, maximum I_B stress and maximum I_g stress.

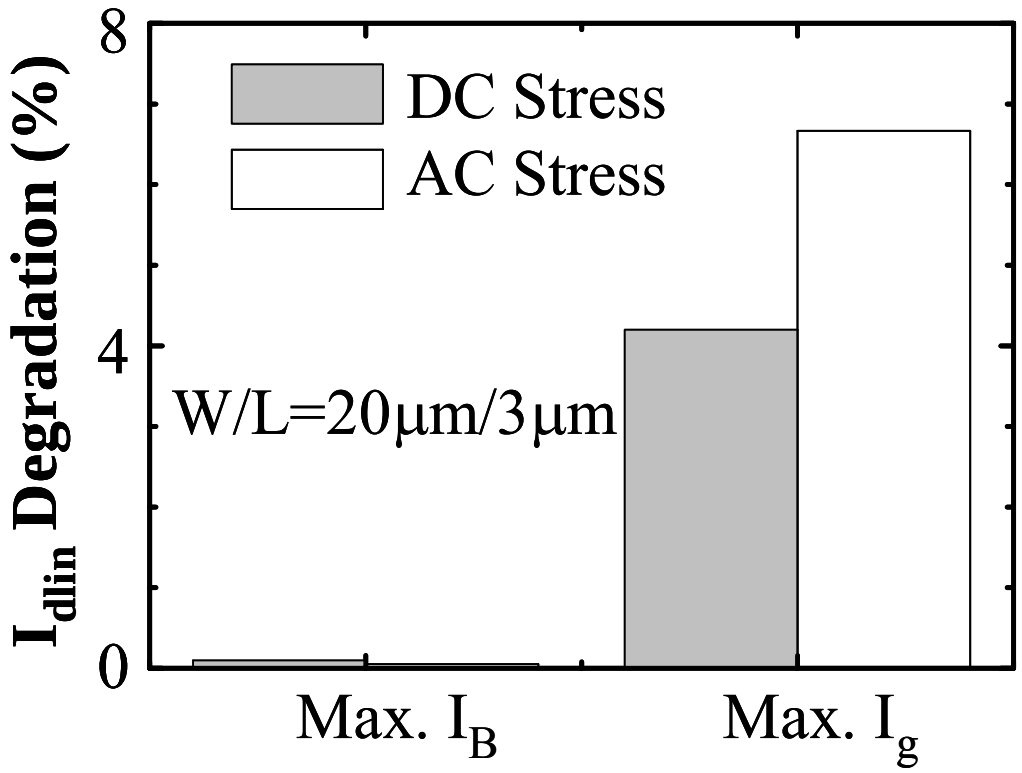

Fig. 3.6: Linear drain current degradation (V_g/V_d= 40V/0.1V) in two hot carrier stress modes. DC and AC stresses have the same cumulative stress time. AC stress has a frequency of 20kHz and a duty cycle of 10%.

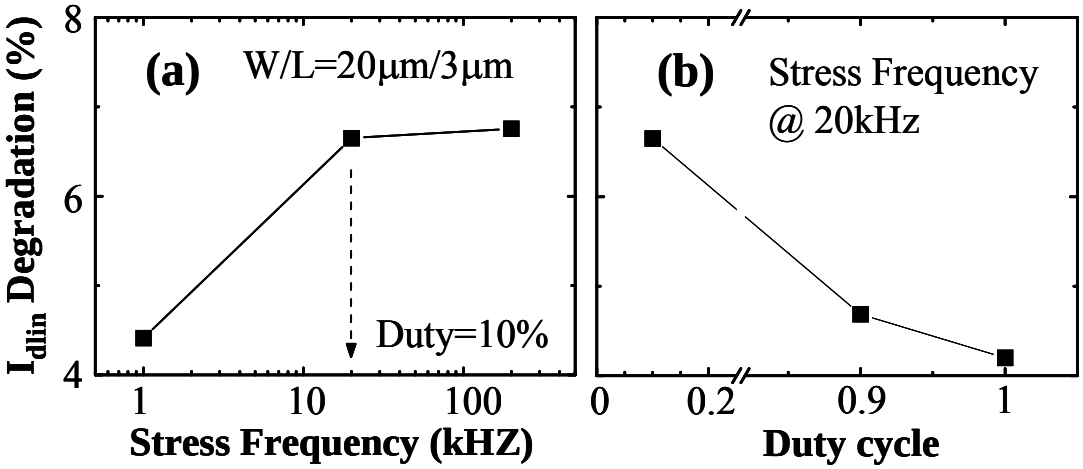

Fig. 3.7: (a) I_{dlin} degradation versus stress frequency with a duty cycle of 10%. A corner frequency (f_1) is around 20kHz. (b) I_{dlin} degradation versus duty cycle for a frequency of 20kHZ.

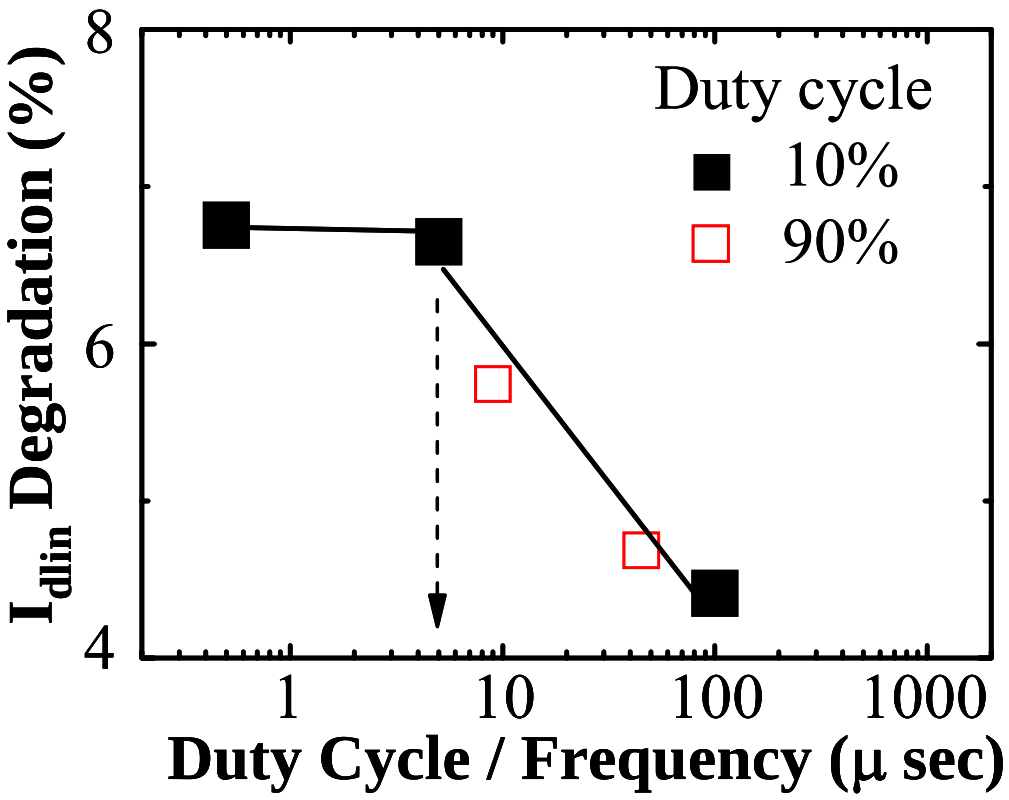

Fig. 3.8: I_{dlin} degradation versus pulse duration (=duty cycle/frequency) in AC stress. The corner time is around 5μs.

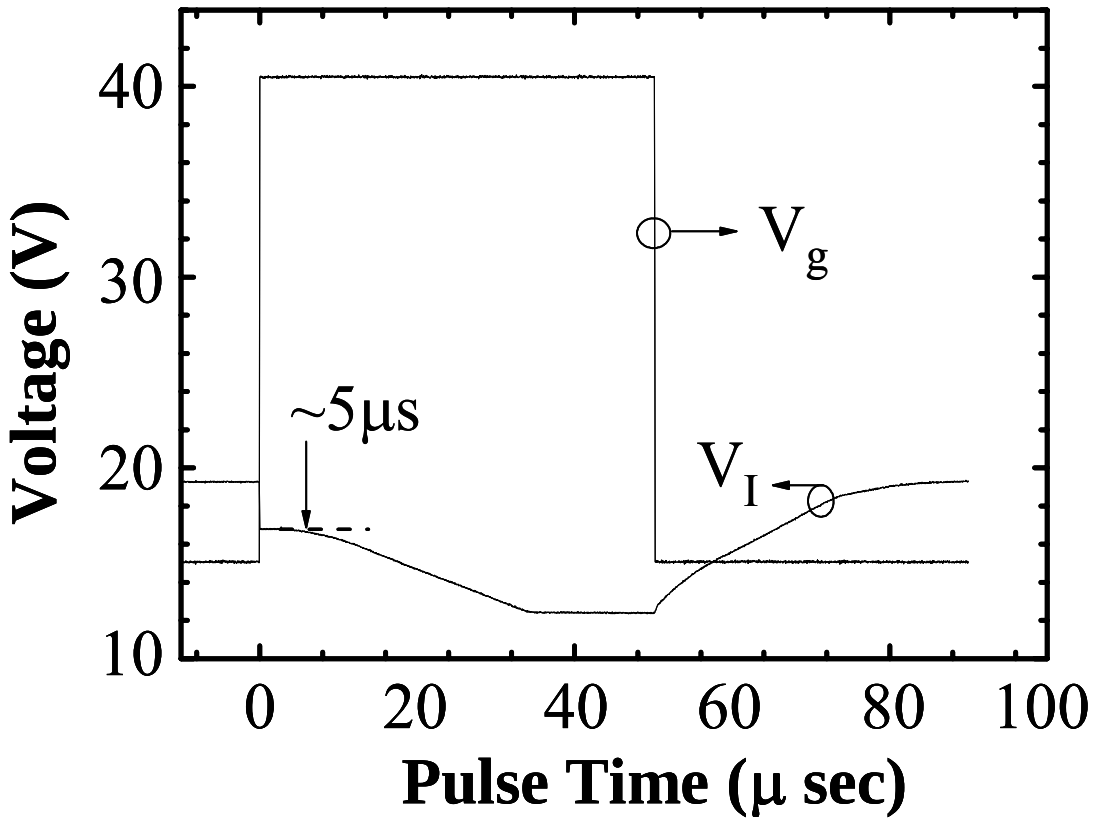

Fig. 3.9: The internal voltage (V_I) transient in a pulsed gate and DC drain voltage (V_d=40V) condition. The waveforms of V_I and V_g are plotted. The onset time for SHE is ~5μs.

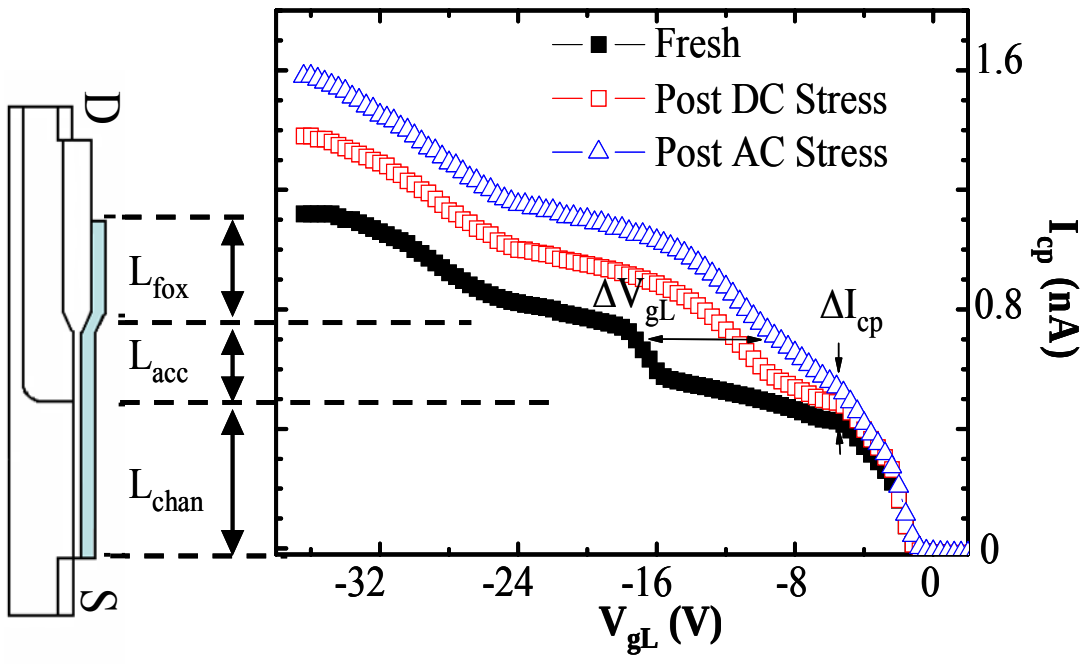

Fig. 3.10: Three-region charge pumping measurement results after maximum I_g AC and DC stress. A V_{gL} shift is in the accumulation region and a I_{cp} increase is in the channel region. For more details, see [45][46].

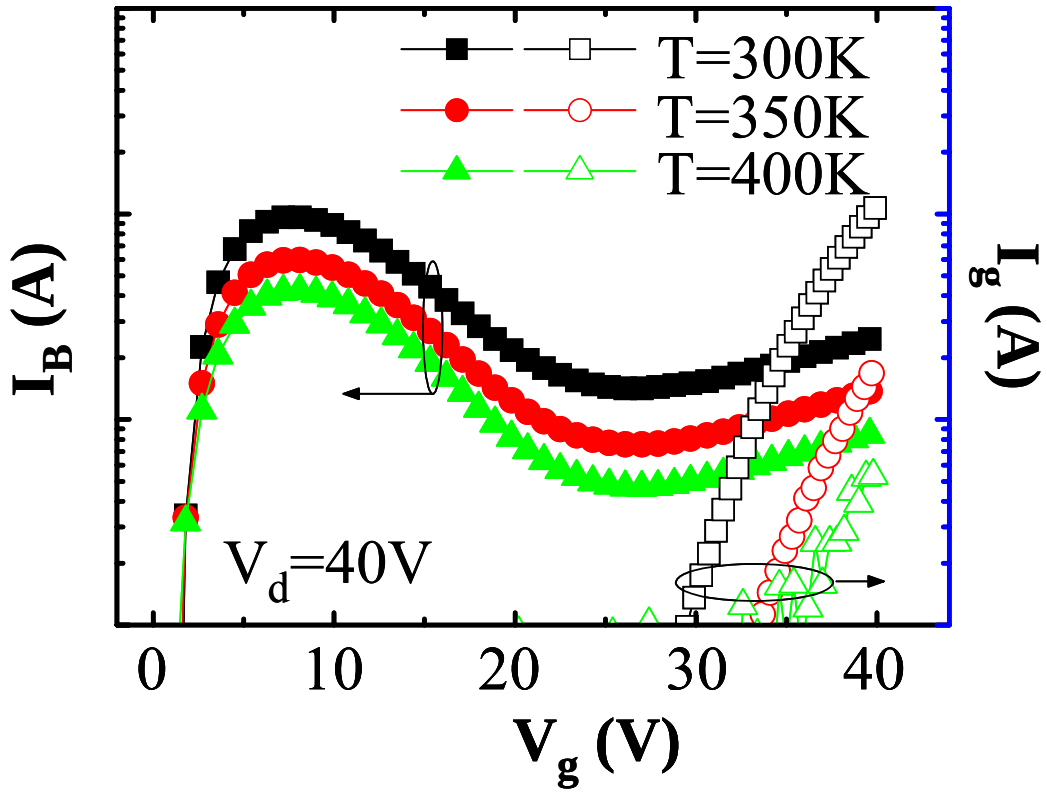

Fig. 3.11: Substrate current and gate current versus gate voltage for different temperatures.

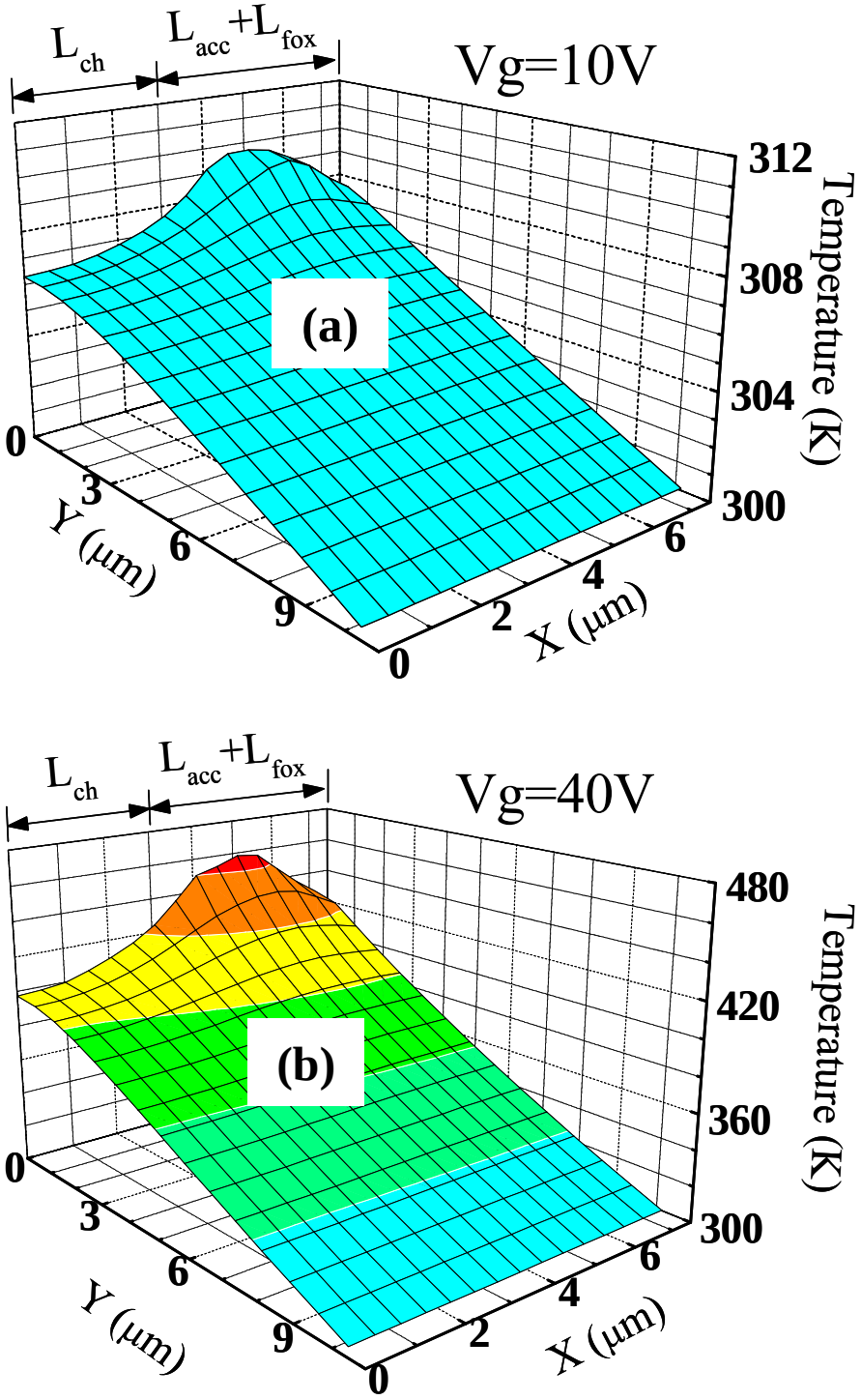

Fig. 3.12: Simulation of a temperature distribution with SHE. The ambient temperature is 300K. X and Y axes are indicated in Fig. 3.1. (a) V_g/V_d=10V/40V. (b) V_g/V_d=40V/40V.

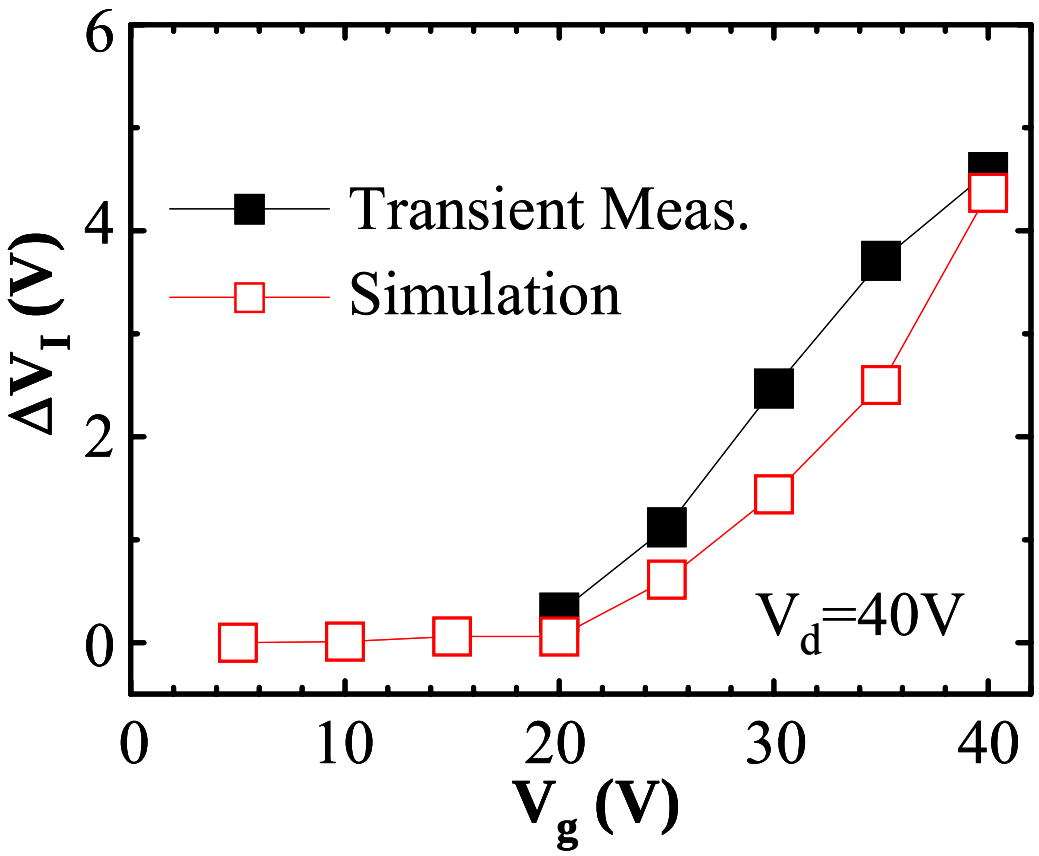

Fig. 3.13: Internal voltage change (V_I(non-SHE)-V_I(SHE)) versus gate voltage from measurement and from simulation.

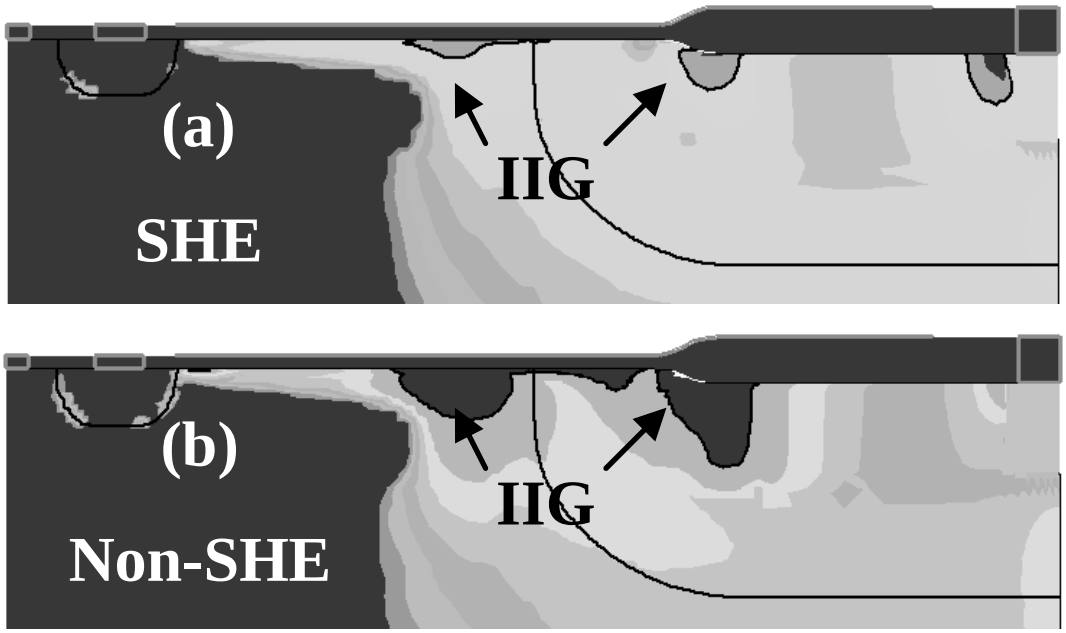

Fig. 3.14: Two-dimensional device simulation of impact ionization generation (IIG) rate at V_g/V_d=40V/40V. (a) SHE is included and (b) SHE is not included.

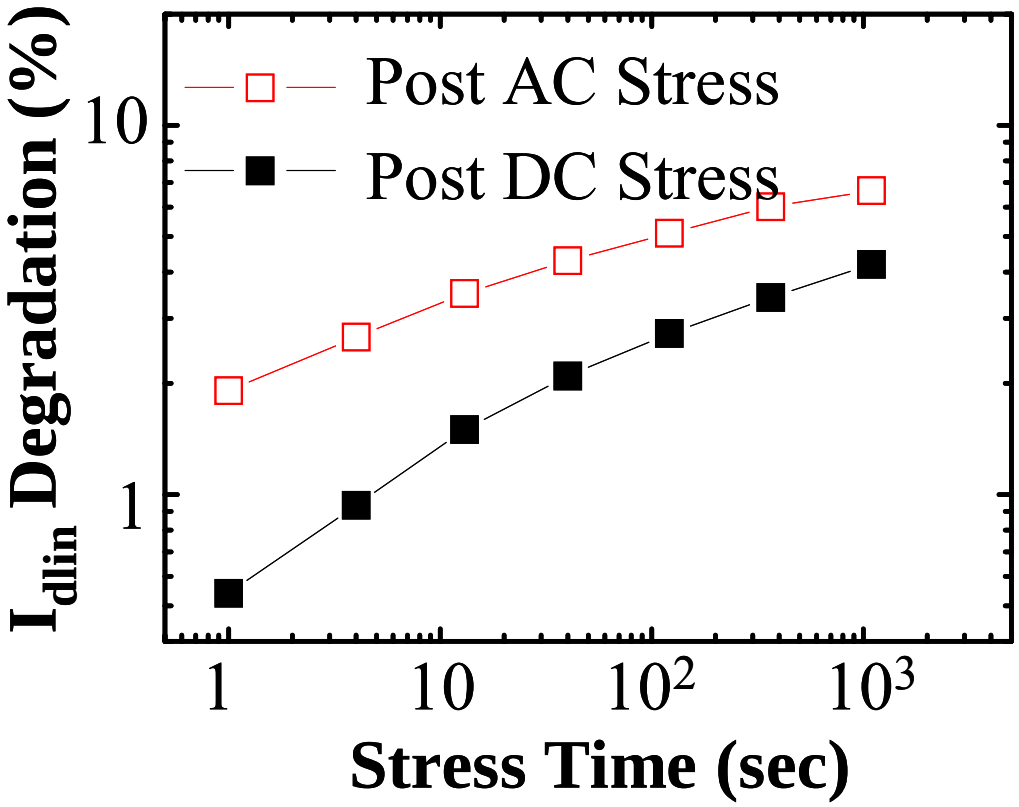

Fig. 3.15: I_{dlin} degradation rate after AC and DC stress in maximum I_g stress condition. The AC stress frequency is 20kHz and the duty cycle is 10%.

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附件四

國科會補助專題研究計畫項下出席國際學術會議心得報告

日期：99 年 07 月 27 日

計畫編號	NSC 96－2628－E－009－165－MY3		
計畫名稱	次 32 奈米 CMOS 元件可靠性分析，量子結構效應，與蒙地卡羅電荷傳輸模擬		
出國人員姓名	周佑亮	服務機構及職稱	國立交通大學 電機學院 電子研究所 博士班三年級
會議時間	2010 年 4 月 30 日至 2010 年 5 月 8 日	會議地點	美國 安納罕
會議名稱	(中文)國際可靠度物理會議 (英文) International Reliability Physics Symposium		
發表論文題目	(中文)利用隨機電報訊號探測快閃記憶體之寫入/抹除電荷橫向分佈 (英文)Use of Random Telegraph Signal as Internal Probe to Study Program/Erase Charge Lateral Spread in a SONOS Flash Memory		

一、參加會議經過

本會議舉行時間為 5 月 2 日到 5 月 6 日共五天，前兩天議程除了邀請各領域專家的演講還有第二天晚上的 workshop，第三天到第五天中午則是本次會議論文的口頭發表，第四天的晚上則是舉辦海報文章的討論會。

二、與會心得

本次會議拓展了我的國際視野，也了解到在各領域的專家他們的想法以及所研究的方向，此外，許多非英語系國家的專業人士都能夠輕鬆的應付各種不同腔調的

人，自覺除了英語口說能力要加強外，也要練就能夠理解非英語系國家的專業人士所說出來的英語。參予這次的會議受益良多，更知道自己需要在哪方面加強，期許自己能拓展研究的領域與深度。

三、考察參觀活動(無是項活動者略)

四、建議

五、攜回資料名稱及內容

會議論文光碟、演講投影片紙本

六、其他

Use of Random Telegraph Signal as Internal Probe to Study Program/Erase Charge Lateral Spread in a SONOS Flash Memory

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Abstract—A novel random telegraph signal (RTS) method is proposed to study the lateral spread of injected charges in program/erase of a NOR-type SONOS flash memory. The concept is to use RTS to extract an interface trap position and to detect a local potential variation near the trap due to injection of program/erase charges. By using this method, we find that CHISEL program has a broader charge distribution than CHE program. A mismatch of CHE program electrons and band-to-band erase holes is observed directly from this method.

I. INTRODUCTION

Two-bit/cell SONOS flash memory has been realized by storing bit charges in two sides of the channel by CHE program and band-to-band hot hole erase [1]. The control of program and erase charge lateral distributions of each bit is a major research thrust to improve cell endurance and scalability [2,3]. Attempts have been made in the past to characterize a trapped charge distribution in a SONOS cell. An inverse modeling approach is used to extract a program charge distribution from measured I-V characteristics [4]. Besides, a modified charge pumping (CP) technique [5] is employed to probe the lateral profile of programmed charges at the source and drain junctions separately. However, the inverse I-V modeling suffers from some limitations, for example, knowledge of precise device doping profile and lack of a unique solution. On the other side, the CP method is based on an assumption that interface traps have a uniform distribution along the channel [6], which is not correct in a buried diffusion bit-line SONOS cell. In addition, a charge pumping current is hardly sensed in a small area SONOS device.

In this work, we will use RTS arising from charge emission and capture at an oxide trap to investigate program/erase charge lateral spread. First, we determine the trap position from RTS without the need to know doping profile. Second, because RTS is very sensitive to a local potential change near the trap, we can use oxide traps as internal probes to detect a potential change due to program/erase charges. Finally, by using this technique, we find that CHISEL program has a broader charge distribution than CHE program and a mismatch of CHE program electrons and band-to-band erase holes is observed.

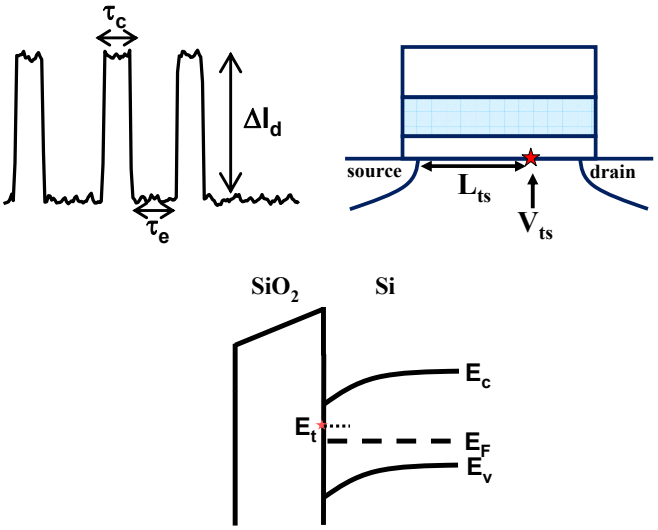

Fig. 1 Illustration of an interface trap induced RTS and the energy band diagram.

II. MEASUREMENT RESULT

Experiments were performed on SONOS flash cells with an ONO thickness of 8.5nm (top oxide), 7nm and 5.8nm, respectively. The cell size is W/L=0.11μm/0.1μm. The CHE program condition is V_{gs}=8V and V_{ds}=3.7V. The band-to-band hot hole (BTBH) erase is performed at V_{gs}= -4V and V_{ds}=5V.

A. Extraction of a Trap Position

An oxide trap position in the channel can be extracted in a way similar to the method in [7]. The RTS capture time τ_c, as illustrated in Fig. 1, can be expressed below,

$$<\tau_c>=1/n_e\sigma v_{th} \quad (1)$$

where σ is the trap cross-section and v_{th} is the thermal velocity. The channel electron concentration n_e is a function of gate overdrive, i.e.V_{gs}-V_{ts}, where V_{ts} is the channel potential at the trap position and is equal to $V_{ts}=(L_{ts}/L)V_{ds}$. L_{ts} is the distance of the trap from the source and L is the channel length, as shown in Fig. 1.

Two different V_{ds} (=0.05V and 0.3V) are used in RTS and capture time (τ_c) measurement. Note that the device is in the linear region at the measurement biases. Since the capture

time is dependent on an electron concentration near the trap, or in other words, a voltage drop between the gate (V_{gs}) and the channel right below the trap (V_{ts}), the amount of the lateral shift of these two curves (ΔV_{ts}) in Fig. 2 is equal to the difference of the voltages, raised by the two drain voltages, at the point (L_{ts}) of the trap. Therefore, the trap position in the channel can be extracted from $\Delta V_{ts}/\Delta V_{ds}=L_{ts}/L$. In this work, the RTS extraction is conducted in more than 30 un-cycled devices. For simplicity, we only record devices with two-level RTS (i.e., a single trap). The extracted trap position distribution is shown in Fig. 3. With this information, we can choose devices with appropriate trap positions as internal probes to investigate program/erase charge lateral spread.

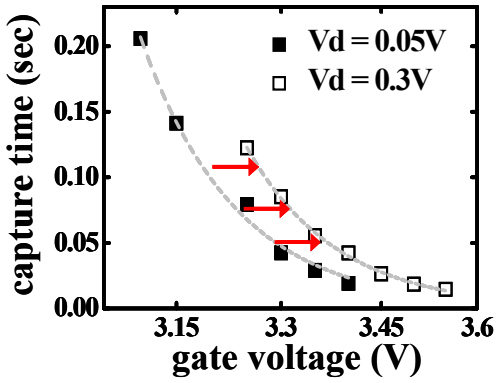

Fig. 2 The gate voltage dependence of average capture time in RTS at two drain voltages, V_{ds}=0.05V and 0.3V. The lateral shift of these two curves corresponds to ΔV_{ts}.

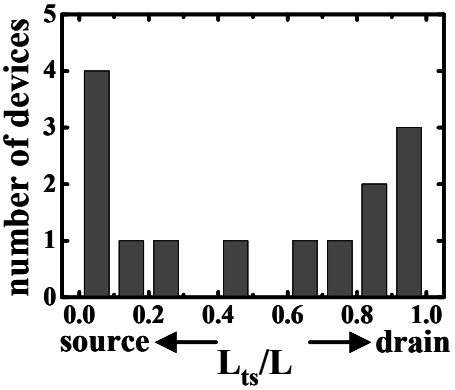

Fig. 3 Cumulative trap position distribution along the channel. L is the channel length and L_{ts} is the distance of a trap to the source.

B. Detection of a local potential change

The ratio of τ_c/τ_e is dependent on the local potential at the trap position, i.e.

$$<\tau_c>/<\tau_e>=g\exp[(E_t-E_F)/kT]\sim\exp(-q\Delta\varphi_s/kT) \quad (2)$$

where g is a pre-factor, E_t is the trap energy and $\Delta\varphi_s$ is a local potential change at the trap position.

C. CHE and CHISEL Programming

In order to detect a surface potential change near the drain during CHE program, a SONOS cell having a trap at x_t=0.2L from the drain edge is used. Fig. 4 shows the average emission time (τ_e) and capture time (τ_c) versus program ΔV_T [8,9]. Fig. 5(a) illustrates the band diagrams during CHE program. The trap energy level increases with respect to the Fermi level as program charge increases. The ratio of (τ_c/τ_e) and the corresponding surface potential change ($\Delta\varphi_s$) from Eq. (2) are plotted in Fig. 5(b). As more electrons are injected into the nitride layer, the conduction band at x_t and the trap level move upward away from the Fermi level. Thus, the τ_c/τ_e ratio becomes larger and larger.

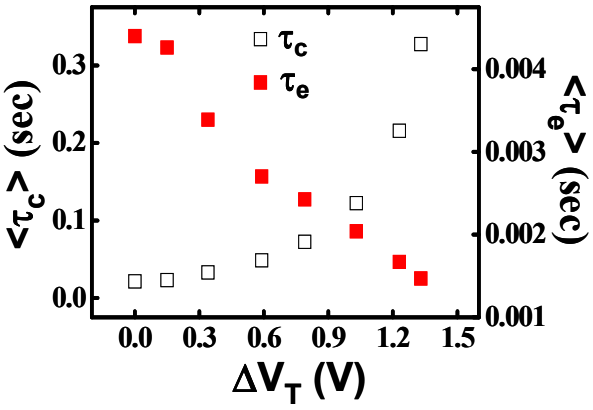

Fig. 4 Average capture time (τ_c) and emission time (τ_e) versus program ΔV_T.

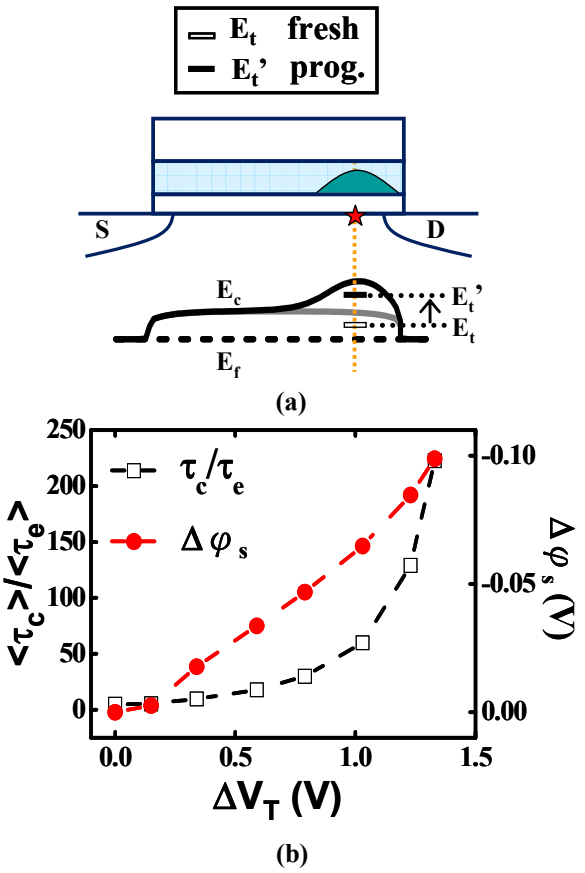

Fig. 5 (a)Band diagrams before and after CHE program. (b) $<\tau_c>/<\tau_e>$ and surface potential change versus program ΔV_T. The local potential change ($\Delta\varphi_s$) at the trap position is calculated from Eq. (2).

Fig. 6 compares the τ_c/τ_e in source side programming and drain side programming. The τ_c/τ_e remains unchanged during source-side programming, as expected, since program charges are near the source junction while the trap is near the drain edge. We also compare the program charge spread by CHE and CHISEL [10] in Fig. 7. The substrate bias is -2V in CHISEL operation. During CHISEL program, holes generated by channel electron impact ionization flow to the substrate and result in secondary impact ionization. The secondary electrons, accordingly, would be accelerated by the drain voltage and inject into the nitride layer. Fig. 7 shows that CHISEL has a broader injected charge distribution than CHE because the τ_c/τ_e and the potential change are larger at the same program ΔV_T.

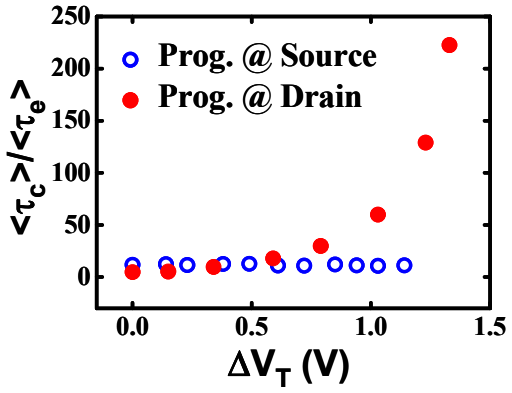

Fig. 6 Comparison of $<\tau_c>/<\tau_e>$ evolutions in source-side CHE program and in drain-side CHE program. Since the trap is near the drain, $<\tau_c>/<\tau_e>$ remains unchanged in source-side programming.

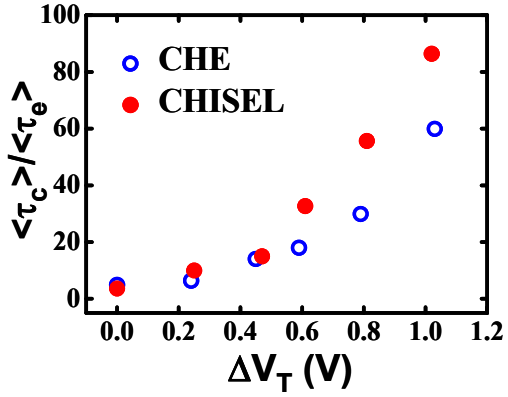

Fig. 7 Comparison of $<\tau_c>/<\tau_e>$ evolutions by CHE program and by CHISEL program. A substrate bias of -2V is applied in CHISEL injection.

D. BTBH Erase and Program/Erase Charge Mismatch

For comparison, we choose two devices with a respective trap position at 0.05L and 0.3L from the drain. CHE program and BTBH erase are performed. The τ_c/τ_e evolutions during program/erase are shown in Fig. 8 (in the x_t=0.05L cell) and in Fig. 9 (x_t=0.3L cell). The τ_c/τ_e increases as program V_T increases by CHE program and decreases by hot hole erase. For the point near the drain (i.e., x_t=0.05L), the τ_c/τ_e curves in program and in erase match very well, suggesting that program electrons at 0.05L are totally neutralized by erase holes. In contrast, at the point of x_t=0.3L from the drain, the τ_c/τ_e does not return to its original value after a P/E cycle. The larger τ_c/τ_e value during erase implies that program electrons (at 0.3L) are not completely compensated although the cell has been erased to its original V_T.

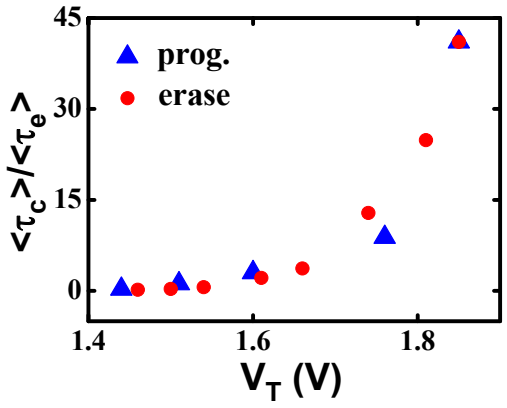

Fig. 8 The $<\tau_c>/<\tau_e>$ evolutions during CHE program and BTBH erase. The device has a trap at 0.05L from the drain. The $<\tau_c>/<\tau_e>$ has the same path in P/E.

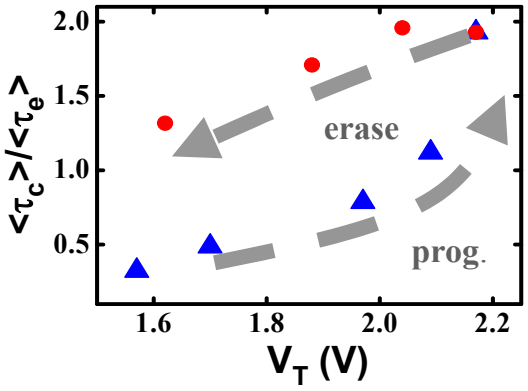

Fig. 9 The $<\tau_c>/<\tau_e>$ evolutions during CHE program and BTBH erase. The device has a trap at 0.3L from the drain. The erase path of $<\tau_c>/<\tau_e>$ is different from the program path.

Fig. 10 illustrates the program/erase charge distributions and the band diagrams after program and erase. The trap position is at x_t=0.05L from the drain in Fig. 10(a), and 0.3L from the drain in Fig. 10(b). In Fig. 10(a), the trap level increases with respect to the Fermi level due to program electron injection and decreases due to erase hole injection. In Fig. 10(b), the trap level increases due to program electrons, but is not affected by injected erase holes. The result in Fig. 9 implies that injected holes have a narrower distribution than program electrons.

III. CONCLUSION

We propose a novel RTS method to characterize program and erase charge lateral spread in a SONOS flash memory without the need to know a doping profile. Since the RTS method is very sensitive to a local potential change due to program/erase charges, it can provide a better resolution than a charge pumping method or an inverse I-V modeling approach. An evidence of a mismatch between program electrons and erase holes is shown by this method.

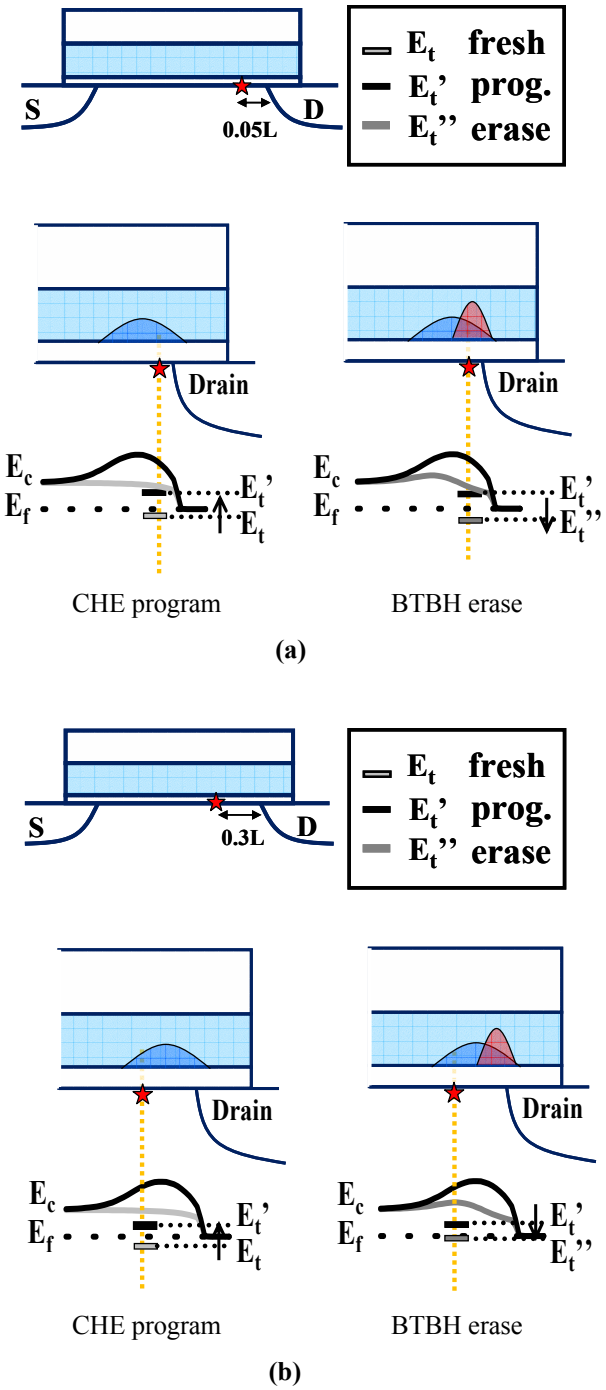

Fig. 10 Illustration of program/erase charge distributions and the band-diagrams after program and erase. The star represents interface trap position at (a) x_t=0.05L and (b) x_t=0.3L from the drain edge. The program electrons at x_t=0.05L are completely compensated, but some far electrons at x_t=0.3L are not compensated after erase.

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無研發成果推廣資料

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□未達成目標（請說明，以 100 字為限）

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近年來，國內在 CMOS 技術研發無論在製程整合、元件特性與量產技術方面，均具有明顯優勢，此可由國內工業界與學術界每年在 IEDM 論文發表數量，均名列前茅，可資證明。唯當 CMOS 元件微縮至 32 奈米以下時，為了增進元件性能與可靠度，在元件結構，材料與載子傳輸理論方面，均將發生重大改變。而國內長期在元件傳輸理論研究方面，相較於國外卻明顯不足。本計劃針對 32 奈米以下時，採用各種新式元件結構與材料所可能面臨之傳輸理論及可靠性議題，進行一為期多年之研究。為了配合此計劃之執行，吾結合國內工業界之優勢(例如元件製程技術)與吾人研究群之優勢(同時具有先進元件量測與蒙地卡羅模擬經驗)，對於先進元件發展方向及人才培育，具有重要價值。