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A Fully-Settled Linear Behavior Plus Noise Model for Evaluating the Digital Stimuli of the Design-for-Digital-Testability Σ-Δ Modulators

Hao-Chiao Hong

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Abstract Evaluating the digital stimuli used in the design-for-digital-testability (DfDT) Σ-Δ modulator is a time-consuming task due to its oversampling and nonlinear nature. Although behavioral simulations can substantially improve the simulation speed, conventional behavioral models fail to provide accurate enough signal-to-noise ratio (SNR) predictions for this particular application. In this paper, a fully-settled linear behavior plus noise (FSLB+N) model for the DfDT Σ-Δ modulator is presented to improve both the accuracy and the speed of the behavioral simulations. The model includes the following parameters: the finite open-loop gains, the offsets, the finite output swings, the flicker noise of the operational amplifiers (OPAMPs), as well as the thermal noises of the switched capacitors, the OPAMPs, and the reference supplies. With the proposed model, the behavioral simulation results demonstrate a high correlation with the measurement data. On average, the SNR difference between the simulation and the measurement is –1.1 dB with a maximum of 0.05 dB and a minimum of –2.2 dB. Comparing with the circuit-level simulation using HSPICE, the behavioral simulation with the FSLB+N model is 1,190,000 times faster. The proposed model not only can be used for evaluating the digital stimulus candidates, but also can be applied to system-level simulations of the mixed-signal design with an embedded DfDT Σ-Δ modulator.

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H.-C. Hong (✉)
Department of Electrical and Control Engineering,
National Chiao Tung University, Hsin-Chu, 300, Taiwan
e-mail: hchong@cn.nctu.edu.tw

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1 Introduction

It has become a major challenge to test a system-on-chip (SoC) chip as such an integrated system typically consists of several complex components such as a digital signal processor (DSP) core, random logic, memory, and analog/mixed-signal (AMS) circuits. Each component in an SoC may require different automatic test equipment (ATE) to satisfy its unique testing characteristics. Among them, testing the AMS part is not only costly but also cumbersome. Conventionally, the AMS and the digital parts of a mixed-signal chip are tested sequentially to avoid interference between the analog and the digital signal paths. However, the sequential flow results in a long test time. The expensive mixed-signal ATE, the low noise test environment requirement, and a long test time combined lead to a high test cost for the AMS circuits [1]. One example of such circuits is the Σ-Δ modulator, a popular analog-to-digital converter (ADC) architecture for high resolution applications. Testing such an ADC by traditional DSP-based functional tests requires a high-quality analog stimulus generator (ASG) and an ultra low noise testing environment.

To reduce the test cost and alleviate the debugging efforts on the test setup, unifying the testing interfaces completely in digital forms is an appealing approach. It benefits from reduced interference in the test environment, using less expensive digital ATE, and an easier test setup. Due to the elimination of analog signal paths

on the loadboard, simultaneously testing the AMS and digital parts becomes possible. As a result, the test time can be reduced.

There are a variety of schemes proposed for testing AMS circuits with digital stimuli in Toner and Roberts [14], Haurie and Roberts [2], Roy et al. [13], and Venuto et al. [15]. In Roy et al. [13] and Venuto et al. [15], four-step exponential staircase waveforms were generated and used as their analog stimuli by feeding a pulse-width-modulated digital stimulus to an R-C low-passed filter. Then, the specific test items of the ADC are analyzed by the polynomial-fitting test algorithm. It successfully measured the gain error and the offset of the ADC under test in addition to the second and the third harmonic distortions.

In Hong [3], a design-for-digital-testability (DfDT) second-order Σ-Δ modulator with pure digital interfaces in the test mode has been proposed. It is based on the Σ-Δ modulation based BIST scheme [4]. In the test mode, the digital stimulus D_{BSG} is generated by a bit-stream generator (BSG) which is a single-bit, digital Σ-Δ modulator. Then, the DfDT modulator accepts the repetitively applied digital bit-stream as its stimulus. Since it is a kind of functional test, all the specifications measured by conventional functional tests can be obtained by the digital stimuli as well. The measurement data show that the digital tests present a peak signal-to-noise ratio (SNR) up to 75.3 dB. In addition, the DfDT Σ-Δ modulator has the advantages of a low hardware overhead, a high fault coverage, a simple test setup, and the capability of performing at-speed tests [3].

The reconfigurable switched-capacitor input structure in Hong [3] can be applied to various Σ-Δ modulators as well. Simulations are necessary to choose the most suitable digital stimulus for the designated DfDT Σ-Δ modulator's architecture and the specified test item. Due to the over-sampling and nonlinear nature of the Σ-Δ modulator, conventional circuit level simulation tools such as HSPICE will take prohibitively long simulation hours to evaluate numerous digital stimulus candidates. Besides, there are other shortcomings in HSPICE simulations. For example, thermal noise and flicker noise are hard to be incorporated with the simulations. To address the issue of long simulation hours, one alternative is to use behavioral simulations for acceleration [3, 8–10]. However, behavioral simulations can underestimate the DfDT modulator's SNR performance in the test mode as shown in Hong [3]. A more accurate behavioral model is needed to improve the simulation accuracy.

In this paper, a fully-settled linear behavior plus noise (FSLB+N) model is proposed to enhance the simulation accuracy without compromising the fast simulation feature provided by behavioral modeling. The model consists of the parameters including the finite open-loop gains, the offsets, the finite output swings, the flicker noise of the operational amplifiers (OPAMPs), and the thermal noises of the switched capacitors, the OPAMPs, and the reference supplies. With this method, we show that the SNR results from our behavioral simulations are within 2.2 dB comparing with their corresponding measurement data.

The rest of the paper is organized as follows. Section 2 reviews the DfDT Σ-Δ modulator and explains why behavioral simulations are necessary for evaluating the digital stimuli. Section 3 introduces the FSLB+N model for the DfDT Σ-Δ modulator. Simulation results of various cases are discussed and analyzed in Section 4. Section 5 compares the measurement data with the simulation results to show the accuracy and speed of our proposed FSLB+N model. Finally, Section 6 concludes.

2 Overview of the DfDT Σ-Δ Modulator

2.1 Circuit Architecture of the Modulator Under Test

Figure 1 shows the schematic of a Σ-Δ modulation based DfDT second-order Σ-Δ modulator [3]. It will be used as the modulator under test (MUT) throughout this paper. The basic analog building blocks include two integrators and a comparator. The integrators are realized using the stray-insensitive switched-capacitor integrator shown in Fig. 2, except that four additional DfDT switches ($S1$ to $S4$) are added to the first integrator. The MUT has two operation modes: the normal mode and the test mode. By setting $T = 0$ and $D_{BSG} = 1$, the MUT operates in the normal mode. On the other hand, by setting $T = 1$ the MUT will operate in the test mode. In either mode, both integrators can still be represented by Fig. 2. The only difference is that the stimulus, $V_s(n)$, in the test mode is

$$V_s(n) = X_{BSG}(n) \times V_{REF}, \tag{1}$$

where

$$X_{BSG}(n) = 2D_{BSG}(n) - 1,\ D_{BSG}(n) \in \{1, 0\}. \tag{2}$$

Here, $X_{BSG}(n)$ is defined as the signed digital stimulus whose value is either 1 or –1.

Figure 3 depicts two possible test setups for the mixed-mode chips embedded with a DfDT modulator. The BSG can be implemented by software. A logic analyzer or PC-based ATE loads the generated digital stimulus and repetitively applies it to the MUT. The digital output of the MUT, D_o, then feeds back to the ATE for data analysis. Alternatively, the DfDT

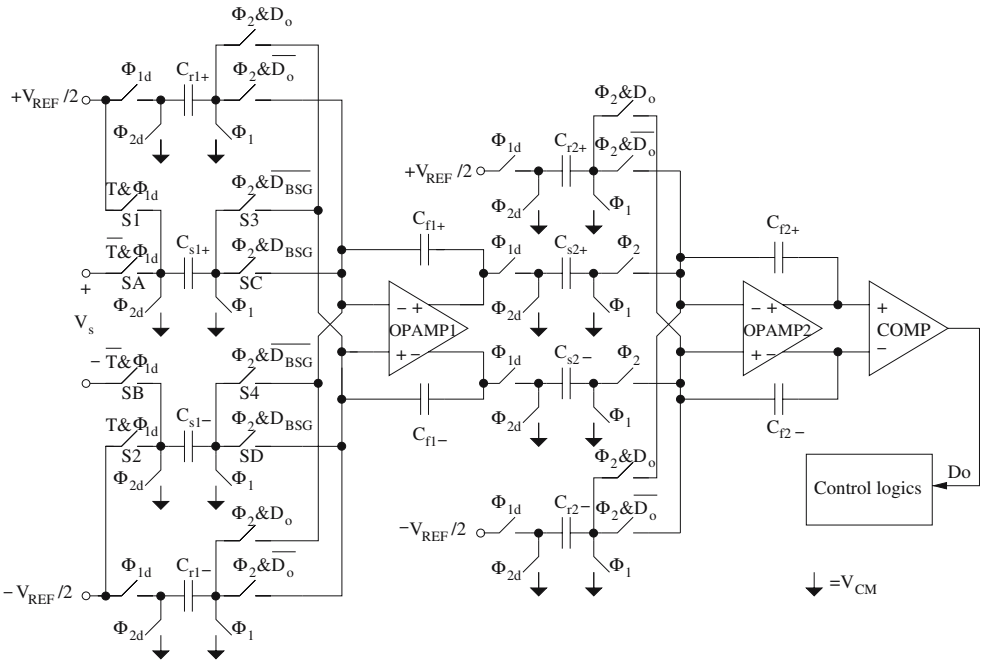

Fig. 1 Schematic of the Σ-Δ modulation based DfDT second-order Σ-Δ modulator [3]

modulator can be designed to be built-in-self-testable by adding an embedded BSG and an output response analyzer [5] to further simplify the test setup.

2.2 Analysis of the MUT

Figure 4 illustrates the generic block diagram of the MUT. Traditionally, the behavior of the integrator is modelled by a linear transfer function $S_i(z)/N_i(z), i \in \{1, 2\}$. Therefore, their behavioral models can be expressed by the difference equations of their input and output sequences [10, 11]. Ideally, $S_1(z) = S_2(z) = \frac{C_s}{C_f} z^{-1}$ and $N_1(z) = N_2(z) = 1 - z^{-1}$ for the example integrator. The actual transfer functions of the integrators depend on their circuit designs. On the other hand, the comparator can be easily described by if-then-else statements. Putting above equations together, the behavior of the Σ-Δ modulator can be simulated with a simple for-loop program.

An alternative way to estimate the performance of the Σ-Δ modulator is using an analytical method. Nonetheless, the Σ-Δ modulator is actually a nonlinear system owing to the comparator, even though all components were ideal. The non-linear nature makes an

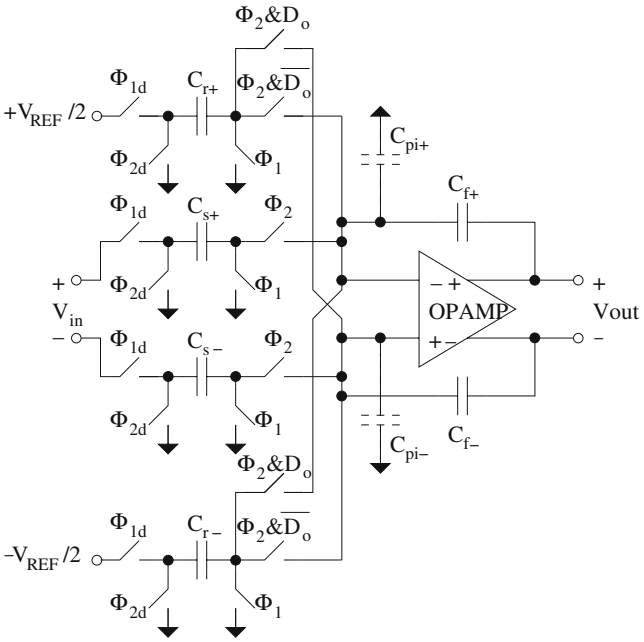

Fig. 2 The fully differential stray-insensitive switched-capacitor summing integrator

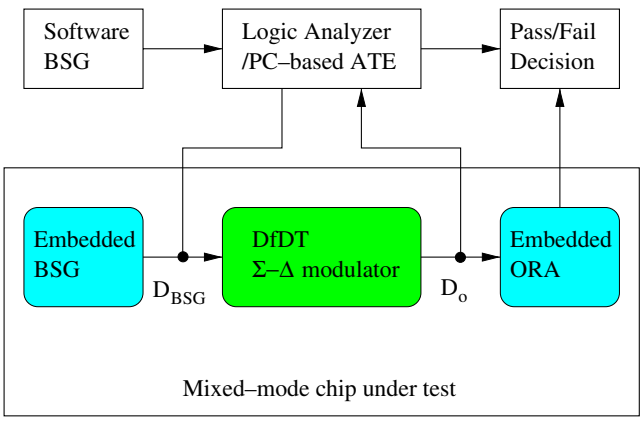

Fig. 3 Typical test setups for the DfDT Σ-Δ modulator

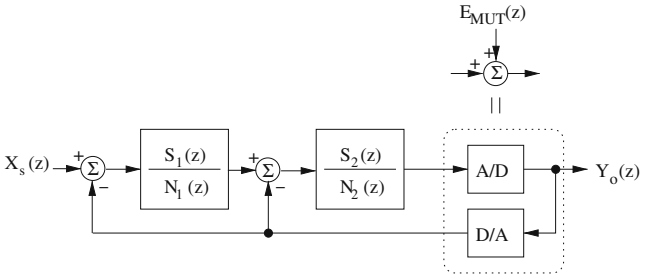

Fig. 4 The generic block diagram and pseudo-linear analytical model of the second-order MUT

accurate analysis of the Σ-Δ modulator very difficult. Yet the analytical results can still provide some preliminary information.

To simplify the analysis, the analytical model shown in Fig. 4 is widely accepted. The comparator (1-bit ADC) and the feedback 1-bit DAC are modelled by adding an additive and white quantization noise $E_{MUT}(z)$. According to the analytical model, the input/output (I/O) relationship of the second-order Σ-Δ modulator can be derived to be

$$Y_o(z) = STF_{MUT}(z)X_s(z) + NTF_{MUT}(z)E_{MUT}(z), \quad (3)$$

where

$$X_s(z) \equiv \frac{V_s(z)}{V_{REF}},$$

$$STF_{MUT}(z) = \frac{S_1(z)S_2(z)}{S_1(z)S_2(z) + N_1(z)S_2(z) + N_1(z)N_2(z)},$$

$$NTF_{MUT}(z) = \frac{N_1(z)N_2(z)}{S_1(z)S_2(z) + N_1(z)S_2(z) + N_1(z)N_2(z)}, \quad (4)$$

and

$$Y_o(z) \equiv 2D_o(z) - 1. \quad (5)$$

$X_s(z)$, $E_{MUT}(z)$, and $Y_o(z)$ represent the normalized test stimulus, the normalized quantization noise, and the signed digital output of the MUT, respectively. $Y_o(n)$ has a value of either 1 or –1.

Equation 3 indicates that $V_s(z)$ is filtered by the signal transfer function (STF), $STF_{MUT}(z)$, and $E_{MUT}(z)$ is shaped by the noise transfer function (NTF), $NTF_{MUT}(z)$, to appear at the digital output of the Σ-Δ modulator. Since $STF_{MUT}(z)$ has a low-pass and $NTF_{MUT}(z)$ has a high-pass characteristic, the in-band $V_s(z)$ will be passed to the output while the in-band $E_{MUT}(z)$ is attenuated by $NTF_{MUT}(z)$. As a result, the remaining shaped quantization noise in the passband determines the SNR performance of the MUT.

Equation 3 is also a generic formula of a general single-bit Σ-Δ modulator's I/O relationship [10]. Since the signed digital stimulus $X_{BSG}(z)$ comes from a single-bit, digital Σ-Δ modulator, it can be expressed by

$$X_{BSG}(z) = STF_{BSG}(z)X_s(z) + NTF_{BSG}(z)E_{BSG}(z). \quad (6)$$

$STF_{BSG}(z)$, $NTF_{BSG}(z)$, and $E_{BSG}(z)$ represent the STF, the NTF, and the normalized quantization noise of the BSG respectively.

Recall that the stimulus $V_s(z)$ is equal to $X_{BSG}(z) \times V_{REF}$ in the test mode. Substituting (6) into (3), the I/O relationship of the MUT in the test mode will be

$$Y_o(z) = STF_{MUT}(z)STF_{BSG}(z)X_s(z) + STF_{MUT}(z)NTF_{BSG}(z)E_{BSG}(z) + NTF_{MUT}(z)E_{MUT}(z). \quad (7)$$

Equation 7 indicates that there are two shaped quantization noise sources in the output of the test mode enabled MUT. One comes from the BSG, the other is generated by the MUT itself. If the two shaped noises were uncorrelated and a suitable BSG is chosen such that

$$|STF_{MUT}(z)NTF_{BSG}(z)E_{BSG}(z)| \ll |NTF_{MUT}(z)E_{MUT}(z)| \quad (8)$$

in the passband, then Eq. 7 could be approximated by

$$Y_o(z) = STF_{MUT}(z)STF_{BSG}(z)X_s(z) + NTF_{MUT}(z)E_{MUT}(z) \quad (9)$$

in the passband. Equation 9 is similar to Eq. 3, thus both modes should have similar measurement results. An intuitive approach to satisfy Eq. 8 is to select a BSG whose order is higher than that of the MUT. A question raises here: Are $STF_{MUT}(z)NTF_{BSG}(z)E_{BSG}(z)$ and $NTF_{MUT}(z)E_{MUT}(z)$ actually uncorrelated when an arbitrary BSG is applied? The shaped noise correlation mechanism is very complicated. It depends not only on the stimulus and the structure of the MUT, but also on the circuits of the MUT. Only the measurement data or the simulation results with a suitable model can provide the answer.

3 Fully-Settled Linear Behavioral Plus Noise Model

Circuit designers usually rely on circuit-level simulators to obtain accurate simulation results. Unfortunately, it can take a long time before the simulations are

completed. The simulation time will get even worse for the over-sampling Σ-Δ converters since a large number of output samples have to be collected in order to analyze their performance. A general solution is to conduct simulations with a simplified behavioral model [8–10]. With such models, the simulation results could be acceptably accurate while the simulation time is greatly reduced.

Such a behavioral model for switched-capacitor Σ-Δ modulators has been proposed in Malcovati [9]. The finite gain, the slew-rate, the unit-gain bandwidth, and a limited output swing of the OPAMP in the first stage are included in the simulations in addition to the KT/C noise of the switched-capacitors of the same stage and the sampling jitter. This model has been shown to be effective in making accurate predictions for the SNR performance of the Σ-Δ modulators; however, it is not appropriate for evaluating the digital stimulus as will be discussed later.

Because the goal of the behavioral simulations is to evaluate the test stimuli rather than the circuits, non-linear behavioral factors such as the finite slew-rates and the finite unit-gain bandwidths of the OPAMPs are excluded to make the behavioral model as simple as possible. In other words, the output responses of the integrators are assumed to be fully-settled in every clock cycle. With this assumption, the behavior of the integrator can be expressed by a simple linear difference equation to reduce the simulation time. On the other hand, the comparator is also assumed to be ideal and noise free. The reason is that any error and noise induced by the comparator will be effectively attenuated by $NTF_{MUT}(z)$ [6, 10]. Consequently, the errors and noise caused by the comparator can be ignored.

3.1 Stray-Insensitive Integrator

Practical transfer function of an integrator depends on its circuit design. To simplify the behavioral model thus speeding up the simulations, only the signal independent circuit impairments are considered.

3.1.1 Operational Amplifier

Four basic static characteristics of the OPAMP are included in the model: the finite open-loop gain A, the offset voltage V_{OS}, the parasitic input capacitance C_{pi}, and a limited output swing. They are all assumed to be constants. Practical integrators always have some offsets. The offset may come from the mismatched devices in the OPAMP and the mismatched differential capacitors. Clock feed-through and charge injection mechanisms of unbalanced switches can induce some offsets as well. To simplify the model, V_{OS} is used to lump all the offset factors together.

According to the charge conservation principle, the difference equation of the stray-insensitive integrator in the presence of these linear impairments of the OPAMP can be derived as

$$\begin{aligned} V_{out}(n) = & \frac{C_f + \frac{C_f + C_{pi}}{A}}{C_f + \frac{C_f + C_r + C_s + C_{pi}}{A}} V_{out}(n-1) \\ & + \frac{C_s}{C_f + \frac{C_f + C_r + C_s + C_{pi}}{A}} V_{in}(n-1) \\ & - \frac{C_r}{C_f + \frac{C_f + C_r + C_s + C_{pi}}{A}} V_{REF} Y_o(n-1) \\ & + \frac{C_r + C_s}{C_f + \frac{C_f + C_r + C_s + C_{pi}}{A}} (V_{OS} - V_{CM}), \end{aligned} \tag{10}$$

where $V_{CM} = 0$. Since Eq. 10 is a singled-ended behavioral description, each of the capacitance in Eq. 10 is the result of the respective differential capacitors in series, i.e., $C_S = C_{S+}/2 = C_{S-}/2$ and so forth. The capacitive values will affect the calculation of the thermal noise power later. Additional if-then-else statements are used to clip the output signals of the integrator once they exceed the output swing limits. It has been shown that a small output swing may lead to considerable SNR degradation when the stimulus amplitude is close to the full-scale [9].

The behavioral model described above only simulates the quantization noise. The output of a practical Σ-Δ modulator, however, contains shaped quantization noise, thermal noise, as well as flicker noise. Due to the high SNR performance of the Σ-Δ modulator, these noises can not be ignored.

3.1.2 Thermal Noise

Each switched capacitor, the OPAMPs, and the reference supplies induces some thermal noise. A uniformly distributed random sequence is suitable for representing this type of noise. Let $R_i(n), i \in \{1, \cdots, 7\}$ be uniformly distributed random sequences with an output range in-between -1 to 1. In theory, such a sequence has a power of one third. Consequently, a thermal noise source whose power is P_N can be represented by a noise sequence $\sqrt{3P_N}R_i(n)$.

The noise sequences are added to the model according to the circuit operations. For instance, a switched-capacitor induces a total thermal noise power of KT/C to its sampled data where C represents the sampling capacitance [12]. During the period when Φ_1 is active, C_s and C_r sample V_{in} and $V_{REF}Y_o(n)$ respectively. Hence,

two noise sequences, $\sqrt{\frac{3KT}{C_s}}R_1(n)$ and $\sqrt{\frac{3KT}{C_r}}R_2(n)$, are added to the respective signals. When Φ_2 is active, C_s and C_r will sample V_{CM} in parallel. The noise sequence, $\sqrt{\frac{3KT}{C_s+C_r}}R_3(n)$, is added accordingly. The transfer coefficient of each noise sequence is the same as that of the corresponding sampled signal.

The thermal noise of the reference supplies is included by replacing their fixed values in Eq. 10 with the following noise sequences

$$V_{cm}(n) = \sqrt{3P_{TNVCM}}R_4(n) \tag{11}$$

and

$$V_{ref}(n) = \sqrt{3P_{TNVREF}}R_5(n) + V_{REF}. \tag{12}$$

Finally, the noise sequence

$$V_{nop}(n) = V_{OS} + \sqrt{3P_{TNOP}}R_6(n) \tag{13}$$

takes over the role of V_{OS} in Eq. 10 because both P_{TNOP} and V_{OS} of the OPAMP are input-referred results. In the above equations, P_{TNOP} represents the input-referred thermal noise power of the OPAMP, while P_{TNVCM} and P_{TNVREF} denote the thermal noise powers of the reference supplies V_{CM} and V_{REF} respectively. These noise powers can be estimated by proper simulations such as the ac noise analysis of HSPICE.

The resulting difference equation of the integrator incorporated with the thermal noises is formulated by

$$\begin{aligned} V_{out}(n) = {} & \frac{C_f + \frac{C_f+C_{pi}}{A}}{C_f + \frac{C_f+C_r+C_s+C_{pi}}{A}} V_{out}(n-1) \\ & + \frac{C_s\left[V_{in}(n-1) + \sqrt{\frac{3KT}{C_s}}R_1(n-1)\right]}{C_f + \frac{C_f+C_r+C_s+C_{pi}}{A}} \\ & - \frac{C_r\left[V_{ref}(n-1)Y_o(n-1) + \sqrt{\frac{3KT}{C_r}}R_2(n-1)\right]}{C_f + \frac{C_f+C_r+C_s+C_{pi}}{A}} \\ & + \frac{[C_r+C_s]\left[\sqrt{\frac{3KT}{C_s+C_r}}R_3(n) + V_{cm}(n)\right]}{C_f + \frac{C_f+C_r+C_s+C_{pi}}{A}} \\ & + \frac{C_r+C_s}{C_f + \frac{C_f+C_r+C_s+C_{pi}}{A}} V_{nop}(n). \end{aligned} \tag{14}$$

It is important to note that since each switched capacitor is switched independently, the random sequences should be independently generated.

A question is that is it necessary to take all thermal noise sources into account? For a normal Σ-Δ modulator, the thermal noise of the first stage will dominate due to the modulator's noise shaping property [10]. That is why the model in Malcovati [9] only takes the KT/C of the first stage into account while still providing satisfactory predictions.

For the DfDT modulator operating in the test mode, the scenario is different. In fact, the thermal noise leads to two contradictory effects on the MUT operating in the test mode. First, it increases the in-band noise power, which is not desirable. On the other hand, it is also a nature source that dithers the internal signals of the MUT. Note that dithering is beneficial for the test mode enabled MUT as it effectively reduces the correlation between signals [10]. Such a technique is widely applied to enhance the performance of Σ-Δ modulators [10]. Because the shaped noise correlation is a major concern in the test mode, excluding any noise source may lead to incorrect results of the shaped noise correlation and reduce the SNR prediction accuracy. Consequently, we suggest to include all thermal noise sources in the simulations.

3.1.3 Flicker Noise

In addition to thermal noise, the OPAMPs also induce flicker noise whose power spectral magnitude is inversely proportional to the frequency. The flicker noise plays the same role as that of the thermal noise and thereby is necessary to be included in the model.

Circuit-level simulators such as HSPICE usually do not provide any embedded command to involve the flicker noise in transient analysis simulations. However, a time-domain flicker noise representation is compulsory for the simulation.

Here, the flicker noise is generated by filtering a uniformly distributed random sequence, $R_7(n)$, through the digital integrator whose transfer function is $\frac{1}{1-z^{-1}}$. A constant, K_f, is used to scale the computed sequence such that the sequence has a similar power to that obtained from the ac input-referred flicker noise analysis. Finally, it is added to the model by modifying Eq. 13 to be

$$\begin{aligned} V_{nop}(n) = {} & V_{OS} + \sqrt{3P_{TNOP}}R_6(n) \\ & + K_f \sum_{m=1}^{m=n} R_7(m). \end{aligned} \tag{15}$$

4 Simulation Results

A large number of behavioral simulations are conducted to check the significance of every parameter in the FSLB+N model. The design and test setup parameters in Hong [3] were used for the experiments. V_{REF} is set to 0.9 V and the output swing of the OPAMPs are

set to ±2.8 V. The stimulus amplitude and frequency are set to –6 dBFS and 21/128K times the sampling frequency respectively unless otherwise noticed. The oversampling ratio (OSR) is set to 128 and the output samples taken for the spectral analysis are 128K points.

Five different types of stimuli are simulated including the analog one in the normal mode and four digital ones in the test mode. The digital stimuli are generated by the second-, the third-, the fourth-, and the fifth-order BSGs adopted from Kuo et al. [7].

Similar to the practical measurement results, the random nature of the added noises will vary the simulation results of the same test from time to time. To alleviate the randomness, each simulated SNR result is an average of the eight simulation results.

4.1 Ideal Case

Figure 5 depicts the relationship between SNR and stimulus amplitude with ideal OPAMPs and an ideal comparator. Additionally, no noise is applied. The results show that the analog stimuli present lower SNR results than their digital counterparts. The higher order the BSG is, the higher SNR the MUT has. Obviously, these results are incorrect. In fact, the output bitstreams of the test mode enabled MUT are identical to its input ones separated by a two-clock delay. In other words, the ideal MUT does not generate any quantization noise ($E_{MUT}(z) = 0$) in the test mode.

Figure 5 also reveals the possible limitation of using high-order BSGs. The fourth- and fifth-order BSGs are not suitable for the test in which the stimulus amplitude is higher than −5 dBFS. Such a high stimulus amplitude will overload the MUT and/or the BSGs and severely deteriorate the test results.

4.2 Finite OPAMP Gain

Figure 6 shows how finite OPAMP gains affect the SNR results. The simulation results contradict with those of the ideal case. The analog stimuli now present higher SNR results than their digital counterparts. The finite OPAMP gains dramatically degrade the tested SNR results of the digital stimuli even if the gains are as high as 120 dB. It is because the finite OPAMP gains make the transfer functions of the integrators no longer having a pole at dc. Thus the integrators leak some of their input signals to the output. The smaller the OPAMP gain is, the more the leakage will be. The leaked signals excite the MUT and result in nonzero $E_{MUT}(z)$.

Recall that $E_{BSG}(z)$ is a part of the digital stimulus. The finite OPAMP gains leak it through the two integrators to the comparator where $E_{MUT}(z)$ is generated. Consequently, $E_{MUT}(z)$ has a strong correlation to $E_{BSG}(z)$. The correlation makes the approximation of Eq. 9 invalid and the in-band quantization noise power increases.

Figure 7 shows the simulated SNR vs. the stimulus amplitude in which only the 75 dB OPAMP gains are considered. In general, the digital stimuli generate poor SNR results than their analog counterparts. Their differences can be more than 16 dB. The only exception is the scenario when the stimulus amplitude is −60 dBFS.

To provide more insights with respect to the shaped noise correlation, Fig. 8 illustrates the simulated output spectrum of the MUT with the −40 dBFS, third-order modulated digital stimulus. There are many spurs that deteriorate the tested result. Similar spurs can be found in the output spectrum of a single-bit first-order Σ-Δ modulator that also suffers from

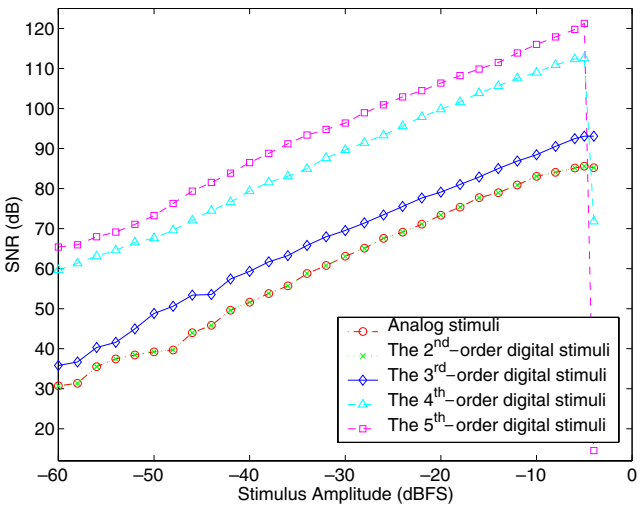

Fig. 5 SNR vs. stimulus amplitude with ideal circuits

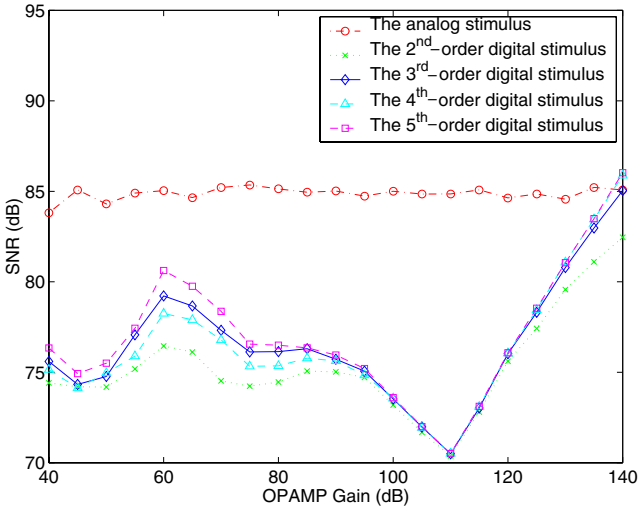

Fig. 6 SNR vs. OPAMP gain

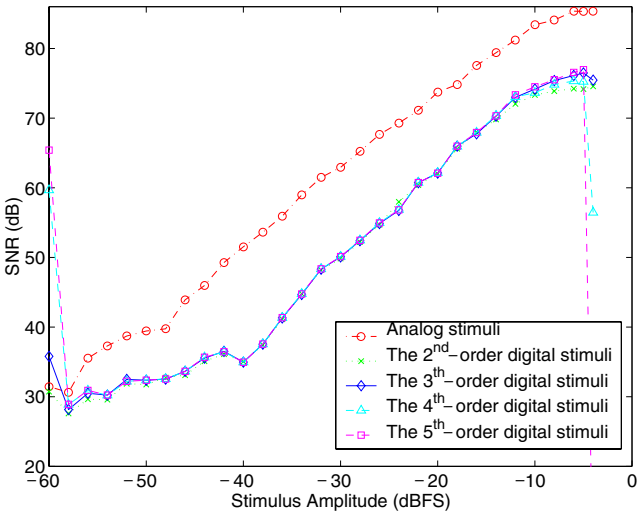

Fig. 7 SNR vs. stimulus amplitude with OPAMP gains of 75 dB

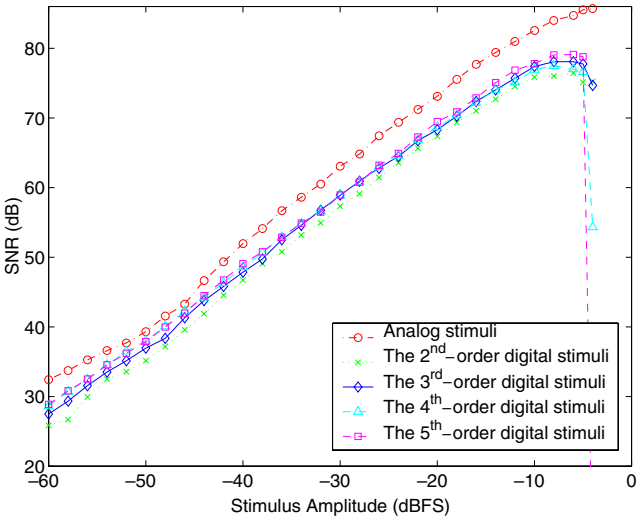

Fig. 9 Stimulated SNR vs. stimulus amplitude. The OPAMPs have the same 75 dB gain and 410 μV offset voltage

the correlation between its input and the quantization noise [4].

4.3 Offset Voltage and Finite Output Swing

The offset was never considered as an important factor in previous behavioral models [8–10]. However, the test accuracy of the digital stimulus is actually much improved due to the unavoidable offsets of the integrators. Excluding the offset will introduce significant simulation errors. Figure 9 plots the stimulated SNRs with different stimulus amplitudes. Both OPAMPs are assumed to have a 75 dB gain and a 410 μV offset.

Comparing Fig. 9 with Fig. 7, the digital stimuli now show much higher SNR results. The reason can be better understood by examining Fig. 10. This illustration plots the output spectrum of the MUT with the same −40 dBFS, third-order digital stimulus applied to Fig. 8. The in-band spurs become much less significant implying that the offsets help de-correlating the shaped noises. Recall that Σ-Δ modulators generate pulse-density-modulated output bit-streams. Since the generated signed digital stimulus, $X_{BSG}(z)$, contains no dc term while the signed digital output of the MUT ($Y_o(z)$) does, these two bit-streams are not likely to be highly correlated. As a result, the shaped noise correlation is mitigated.

Figure 11 shows the SNR differences between with and without offset voltages when the OPAMP gains are all 75 dB and the stimulus amplitude is −40 dBFS. Although the offsets do not affect the test results of the conventional analog stimulus, they do have profound effects on the digital ones. Without any

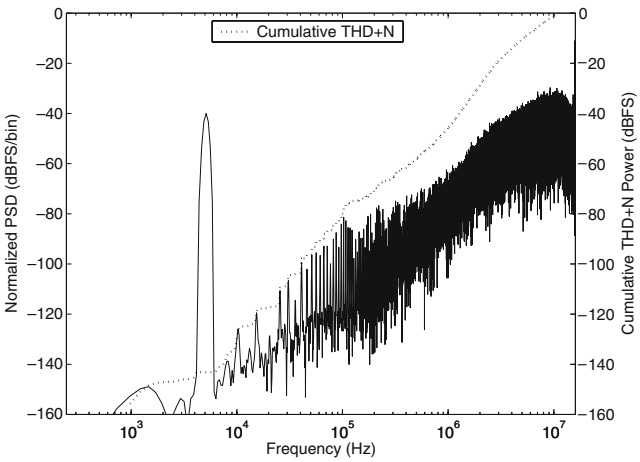

Fig. 8 Output spectrum of the MUT with the third-order, −40 dBFS digital stimulus. Only the 75 dB OPAMP gains are considered

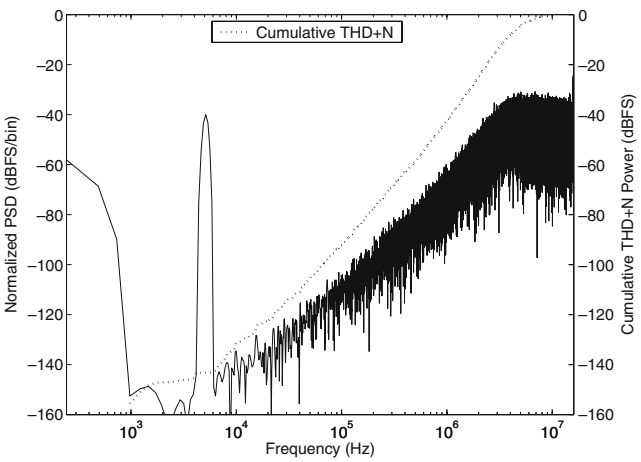

Fig. 10 Output spectrum of the MUT with the third-order, −40 dBFS digital stimulus. The gains and offsets of the OPAMPs are 75 dB and 410 μV respectively

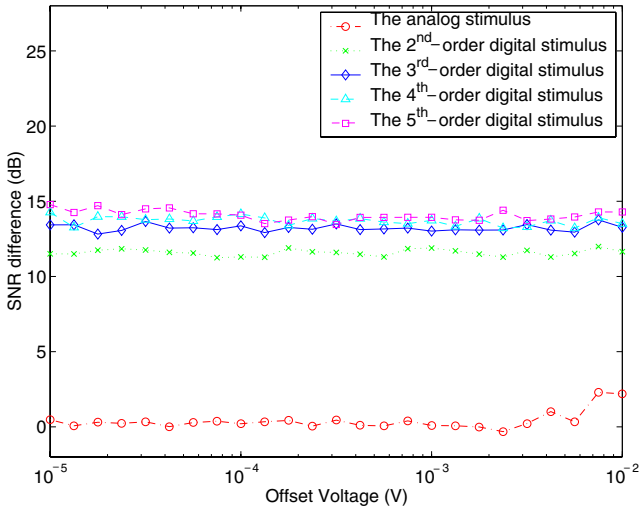

Fig. 11 SNR difference between with and without offset voltages. The OPAMP gains are 75 dB

offset, all digital stimuli only deliver SNR results around 35 dB. However, an offset voltage as small as 10 μV instantly improves these values over 11 dB. Practical offset of a properly designed OPAMP is around several millivolt, the digital stimuli thereby do not suffer from severe SNR degradation.

4.4 Thermal Noise and Flicker Noise

To predict the MUT's SNR more accurately, the final parameters added to the FSLB+N model are the thermal noise and the flicker noise. Figure 12 shows the simulation results of the complete FSLB+N model.

According to the requirement of Eq. 8, the intuition suggests using the BSG with the highest possible order. Indeed, the second-order BSG does provide a smaller SNR result than the other BSGs do in most of the tests.

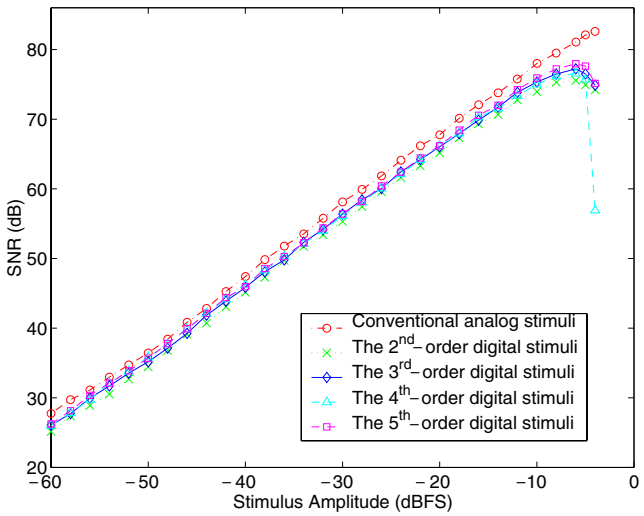

Fig. 12 SNR vs. stimulus amplitude of the MUT with the complete FSLB+N model

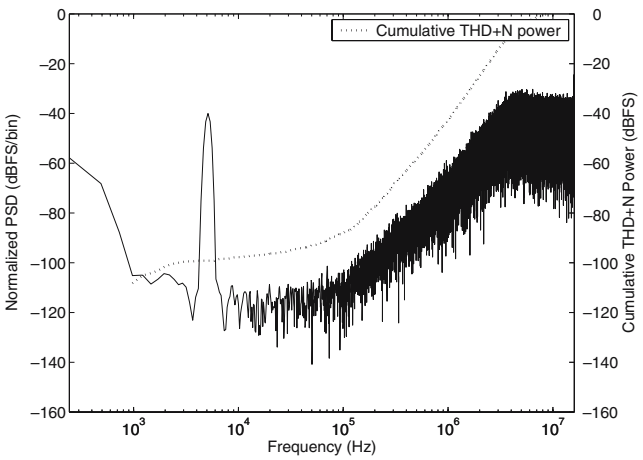

Fig. 13 Output spectrum of the MUT with the third-order, −40 dBFS digital stimulus using the complete FSLB+N model

However, the simulation results indicate the fourth-order BSG is inferior to the third-order one for testing the peak SNR, even though the fourth-order stimulus does contain much less in-band noise than the third-order one as shown in Fig. 5.

The simulation results also indicate that the fifth- and the fourth-order BSG candidates are not suitable for the test that requires a stimulus amplitude larger than −5 dBFS. The third-order BSG is found to be the most appropriate for general tests of the MUT.

Different MUTs may have different choices. With the proposed FSLB+N model, design engineers can design their own BSG structures and check their performance within a short turnaround time.

Figure 13 shows the output spectrum of MUT with the complete FSLB+N model. The same −40 dBFS, third-order digital stimulus was applied. Comparing it with Fig. 10, a noise floor appears. To demonstrate that the FSLB+N model can be used for projecting and evaluating the performance of the digital stimuli, Fig. 14 illustrates the measured output spectrum of the MUT with the same digital stimulus as a reference. As can be seen, Figs. 13 and 14 show a great resemblance.

5 Performance of the FSLB+N Model

5.1 Model Accuracy

To check the accuracy of the proposed FSLB+N model, the simulation results are compared with the measurement data of the DfDT second-order Σ-Δ modulator manufactured by a 0.35 μm CMOS mixed-signal process. The measurements were done at a sampling rate of 32 MHz, which is the measured maximum speed of the test chip operating in the normal mode without

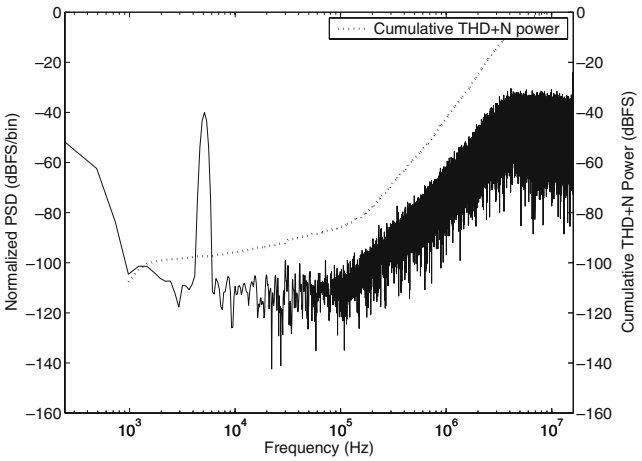

Fig. 14 Measured output spectrum of the MUT with the third-order, −40 dBFS digital stimulus

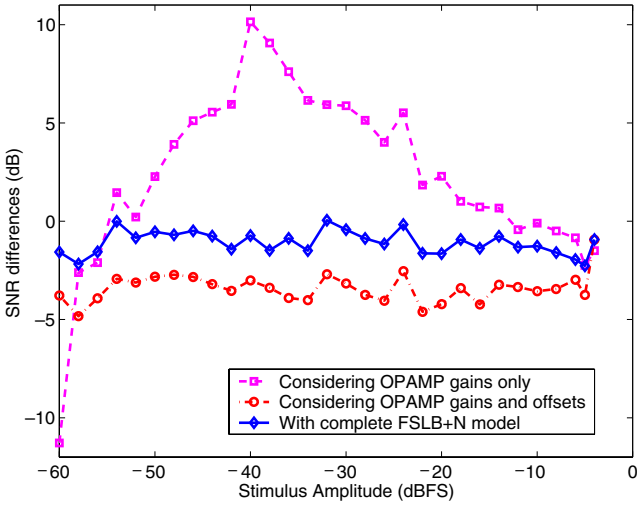

Fig. 16 SNR differences between the measurement data and corresponding simulation results of the MUT in the test mode

significant SNR degradation. At this extremely high sampling rate, the effects of a finite bandwidth and slew rate of the OPAMPs will be the most significant. The rest of the test setups such as the stimulus frequency, the reference voltages, and so on are the same as those applied to the behavioral simulations mentioned above. The third-order BSG is used to conduct the experiments in the test mode.

Figure 15 compares the simulation results of Figs. 7, 9, and 12 with the measurement data of the MUT in the normal mode. Essentially, the behavioral simulation results with the complete FSLB+N model are consistent with the measurement data. The SNR differences between the measurement data and simulation results

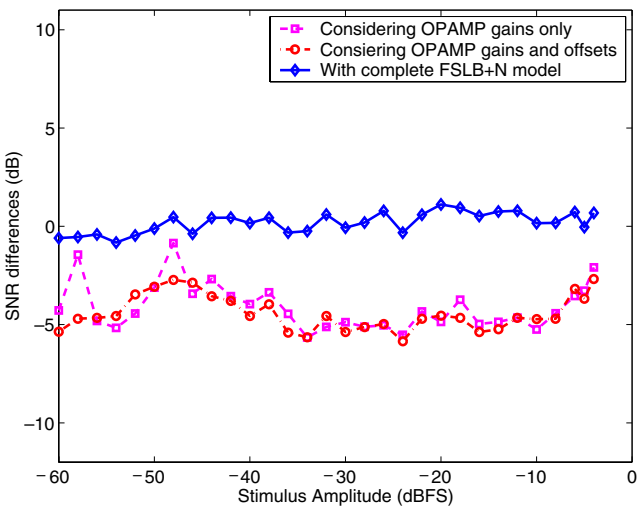

Fig. 15 SNR differences between the measurement data and corresponding simulation results of the MUT in the normal mode

show an average value of 0.2 dB with a maximum value of 1.1 dB and a minimum value of −0.8 dB. As shown, the finite gains and nonzero offsets of the OPAMPs are less critical for simulating the MUT operating in the normal mode. The noise sources dominate the simulation accuracy.

The comparison results of the test mode enabled MUT are different as shown by Fig. 16. The simplest model considering only the finite OPAMP gains gives the worst SNR prediction. The SNR differences between corresponding measurements and simulations range from −11.3 to 10.1 dB. Including the offsets effectively improves the SNR differences to be no worse than −5 dB. As such, including the offsets to the behavioral model is essential to achieve a more precise simulation for the MUT operating in the test mode. Aside from these, another concern is that what will happen if the modelled offset values are different from what the MUT actually has? As Fig. 11 indicated, the accuracy of the offsets are insensitive in most cases as long as they are nonzero.

The noise sources further improve the simulation accuracy. The SNR differences between the measured data and the corresponding simulation results using the complete FSLB+N model range from 0.05 to −2.2 dB with an average of −1.1 dB. This average value is 1.3 dB lower than that of the normal mode case. In other words, the MUT exhibits an extra 1.3 dB noise power when the test mode is enabled.

Figure 17 illustrates the output spectra of the peak SNR test for further analyze the differences between the measured data and simulation results. The same third-order, −6 dBFS digital stimulus were

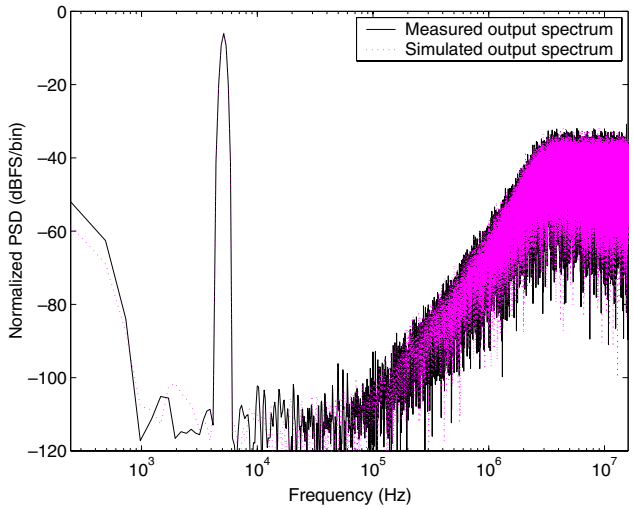

Fig. 17 Measured and simulated output spectra of the MUT with the same third-order, −6 dBFS digital stimulus

applied. Both measurement and simulation show almost the same high frequency noise components, but their in-band noise floors look different. The measured spectrum of the digital stimulus shows some spurs that are less significant in the simulated one. They are absent in the measured output spectrum of the corresponding analog stimulus as well. It implies that some signal coupling mechanisms of the fabricated MUT inter-modulate the test stimulus tone to the high frequencies. Since the digital stimuli contain significant high frequency shaped noises, these noises will be inter-modulated into the passband as well. Consequently, the in-band noise power increases. The simulation results can be improved by adding more comprehensive parameters to the model such as those for capacitive crosstalk, the nonlinearity of the OPAMP gains, and other inter-modulation mechanisms at the cost of increased modeling complexity and a longer simulation time.

5.2 Simulation Time

Table 1 compares the simulation times and results of two tools on the same computer. The first one used MATLAB with the proposed FSLB+N model. The other exerted HSPICE. The measurement result was also listed as a reference. Due to the extremely long simulation time, the sample points taken from the HSPICE simulation are limited to 8,292. As shown, even the sample points of the MATLAB simulation are 17 times more, the behavioral simulation is still 694,500 times faster and provides an SNR result within 2.2 dB of the measured data. The SNR obtained by HSPICE is lower because neither any noise nor any offset was taken into account. The limited sample number for analysis also reduces the prediction accuracy.

6 Conclusion

In this paper, an FSLB+N model for the DfDT Σ-Δ modulator is presented. Our goal is to improve the simulation time and accuracy in the test mode. The model considers the finite open-loop gains, the offsets, the limited output swings, the flicker noises of the OPAMPs, and the thermal noises induced by the switched capacitors, the OPAMPs, and the reference supplies. The SNR differences between the measured data and the simulation results of the second-order MUT have a mean value of −1.1 dB, a maximum of 0.05 dB, and a minimum value of −2.2 dB. Comparing with the conventional circuit-level simulation, the behavioral simulation with the FSLB+N model is 1,190,000 times faster while it achieves compatible accuracy. The simulation results can be improved by adding more comprehensive parameters such as those for capacitive crosstalk, nonlinearity of the OPAMP gains, and other inter-modulation mechanisms at the expense of increased modeling complexity and simulation time. The proposed model not only can be used to evaluate the digital stimulus candidates, but also can be used in system-level simulations of the mixed-signal design with an embedded DfDT Σ-Δ modulator.

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Table 1 Performance of the test mode simulations with the same −6 dBFS digital stimulus

Tool	Simulated samples	Simulation time (s)	Peak SNR result (dB)
MATLAB with FSLB+N	142,000	4.188	77.3
HSPICE	8,292	2.91×10^5	72.0
Measurement	131,072	–	75.3

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Hao-Chiao Hong received his B.S., M.S., and Ph.D. degrees in electrical engineering in 1990, 1992, and 2003 respectively, all from National Tsing-Hua University, Hsin-Chu, Taiwan.

He joined TSMC, Hsin-Chu, Taiwan in 1997 where he developed DACs and PLLs for various customers. He also designed specialized IPs of the mixed-signal test vehicles for monitoring the processes. From 2001 to 2004, he was a senior manager of Intellectual Property Library Company, Hsin-Chu, Taiwan where he led Mixed-Signal IP Department developing customized mixed-signal IPs.

Dr. Hong is currently an assistant professor of Electrical and Control Engineering Dept., National Chiao Tung University, Hsin-Chu, Taiwan.

His research interests include design-for-testability and built-in-self-test techniques for mixed-signal circuits, as well as high performance mixed-signal circuit design.