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This study reveals the formation of nickel-oxygen-silicon nanoparticles with nonvolatile memory effect by sputtering a commixed target in argon and oxygen ambiance. A transmission electron microscope clearly shows the embedded nanoparticles in the silicon oxide and the constituent was examined by x-ray photoelectron spectroscopy. The capacitor structure with embedded nickel-oxygen-silicon nanoparticles was also studied and it exhibited hysteresis characteristics after electrical operation. The memory window and retention of nickel-oxygen-silicon nanoparticles were enough to apply on nonvolatile memory. In addition, a physical mechanism was deduced to expound the role of oxygen in the formation of nickel-oxygen-silicon nanoparticles. © *2007 American Institute of Physics.* [DOI: 10.1063/1.2816125]

Nonvolatile memory (NVM) plays an important role in the market of portable electronic products and is required for further possessing the high memory capacity, low-voltage, and high-speed operation for next-generation memory with scaling down devices.[1–3] However, the carriers will run out of the floating gate since the tunnel oxide of conventional NVM generates leakage paths during endurance test. Therefore, the tunnel oxide thickness is difficult to scale down in terms of charge retention and endurance characteristics. The nonvolatile nanoparticle memory devices are promising to substitute for the conventional floating gate memory because the discrete traps as the charge storage media have been reported that they can effectively avoid data loss under reliability test for the scaling down devices.[4,5] Among various nanoparticles for memory technology, the metallic nanoparticles were extensively investigated over semiconductor nanoparticles because of several benefits, such as enhanced gate control ability (i.e., stronger coupling with the conduction channel), higher density of states, and smaller energy disturbance and larger work function (faster programing time and better data retention).[5,6] In addition to the nanoparticle application, the induction of charge trapping layer can increase trap states to improve charge storage capacity for the metal nanoparticle memory devices, such as those embedded in the SiO_x and SiN_x layer.[7] In this work, a simple process was proposed to form nickel-oxygen-silicon (NiOSi) nanoparticles by sputtering a commixed target ($Ni_{0.3}Si_{0.7}$) in argon (Ar)/oxygen (O_2) ambiance at room temperature. Material and electrical analyses were performed to study the metal nanoparticles memory.

This nonvolatile memory-cell structure in this letter was fabricated on a 4 in. *p*-type silicon (100) wafer. After a Radio Corporation of America (RCA) standard clean process which removed native oxide and microparticles form wafer surface, 3-nm-thick tunnel oxide was thermally grown by a dry oxidation process at 950 °C in an atmospheric pressure chemical vapor deposition furnace. Afterwards, a 10-nm-thick charge tapping layer was deposited by reactive sputtering (metallic mode) with the 4 in. $Ni_{0.3}Si_{0.7}$ commixed target in the Ar/O_2 [24/2 SCCM (SCCM denotes cubic centimeter per minute at STP)] ambiance at room temperature. The direct current (dc) sputtering power and pressure of sputter system were set to 80 W (the deposition rate ~0.2 Å/s) and 7 mtorr. During the foregoing process, nanoparticles could be found to precipitate and embed in SiO_x layer because of the competition of oxygen between silicon and nickel in the oxygen incorporated $Ni_{0.3}Si_{0.7}$ layer (we discuss this formation mechanism of nanoparticles later). Then, a 30-nm-thick blocking oxide was deposited by the plasma enhanced chemical vapor deposition system at 300 °C. Al gate electrodes were finally deposited and patterned to form a metal/oxide/insulator/oxide/silicon (MOIOS) structure. Transmission electron microscope (TEM) analysis and x-ray photoelectron spectroscopy (XPS) were adopted for microstructure and chemical material analysis of nanoparticles. Electrical characteristics of the capacitance-voltage (*C-V*) hysteresis were also measured by HP4284 Precision *LCR* Meter with high frequency 100 kHz. Moreover, we fabricated an oxygen deficient $Ni_{0.3}Si_{0.7}$ layer which only used Ar (24 SCCM) during sputter process as charge trapping layer of MOIOS structure (control sample) to compare with the above-mentioned MOIOS structure for electrical characteristics of *C-V*.

Figure 1(a) shows a cross-sectional TEM image of control sample. It was found that a uniform $Ni_{0.3}Si_{0.7}$ layer was deposited on the tunnel oxide and the thickness of the $Ni_{0.3}Si_{0.7}$ layer was about 10–11 nm. However, the cross-

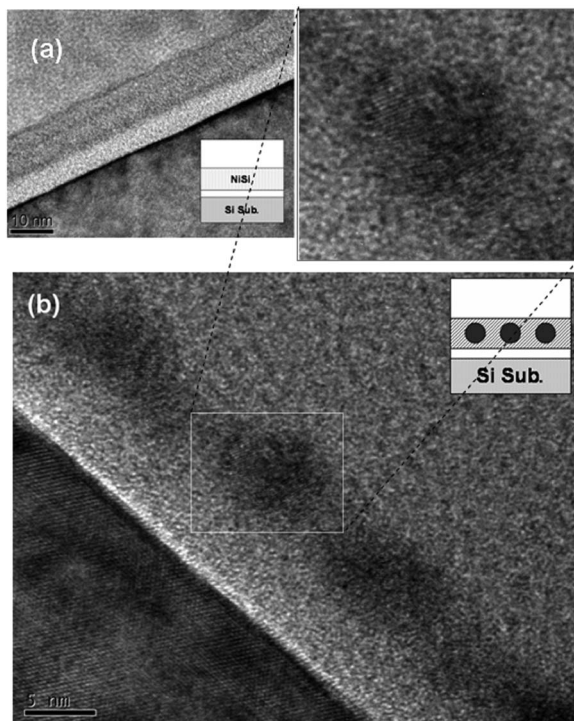[a]Electronic mail: tcchang@mail.phys.nsysu.edu.tw

FIG. 1. Cross-sectional transmission electron microscope (TEM) analysis of (a) control sample, and (b) MOIOS structure containing nanoparticles. The nanoparticles size and density are about 5–6 nm and 1.33×10^{12} cm^{-2}, respectively. The inset shows sketch diagrams of control sample and MOIOS structure.

FIG. 2. Capacitance-voltage (*C-V*) hystereses of MOIOS structure with (a) the control sample, and (b) NiOSi nanoparticles. The memory windows of NiOSi nanoparticles 0.8 and 2.5 V can be obtained under ±10 (dash line) and ±15 V (solid line) gate voltage operation, respectively.
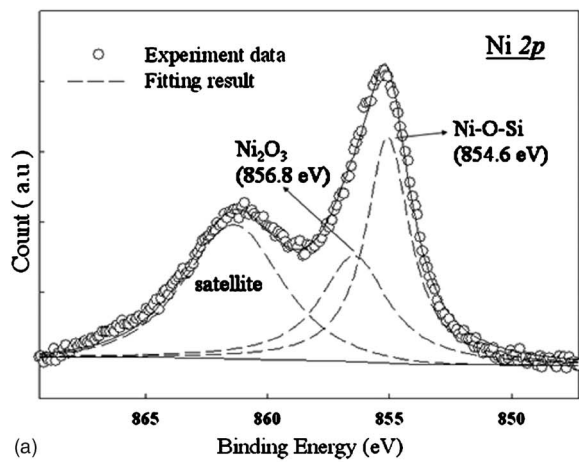
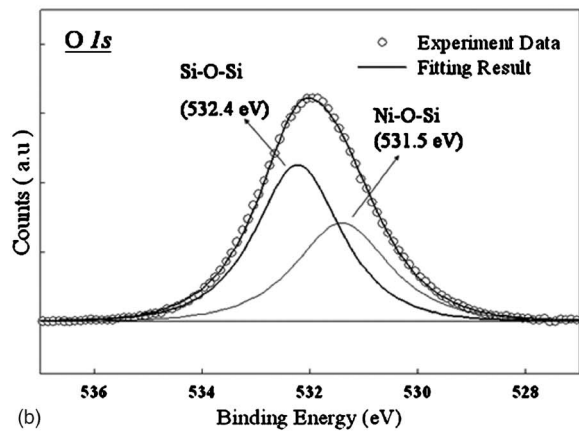sectional TEM image of MOIOS structure containing spherical and separated nanoparticles was shown in Fig. 1(b). It is found that the thickness of tunnel oxide is larger than 3 nm by TEM analysis, since this redundant SiO$_x$ matrix is formed form oxygen incorporated Ni$_{0.3}$Si$_{0.7}$ layer during sputter process. From TEM analysis, the average diameter of the nanoparticles is approximately 5–6 nm and the area density of the nanoparticles is estimated to be about 1.33×10^{12} cm^{-2}.

(*C-V*) hysteresis is shown in Figs. 2(a) and 2(b) for the control sample and nanoparticles, respectively. From Fig. 2(a), memory effect is not found in the control sample under ±10 V gate voltage operation. On the contrary, it is clearly observed that 0.8 and 2.5 V of memory windows can be obtained, respectively, under ±10 and ±15 V gate voltage operation for the MOIOS structure with nanoparticles, as shown in Fig. 2(b). Hence, it is considered that the memory effect of nanoparticles is dominated by formation of nanoparticles as compared with Fig. 2(a). Moreover, the hysteresis loops follow the counterclockwise direction due to injection of electrons from the inversion state and discharge of electrons from the accumulation state of Si substrate. The memory window of MOIOS with nanoparticles is enough to determine data information by different memory window for nonvolatile memory application. As a result, our electrical characteristics of *C-V* show that formation and nonvolatile memory effect of nanoparticles are influenced by oxygen doping during sputter process.

In our work, the chemical composition of the nanoparticles is demonstrated by XPS analysis using an Al $K\alpha$(1486.6 eV) x-ray radiation, as shown in Fig. 3. Figure 3(a) exhibits the XPS Ni 2*p* core-level photoemission spectra that consist of two main peaks, Ni 2$p_{3/2}$ and satellite. According to previous research,[8,9] the composition of Ni
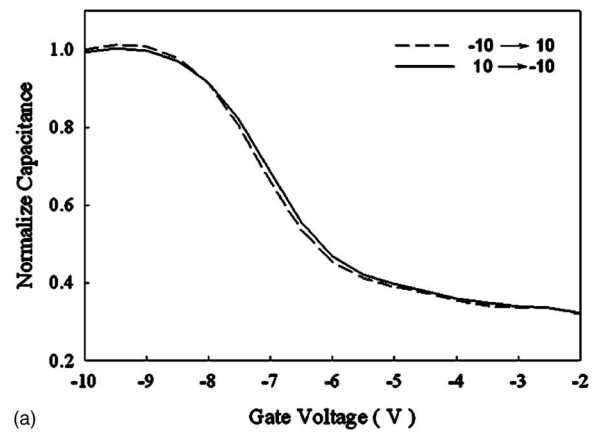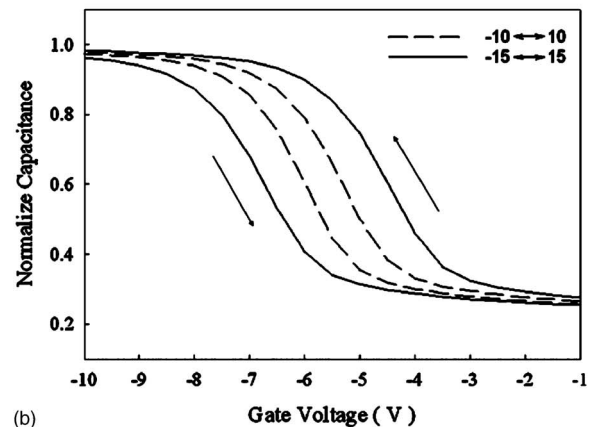
2$p_{3/2}$ peak can be separated out Ni–O–Si(854.6 eV) and Ni$_2$O$_3$(856.8 eV) by fitting results of XPS analysis.[10] The nanoparticle is thereby believed to be composed of Ni–O–Si ternary element. Moreover, the XPS O 1*s* photoemission spectra can be utilized to verify this contention, as shown in Fig. 3(b). By fitting result of experiment data, it is found that the main peak can be composed into two components which center at 531.5 and 532.4 eV corresponding to Ni–O–Si bond and Si–O–Si bond, respectively.[9] In addition, we can use XPS analysis to evaluate the atomic concentration in the trapping layer, which is 14%, 47%, and 39% for nickel, silicon, and oxygen of charge trapping layer, respectively.

For the formation of Ni–O–Si nanoparticles during sputter process, the enthalpies ($-\Delta H$) of Si–O, Ni–O and Ni–Si at room temperature are 799, 382, and 318 kJ mol^{-1}, respectively.[11] Because of the higher enthalpy of Si–O compared with Ni–O, the oxygen radicals can interact with Si atom easier than with Ni atom on the wafer surface during the sputter process. It can be explained that an internal oxidation reaction will induce self-assembled phenomenon of Ni–O–Si nanoparticles, which is dependent on the different enthalpies of compounds of charge trapping layer, as shown in Fig. 2(b). Therefore, Ni–O–Si nanoparticles can be formed at low temperature and no need of further thermal annealing in our experimental method.

Figure 4(a) demonstrates the data retention characteristics of the nonvolatile NiOSi nanoparticles memory at room temperature. The memory cell is programed by 10 V for 5 s, and erased −10 V for 5 s. The flatband voltage shift is ob-
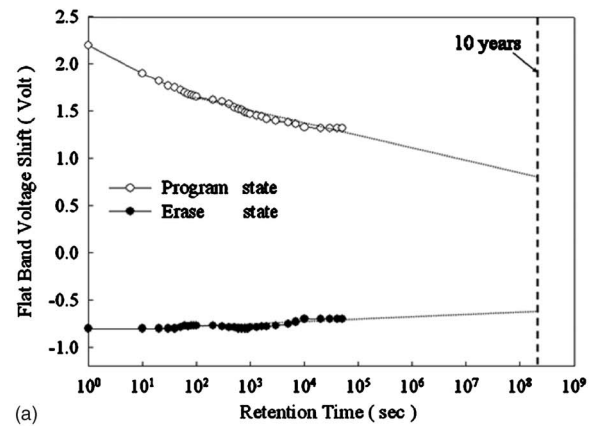
FIG. 3. (a) Ni 2*p* and (b) O 1 *s* x-ray photoelectron spectroscopy (XPS) analysis of the charge trapping layer. Empty circles and straight line indicate experimental and fitting results, respectively.

FIG. 4. (a) Retention characteristics of the memory structure with NiOSi nanoparticles using a ±10 V gate voltage stress for 5 s at room temperature. The dotted line is the extrapolated value of retention data after 100 s. (b) Programing and erasing characteristics of the NiOSi nanoparticles under ±10 and ±15 V gate voltage.
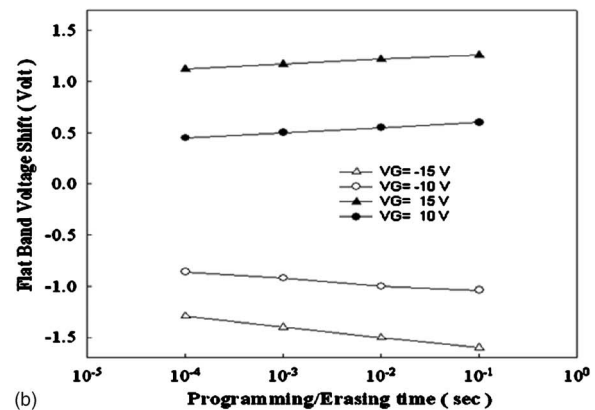
tained by comparing the *C-V* curves from a charged state and the quasineutral state. The memory window significantly decays during the first 100 s due to charge emission from the shallow traps in SiO$_x$ matrix to the substrate. However, a 1.4 V memory window (charge remained ratio of 50%) can be obtained even after 10 yr by analyzing the extrapolation value of retention data (stable range of $10^2 - 4 \times 10^4$ s).

Figure 4(b) shows the programing/erasing characteristics of NiOSi nanoparticles under ±10 and ±15 V. The flatband voltage shift is increased as the programing/erasing voltage increased at the same programing/erasing duration, and also increased with the increasing programing/erasing duration at the same programing/erasing voltage. Moreover, the defined window 0.5 V can be obtained at programing/erasing $\sim 10^{-4}$ s under ±10 V operation. This memory device reveals a high speed programing/erasing time for further nonvolatile memory application.

In conclusion, the NiOSi nanoparticles embedded in the SiO$_x$ layer were fabricated for the nonvolatile memory application by sputtering a commixed target in an Ar/O$_2$ environment at room temperature. Due to different enthalpies of Si–O, Ni–O, and Ni–Si, the nanoparticles can be self-assembly fabrication in this study. A larger memory window of 2.5 V was clearly observed after ±15 V voltage sweep and the retention can get up to 10 yr for NVM application. In addition, this memory device is suitable for high speed operation and the fabrication technique of NiOSi nanoparticles can be compatible with current manufacture process of the integrated circuit manufacture.

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