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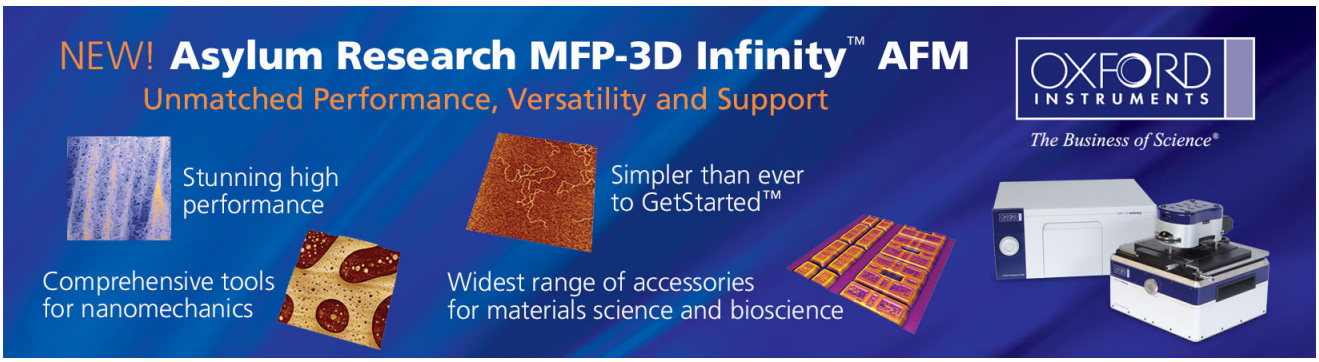

Pi-shape gate polycrystalline silicon thin-film transistor for nonvolatile memory applications

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In this work, we studied a pi-shape gate polycrystalline silicon thin-film transistor (poly-Si TFT) with silicon-oxide-nitride-oxide-silicon (SONOS) layers and nanowire channels for the application of electric driver and nonvolatile memory. The proposed pi-gate TFT-SONOS has superior transfer characteristics and its output characteristic also exhibits the high driving current and the suppression of the kink effect. For memory application, the device can provide high program/erase efficiency and large threshold voltage shift under adequate bias operation. The enhanced performance for the pi-gate TFT-SONOS is attributed to the larger effective channel width and the number of channel corners. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2813621]

In recent years, polycrystalline silicon thin-film transistors (poly-Si TFTs) have attracted much attention for active-matrix liquid crystal displays since they can be integrated on display panel as peripheral driving circuits.[1] In addition, the further improvement of poly-Si TFT's performance can enable various functional devices, such as memory and controller, to be integrated on a glass panel to achieve system-on-panel (SOP) display.[2,3] Because SOP technology is primarily used for portable electronics, low power consumption is basically required to maintain a long battery life. It is well known that the nonvolatile memory is widely utilized for data storage in portable electronics system due to its properties of low-power consumption and nonvolatility. Compared with the conventional nonvolatile floating gate memory, silicon-oxide-nitride-oxide-silicon (SONOS)-type memory has become a promising candidate for SOP application due to its full compatibility with poly-Si TFTs process. Recently, various approaches have been proposed for poly-TFTs combined with nonvolatile SONOS memory (TFT-SONOS) on SOP applications.[4,5] In our previous study,[6] the TFT-SONOS with nanowire channels was demonstrated to exhibit superior electrical performance for transistor and memory device due to good gate controllability.

However, in complementary metal-oxide semiconductor technology, high performance nonplanar multiple-gate structures in silicon-on-insulator (metal-oxide-semiconductor field-effect transistor), such as double-gate,[7] trigate,[8] pi-gate,[9] and gate-all-around structures,[10] have been reported to present greater gate control over channel than a conventional single-gate structure device. Different from the double-gate or gate-all-around devices, the pi-gate device can be easily manufactured and also exhibits excellent electric characteristics. Thus, in this paper, we propose the nanowire TFT-SONOS with pi-shape gate structure to enhance electric performance for the applications of transistor and high program/erase speed nonvolatile memory.

In this work, the pi-gate structure was formed on nanowire poly-Si channels (PN) with a buried oxide overetching. In addition, a series of standard TFT-SONOS memories without the implementation of buffer oxide overetching were also fabricated for comparison. These standard TFT-SONOS memory devices were marked as SN with ten strips of multiple 65 nm nanowire, S5 with five strips of multiple 0.2 μm channels, S2 with two strips of multiple 0.5 μm channels, and S1 with a single 1 μm of channel in width. The gate length of devices is kept 5 μm. First, an undoped 45 nm

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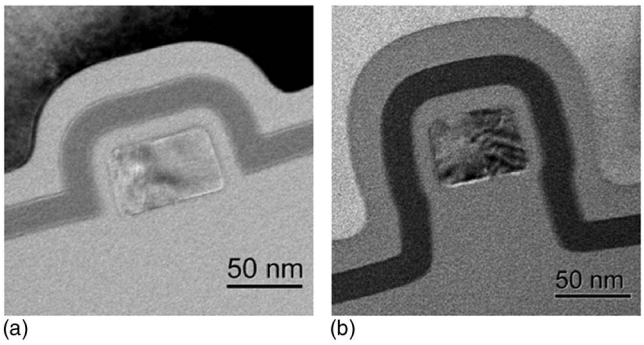
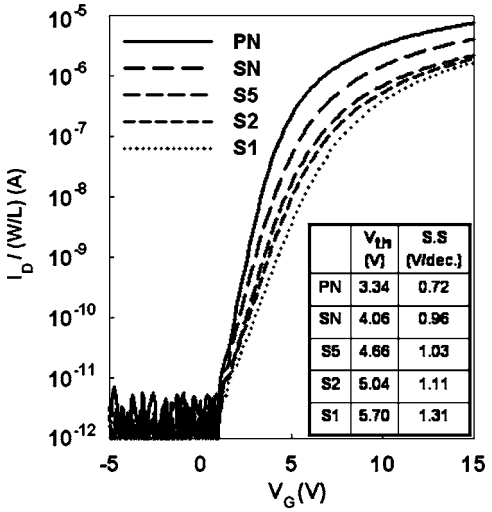


FIG. 1. Transmission electron microscopy of (a) the standard nanowire and (b) nanowire surrounded by pi-gate structures.

amorphous silicon (*a*-Si) was deposited on oxidized silicon wafers by low-pressure chemical vapor deposition (LPCVD) at 550 °C. Then, the deposited *a*-Si layer was recrystallized by solid-phase crystallization method at 600 °C for 24 h. After the active region patterning by electron beam lithography, for the pi-gate structure, the active layer and buried oxide were etched subsequently by reactive ion etching. The additional buried oxide overetching step can assure the vertical gate electrode extend over the bottom of nanowire. After the active region definition, an ONO multilayer gate dielectric with 15 nm tunnel oxide/20 nm silicon nitride/25 nm blocking oxide was deposited by LPCVD. Subsequently, a 150-nm-thick *in situ* n^+ doped poly-Si layer was deposited and transferred to a gate electrode. After the formation of source/drain with self-aligned phosphorous implantation, a 300 nm oxide passivation layer was deposited and contact holes were patterned. Finally, Al metallization performed and the devices were sintered at 400 °C in nitrogen ambient for 30 min.

Figures 1(a) and 1(b) show the transmission electron microscope photography of the standard nanowire structure and pi-gate structure. Obviously, in pi-gate device, the nanowire channel is surrounded by the control gate and the gate electrode extends to 20 nm in depth into the buried oxide. In addition to the top and two sides channel regions, the bottom channel and two additional corner regions also can be controlled by the extended gate electrode. The physical width of nanowire channel and the thickness of ONO are also confirmed to be 65 and 60 nm, respectively. Figure 2 presents the typical I_D-V_G curves of the PN and the standard devices with different channel width structures. The threshold voltages and subthreshold swing (SS) are also extracted in the insert tables. The result reveals that the PN device has superior performance than those of other devices, exhibiting the highest on-current, smallest threshold voltage (V_{th}) and SS. For the standard devices, the electrical characteristics are improved as the channel width decreased. The gate fringing field crowding at the channel surface and corner regions can induce a larger electrical field as the channel width is scaling down. Hence, the standard devices with the decreased width will obtain the better gate control ability. For the PN device, compared to the SN device, the electrical performance is enhanced further due to the effective channel width and corner numbers are increased. In addition, the corner current can provide most of the total current as the device operated in subthreshold region.[8] The pi-gate device has most corner numbers, thus, it has the best subthreshold behavior.



	V_{th} (V)	S.S (V/dec.)
PN	3.34	0.72
SN	4.06	0.96
S5	4.66	1.03
S2	5.04	1.11
S1	5.70	1.31

FIG. 2. Comparison of typical I_D-V_G characteristics of the pi-gate TFT-SONOS and the standard TFT-SONOSs with different channel width. The threshold voltages and SS of all devices are also extracted in the inset tables.

Figure 3 shows the typical output characteristics of standard and pi-gate devices. By comparing with all devices in this work, the pi-gate device has the highest driving current due to the larger effective channel width. Moreover, due to the presence of the abundant grain boundary trap states in poly-Si film, the conventional device will suffer from severe impact ionization, which causes the pronounced kink effect at high drain bias (V_D). It is clearly found that the drain current becomes larger and the kink effect is less pronounced as the channel width is decreased. This result implies the device with narrower width can provide a better gate control ability to shield the electric field lines from the drain. The horizontal electrical field is thereby reduced and the output characteristic is improved. It is well known that the impact-ionization rate is also related to the current density. Hence, in pi-gate device, the increased current contributes to impact-ionization effect and results in the slightly kink effect.

In addition to transistor application, the TFT-SONOS also can be functioned as a nonvolatile memory under adequate gate voltage operation. Tunneling current is mainly dominated by Fowler-Nordheim (FN) tunneling as the thickness of tunneling oxide is thicker than 5 nm.[11] In this work, therefore, the devices could be programed and erased by FN tunneling mechanism. Figures 4(a) and 4(b) show the programing and erasing characteristics of the S1, SN, and PN

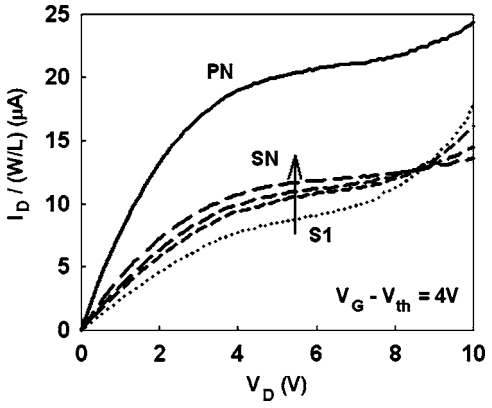


FIG. 3. Output characteristics of the pi-gate TFT-SONOS and the standard TFT-SONOSs at (V_G-V_{th})=4 V.

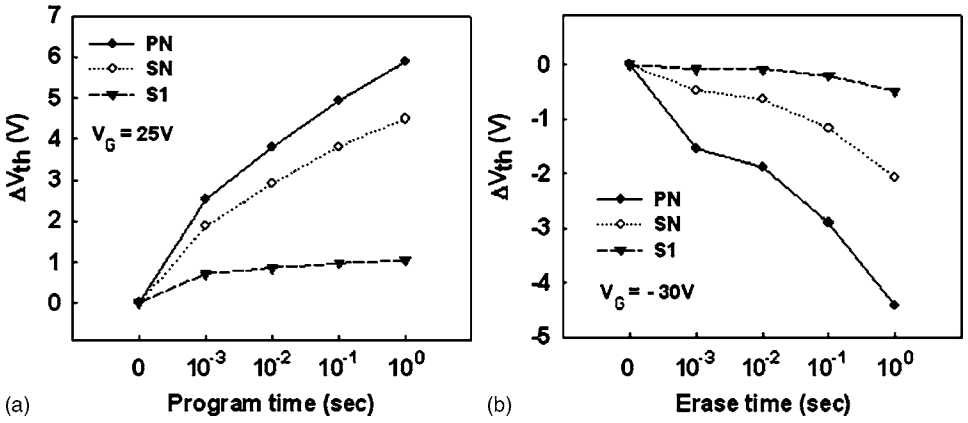


FIG. 4. (a) Programing and (b) erasing characteristics of the S1, SN, and PN devices. The devices with nanowire channels show that V_{th} shift significantly increases comparing to S1 device.

devices. In general, for FN tunneling mechanism, the electrical field required for an apparent tunneling current is around 6 MV/cm.[12] The effective oxide thickness of the stacked ONO multilayer is about 50 nm in this work. Thus, the program/erase efficiency of S1 device is very low even at the gate voltages of 25 and −30 V. However, for SN and PN devices, the electrical field at the corner region is much higher than that at noncorner region due to the corner effect. The results also reveal that the electrons mainly tunneled via the corner region and then were stored in nitride layer. Because there are four corners around the nanowire for pi-gate structure, the PN device has the superior program/erase efficiency and the larger threshold voltage shift comparing the SN device.

In summary, the pi-gate TFT-SONOS functioned as both transistor and nonvolatile memory is demonstrated in this work. The experimental results show that the pi-gate SONOS-TFT has the superior electrical characteristics due to the increased effective channel width and additional corner current induced by corner effect. In addition, the proposed device also exhibits memory characteristics with high program/erase speed under adequate bias operation (>20 or <-20 V). Thus, pixel transistor in display area and functional memory circuitry in the peripheral system area can be fabricated at the same time, and the functions of TFT-SONOS can be controlled by different bias operation (for pixel transistor application, the operated gate voltage should be below the FN tunneling threshold). Although the pi-gate TFT-SONOS cannot be easily fabricated using panel maker's existing manufacturing facilities, it is still an applicable technology for system-on-panel display in the future.

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