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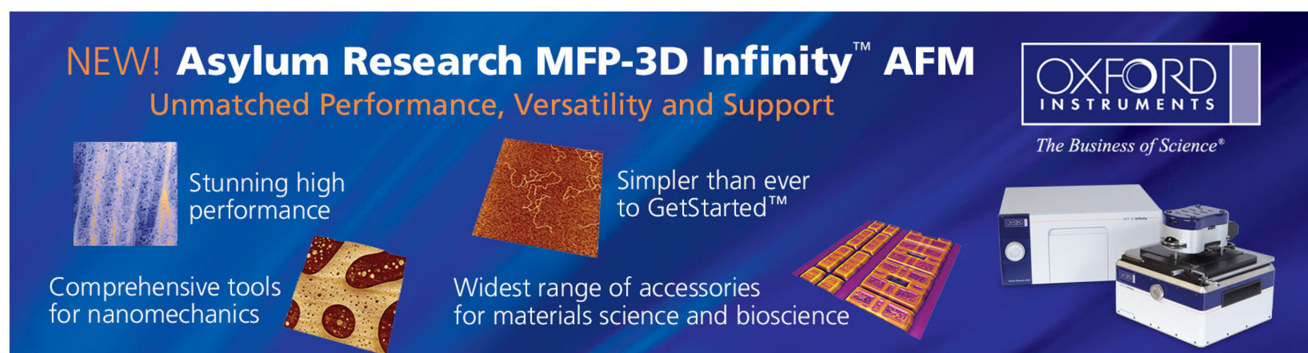

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Polycrystalline silicon thin-film transistors with location-controlled crystal grains fabricated by excimer laser crystallization

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In this paper, location-controlled silicon crystal grains are fabricated by the excimer laser crystallization method which employs amorphous silicon spacer structure and prepatterned thin films. The amorphous silicon spacer in nanometer-sized width formed using spacer technology is served as seed crystal to artificially control superlateral growth phenomenon during excimer laser irradiation. An array of 1.8-μm-sized disklike silicon grains is formed, and the *n*-channel thin-film transistors whose channels located inside the artificially-controlled crystal grains exhibit higher performance of field-effect-mobility reaching 308 cm^2/V s as compared with the conventional ones. This position-manipulated silicon grains are essential to high-performance and good uniformity devices. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2801525]

Low-temperature polycrystalline silicon thin-film transistors (TFTs) have been extensively studied for active matrix flat panel displays (AMFPDs) and potential for three-dimensional integrated circuit (3D-IC) applications owing to their high driving-current capability.[1,2] Metal-induced lateral crystallization (MILC) of amorphous silicon (*a*-Si) thin film has been proved to produce good-performance polycrystalline silicon (poly-Si) TFTs.[3] However, metal contamination and high intragrain defect densities in MILC poly-Si thin films degrade TFT performance, such as large leakage current and high subthreshold swing.[4] At this moment, excimer laser crystallization (ELC) seems to be the most promising method for its great potential in mass production and high quality silicon grains without damage to glass/plastic substrates. However, the average grain size of poly-Si thin films crystallized by conventional ELC is less than 0.8 μm, which results in inferior TFT performance as compared with silicon-on-insulator (SOI) metal-oxide-semiconductor field-effect transistor.[5] Since the randomness of grain-boundary location and the electrical potential barrier localized at the grain boundaries are the major factors in causing the device nonuniformity and degrading the TFT performance by hindering the carrier transport,[6] enlarging silicon grain size and controlling the grain boundary location are effective approaches to high-performance TFT and good device uniformity.[7–11] For realizing system-on-panel (SOP) technology, integrating memory, microprocessor unit, etc., on a single substrate, both of the device performance and device-to-device uniformity need further enhancement. Single-grain TFT in which the channel is grain-boundary-free will exhibit SOI-like performance to satisfy the requirements of SOP. More researches, therefore, have been devoted to the two-dimensional grain control, aiming at single-grain TFT.[7,9,10,12–14]

In our previous work, the laser crystallization method with *a*-Si spacer structure has been proposed and demonstrated to produce one-dimensional periodically lateral silicon grains.[15] The purpose of this paper is to present a crystallization method for producing high quality two-dimensional lateral grain growth based on spatial temperature distribution and artificial sites. 1.8-μm-sized disklike grains can be artificially grown in the channel regions via the *a*-Si spacer structure and prepatterned silicon thin film with excimer laser irradiation. The experimental results exhibit that both the device performance and the device-to-device uniformity are improved in proposed TFTs.

Figure 1 illustrates the key processes for the fabrication of excimer-laser-crystallized poly-Si TFTs with *a*-Si spacer

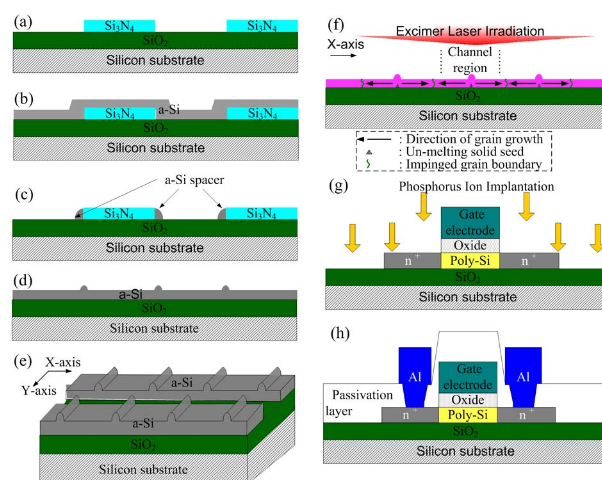

FIG. 1. (Color online) The key processes for the fabrication of poly-Si TFTs with *a*-Si spacer structure and prepatterned silicon thin films.

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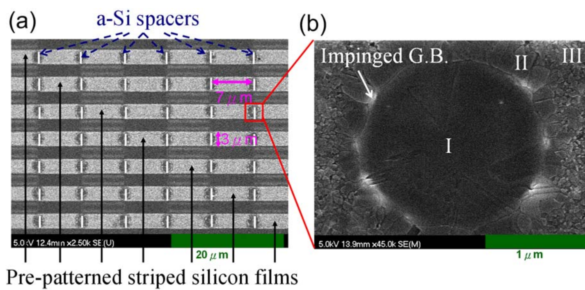

FIG. 2. (Color online) (a) SEM graph of excimer-laser-crystallized striped poly-Si films with amorphous Si spacer structure after Secco etching and the disklike grains with 1.8 μm in length formed periodically. (b) Enlarged SEM graph focuses on single silicon grain.

structure and prepatterned silicon thin films. At first, Si_3N_4 thin film with a 500 Å thickness was deposited on oxidized silicon wafer with oxide thickness of 1 μm and was defined to form individual islands [Figure 1(a)]. Then, a 1000 Å *a*-Si layer was deposited by pyrolysis of pure silane (SiH_4) gas source with low pressure chemical vapor deposition (LPCVD) at 550 °C [Fig. 1(b)]. The *a*-Si layer was subjected to reactive ion etching (RIE), so that the *a*-Si spacer with a 500 Å height was formed at the sidewall of the Si_3N_4 islands, as shown in Fig. 1(c). After removing the Si_3N_4 layer, another 1000 Å *a*-Si layer was deposited by LPCVD. Therefore, *a*-Si thin film with two kinds of thicknesses (1000 and 1500 Å) in a local region was formed by this spacer technique [Fig. 1(d)]. *a*-Si layer was subjected to another RIE to define silicon stripes which were perpendicular to the previous Si_3N_4 islands, as shown in Fig. 1(e). After RCA cleaning process, the samples were subjected to 248 nm KrF ELC in a vacuum chamber pumped down to 10^{-3} Torr [Fig. 1(f)]. The number of laser shots per area was single pulse and laser energy density was controlled in the near-complete-melting regime for 1500-Å-thick *a*-Si spacers and completely melting condition for 1000-Å-thick *a*-Si thin films.[6] The surface morphology and microstructure of laser-crystallized poly-Si thin films were analyzed by transmission electron microscopy (TEM) and scanning electron microscopy (SEM), respectively. The TEM samples were prepared via the focused-ion-beam (FIB) technique and the SEM samples were prepared using the Secco-etching process. After laser crystallization, poly-Si thin films were etched to form the device active region. Then, a 1000-Å-thick tetraethyl orthosilicate gate oxide was deposited by LPCVD. A 2000-Å-thick *a*-Si thin film was deposited by LPCVD for formation of the gate electrode. Then, *a*-Si thin film and gate oxide were etched by RIE to form the gate electrode. A self-aligned phosphorous ion implantation with dose of 5×10^{15} cm^{-2} was carried out to form source and drain regions [Fig. 1(g)]. Next, the typical passivation layer deposition, dopant activation, contact hole opening, metallization, and sintering processes completed the fabrication of TFTs with prepatterned spacer structure [Fig. 1(h)]. No hydrogenation plasma treatment was performed during the device fabrication process. For comparison, the conventional ELC poly-Si TFTs with an average grain size of about 5000 Å and a channel thickness of 1000 Å were also fabricated in the same run.

Figure 2(a) displays the SEM graph of excimer-laser-crystallized poly-Si thin films with prepatterned *a*-Si spacer structure after Secco etching. In this case, the thick region of *a*-Si spacer is 1500 Å and a-Si in the other thin region is 1000 Å. The distance between adjacent *a*-Si spacers is 7 μm and the width of the prepattern silicon stripes is 3 μm. The locations of *a*-Si spacer seeds and the prepattern silicon stripes are indicated by the white dash lines and the solid black arrowhead lines, respectively. The laser energy fluence is controlled at 475 mJ/cm^2 (near-complete-melting condition for 1500-Å-thick *a*-Si spacers) and the substrate temperature is isothermally heated at 400 °C during laser irradiation to reduce the cooling rate of the complete melting silicon for enlarging silicon grain size.[16] It can be observed that disklike grains are formed periodically in the laser-crystallized poly-Si thin film, as shown in Fig. 2(a). Figure 2(b) shows the enlarged SEM graph to focus on a single grain with grain size of 1.8 μm in diameter, and there are three different kinds of poly-Si regions, which are the large disklike grain formed in the center of the striped poly-Si film (region I), the radial grains (~150-nm-sized) surrounded the large disklike grain in the form of thin ring (region II), and the small and fine grains (~40-nm-sized) in the outer zone (region III). The scenario for this crystallization mechanism of *a*-Si thin films is described as follows. It has been reported that lateral thermal gradient could arise as a result of the heat generated at moving solid-melting interfaces.[6] In our proposed ELC method, as excimer laser irradiation is performed on the striped amorphous silicon thin film with *a*-Si spacers, the laser energy densities can cause the complete melting of 1000-Å-thick silicon thin film but near-complete melting of 1500-Å-thick *a*-Si spacer. In addition, along the *y* axis, since the edges of the striped silicon films adjacent to the air during laser irradiation and the surface regions of the bulk silicon wafer outside the prepatterned stripes can absorb intense excimer laser UV light, they are melted to high temperature. Therefore, for the striped silicon films, the cooling rate of the edges is slower than that of the center because of the poor thermal conductivity of air and the heated surface regions of the bulk silicon wafer by laser irradiation. Therefore, the temperature near the edges of the striped Si films is higher than that in the center of the striped films. As a result, the temperature gradient also occurs along the *y* axis due to surface tension effect and additional heat reservation at the edges of striped films so that the numbers of silicon solid seeds are gradually reduced resulting from prepatterned effect.[17,18] As a result, only a part of the spacers survive to serve as the seeds and a large lateral thermal gradient will exist between the unmelting solid seeds and the complete-melting liquid regions. Therefore, the residual seeds will proceed to start the lateral grain growth in the silicon films and extend toward the completely melted region until the solid-melting interface from opposite direction impinges after excimer laser irradiation, forming region I with the disklike grain of 1.8 μm in diameter. For the complete-melting outer zone, fine-grained poly-Si form region III due to the random spontaneous nucleation in the severely deep supercooling of melting liquid silicon films. Finally, the spontaneously nucleated grains grow inward and then impinge on the oncoming lateral disklike grain; therefore, radial grains form region II. It is also found that the locations of the grain boundaries where grains collide with each other shows brightly shining parts [indicated by an arrow in Fig. 2(b)].[19] Figure 3(a) shows the plane-view TEM image of the silicon film after ELC, which exhibits a 1.8-μm-sized silicon grain formed at the artificial site. This disklike grain is analyzed by its electron diffraction pattern and it reveals that the silicon grain

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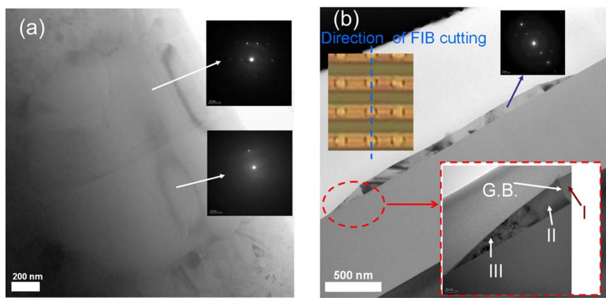

FIG. 3. (Color online) (a) Plane-view TEM image and the selected-area electron diffraction pattern of the disklike grain. (b) Cross-sectional TEM image of striped silicon film displays the disklike grain. The insets of (b) are optical micrograph, electron diffraction pattern, and magnified cross-sectional TEM image.

has an excellent crystallinity due to the clear dot pattern. The crystallization mechanism we proposed is further verified by the cross-sectional TEM image [Fig. 3(b)]. The blue dash line indicates the cutting direction of FIB-prepared sample shown in the inset optical micrograph of Fig. 3(b). The bright-field TEM image and the selected-area electron diffraction pattern show that the edges of the stripe silicon films become thinner, attributed to the surface tension effect after laser irradiation, and the lateral silicon grain possesses a good crystallinity, respectively. Moreover, the inset high-magnification cross-sectional TEM image of Fig. 3(b) displays that these three different kinds of poly-Si regions and the impinged grain boundary are apparently recognized, which are consistent with our proposed mechanism. Figures 4(a) and 4(b) compare the transfer and output characteristics of poly-Si TFTs on location-controlled silicon grains with those of conventional TFTs on random grain structure for $W=L=1.5\ \mu$m. Poly-Si TFTs made by this crystallization exhibit a higher field-effect mobility $(308\ \mathrm{cm^2/V\ s})$ and a lower leakage current than those of conventional ones. The superior performance of proposed TFTs is attributed to the high quality large silicon grains grown in the device channel region. Table I lists the average values of several important electrical characteristics of the two different TFT structures with the standard deviations in parentheses. Ten TFTs were measured in each case to investigate the device-to-device variation, and the laser energy density was controlled at nearly optimal value for these two different TFT structures. As compared with the conventional TFTs, the small standard deviations of proposed TFTs indicate an improved uniformity owing to the location-controlled silicon grains.

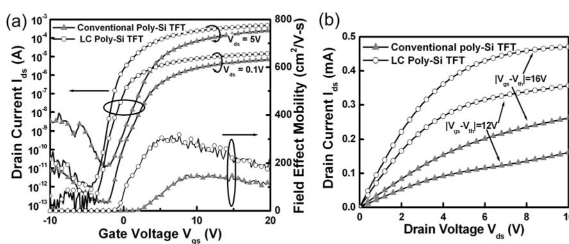

FIG. 4. (a) Transfer and (b) output characteristics of poly-Si TFTs on location-controlled grains and conventional TFTs on random grain structure.

TABLE I. Measured electrical characteristics of poly-Si TFTs with location-controlled (LC) silicon grains and conventional TFTs with random grain structure. The threshold voltage was defined as the gate voltage required to achieve a normalized drain current of $I_{ds}=(W/L)\times10^{-8}$ A at $V_{ds}=0.1$ V. The field-effect mobility and subthreshold swing were extracted at $V_{ds}=0.1$ V, and the I_{on}/I_{off} current ratio was defined at $V_{ds}=5$ V.

TFT structure ($W=L=1.5\ \mu$m)	Threshold voltage (V)	Field-effect Mobility ($\mathrm{cm^2/V\ s}$)	Subthreshold swing (mV/dec)	On/Off current ratio
Conventional	2.4(0.85)	150(41)	875(80)	3.3×10^6
LC grains	−0.8(0.18)	308(22)	390(42)	9.7×10^7

In summary, a crystallization technology for producing two-dimensional lateral grain growth has been developed by excimer laser irradiation relying on spatially temperature distribution at artificial sites. The high quality silicon grains are controlled via manipulating superlateral growth phenomenon by spatially two kinds of silicon films and prepatterned structure. Not only high-performance poly-Si TFTs with field-effect mobility reaching $308\ \mathrm{cm^2/V\ s}$ but also excellent device uniformity are demonstrated owing to the artificially controlled lateral grain growth. Proposed poly-Si TFTs, therefore, have great potential for future SOP and 3D-IC applications.

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