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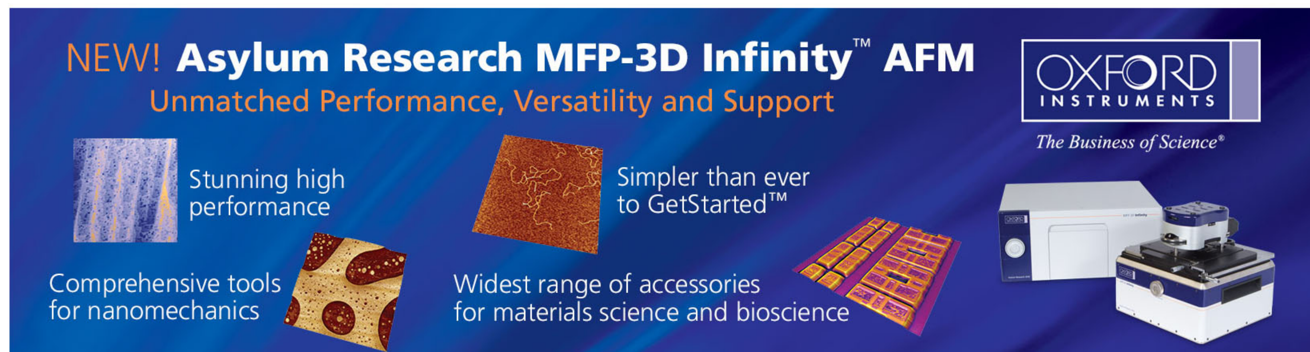

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Nonvolatile $Si/SiO_2/SiN/SiO_2/Si$ type polycrystalline silicon thin-film-transistor memory with nanowire channels for improvement of erasing characteristics

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A silicon-oxide-nitride-oxide-silicon type polycrystalline silicon thin-film transistor (poly-Si TFT) with nanowire channels was investigated for both transistor and memory applications. The poly-Si TFT memory device has superior electrical characteristics, such as higher drain current, smaller threshold voltage, and steeper subthreshold slope. Also, the simulation result on electrical field reveals that the electrical field across the tunnel oxide is enhanced and that across the blocking oxide is reduced at the corner regions. This will lead to the parasitic gate injection activity and the erasing speed can be apparently improved in the memory device due to the pronounced corner effect and narrow channel width. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2798600]

System-on-panel (SOP) display technology with high performance polycrystalline silicon thin-film transistors (poly-Si TFTs) designed as functional devices has rapidly advanced recently.[1,2] The SOP technology primarily focuses on mobile electronics application; thus, low power consumption is required for a long battery life. It is well known that the nonvolatile memory is widely utilized for data storage in portable electronics system due to its properties of low-power consumption and nonvolatility. Compared to conventional nonvolatile memory with floating gate structure, the silicon-oxide-nitride-oxide-silicon (SONOS) type poly-Si TFT memory devices have been proposed for SOP application due to its full process compatibility.[3] A SONOS memory array using Fowler-Nordheim (FN) tunneling for program/erase (P/E) operation has been demonstrated to achieve the low power consumption requirement compared with channel hot electron injection scheme.[4] However, this type of SONOS memory still has several issues on performance, such as insufficient programing/erasing (P/E) efficiency and an undesirable gate injection phenomenon.[5] Recently, various approaches have been proposed to improve the P/E speed and gate injection by using high-k dielectric as a blocking layer.[6,7] The electric field in high-k dielectric is lower than that in the typical SiO_2 film, and thus, it is expected that parasitic gate injection through blocking oxide should be suppressed. In addition, gate engineering methods also proposed by using high work function materials[8,9] to reduce the unwanted charge transport from gate. In this paper, the poly-Si TFT combined with nonvolatile SONOS memory and nanowire channels, called NW SONOS-TFT, is proposed. Not only does the NW device exhibit superior electrical performance for transistor, but it can also suppress the undesirable gate injection and improve the erasing speed for the memory device. The most important is that the fabrication involves no materials replacement, and thereby it is very promising for SOP application in the future.

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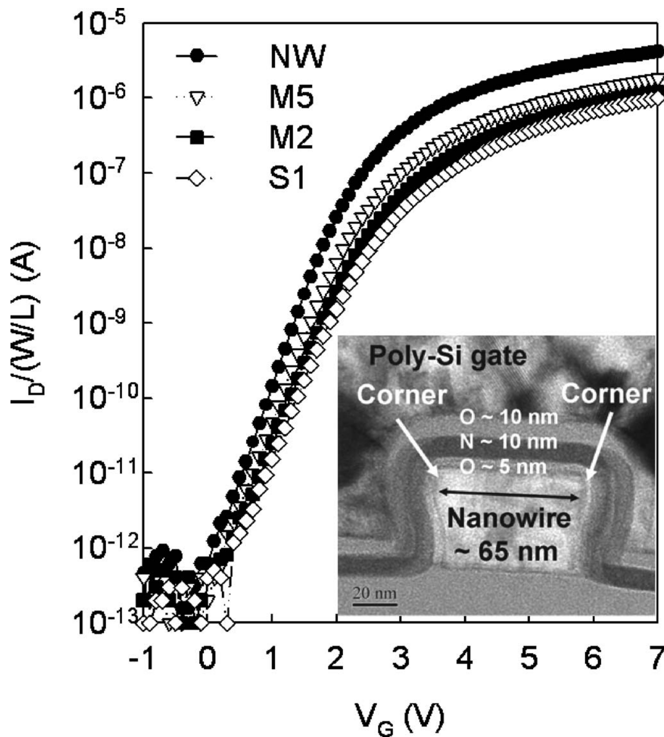

FIG. 1. Comparison of typical I_D-V_G characteristics of the SONOS-TFTs with various structures. The inset exhibits the transmission electron microscopy (TEM) of a single nanowire channel of NW SONOS-TFT.

A 400-nm-thick thermal oxide layer was first grown on the Si wafer by furnace system to replace a glass substrate. Then an undoped 50-nm-thick amorphous silicon (*a*-Si) layer was deposited on the oxidized silicon wafer by low-pressure chemical vapor deposition (LPCVD) at 550 °C. Subsequently, the deposited *a*-Si layer was recrystallized by solid-phase crystallization at 600 °C for 24 h under N_2 ambient. After the patterning of active region with electron beam lithography and dry etching process, the 25-nm-thick oxide-nitride-oxide (ONO) multilayer gate dielectric layers were formed by LPCVD: the 5 nm tunnel oxide (TO), 10 nm silicon nitride (SiN), and 10 nm blocking oxide (BO), sequentially. A 150-nm-thick *in situ* n^+ doped poly-Si layer was then deposited and defined. After S/D formation by self-aligned phosphorous implantation, a 200 nm oxide passivation layer was deposited and contact holes were patterned. Finally, Al metallization was performed and the devices were sintered at 400 °C in nitrogen ambient for 30 min. The studied TFT devices with the same gate length of 5 μm consist of different channels in width, including ten strips of 65 nm nanowire (NW), five strips of 200 nm channels (M5), two strips of 500 nm channels (M2), and a single-channel (S1) with 1 μm.

Figure 1 presents the transfer normalized I_D-V_G curves of SONOS-TFTs with various structures. Obviously, the NW device has superior performance, such as the highest drain current, smallest threshold voltage (V_{th}), and steepest subthreshold swing (SS). The V_{th} decreases from 2.5 V 1.7 V and SS decreases from 0.5 to 0.4 V/decade in order from the S1 structure to the NW structure. Different from the other structures, the nanowire is surrounded by the poly-Si gate to form the trigate structure, shown as the inset TEM photography. The physical width of nanowire channel is confirmed to be 65 nm and the thickness of ONO is 25 nm. Since the

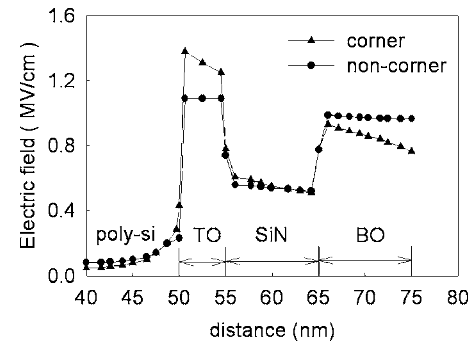

FIG. 2. Simulation of the electrical fields with a gate bias of 2 V in nanowire at corner and noncorner regions.

effective channel width is increased by the trigate structure, the drain current can be improved in NW SONOS-TFT. To study the electrical improvement for the subthreshold behavior, the distribution of electrical field across the stacked gate dielectric of nanowire channel were numerically simulated at a gate bias of 2 V ($\sim V_{th}$) by ISE-TCAD simulator, as shown in Fig. 2. It can be seen that the electrical field near the SiO_2/poly-Si interface at corner region is very high. This will lead the current at the corner region to turn on earlier than that at the noncorner region due to the corner effect induced electrical field. The corner current can provide major current as the device operated in subthreshold region.[10] Thus, the corner effect plays a dominant role to enhance the subthreshold behavior.

The SONOS-TFTs also can act as a nonvolatile memory by using the nitride layer as a charge trapping layer, in addition to transistor application. Figure 3 shows the I_D-V_G curves of device before and after the programing/erasing operations by FN tunneling scheme. The results reveal that the threshold voltage of a fresh memory device is different from those of the memory device after erasing operation. Because the electrons will inject to silicon nitride layer from the control gate via FN tunneling, it is difficult for the SONOS-TFT memory to return to the original state of threshold voltage after performing an erase procedure.

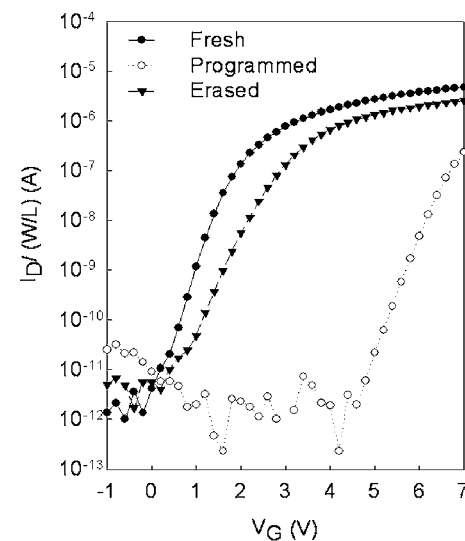

FIG. 3. The I_D-V_G curves of device before memory operation (fresh) and after the programing/erasing operations. The program and erase conditions are 16 V for 100 μs and −18 V for 10 s, respectively.

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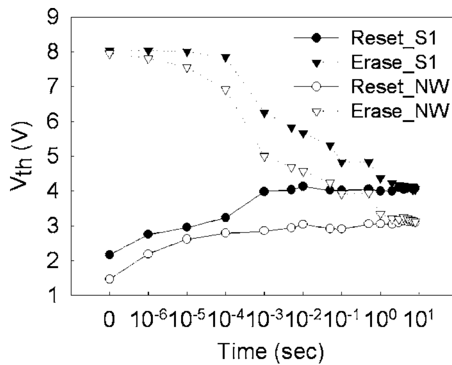

FIG. 4. Self-convergent reset-erase characteristics of S1 and NW devices with a −18 V erasing bias. The devices are both programed with a 18 V gate bias.

Figure 4 presents the self-convergent reset-erase characteristics of the S1 and NW devices. Firstly, the fresh devices were reset by FN mechanism erase with a −18 V to achieve the dynamic balance condition. Next, the devices were programed and then erased with the same negative bias. The results reveal that the self-convergent property is really caused by the balance of electron injection from gate and electron detrapping to substrate. Thus, the reset state V_{th} is determined by the dynamic current balance through the ONO layer. It can be found that the NW device has a smaller reset voltage than that of S1 device. Moreover, the erasing speed is also enhanced in NW structure. Figure 5 shows the threshold voltage shift ($V_{th,reset} - V_{th,fresh}$) before and after the memory operation with various structures. Obviously, the V_{th} shift is almost the same for S1 and M2 devices, and then it decreases as the channel width decreases and corner numbers increase. Due to the pronounced corner effect and narrow channel width, the memory characteristic is dominated by the electrons stored in nitride layer at the corner regions for NW device. Comparing the electrical fields at noncorner region, the electrical field across the tunnel oxide is greatly enhanced and the electric field across the blocking oxide is slightly reduced. The schematic band diagrams across ONO layer are illustrated in the inset. Therefore, the parasitic gate injection and the erasing speed can be improved for NW device due to the corner effect.

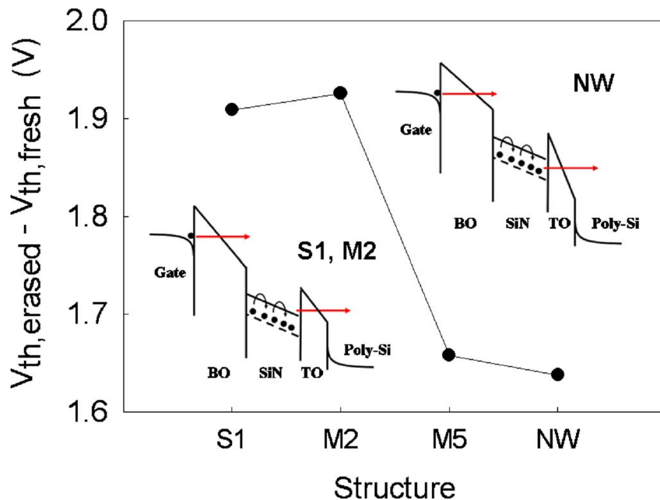

FIG. 5. Threshold voltage shift ($V_{th,reset} - V_{th,fresh}$) vs different structures. The insets exhibit the schematic band diagrams at corner (for NW structure) and noncorner (for S1, M2 structures) regions.

In conclusion, we have demonstrated the SONOS type poly-Si TFT memory with nanowire channels. Since the effective channel width is increased by trigate structure and the subthreshold behavior is improved by additional corner current, the NW device has superior transistor performance than other devices. As the devices operated for memory mode by using FN tunneling mechanism, the self-convergent characteristics reveal the undesirable gate injection and inefficient erase speed can be improved apparently from S1 to NW structure. According to the simulated results, the improvement for the transistor and memory with nanowire structure is mainly contributed to the pronounced corner effect. Although the NW devices cannot be easily fabricated using panel maker's existing manufacturing facilities at present time, it is still a very promising technology because of no material replacement.

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