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Statistical variability in FinFET devices with intrinsic parameter fluctuations

Chih-Hong Hwang [a], Yiming Li [a,b,*], Ming-Hung Han [a]

[a] Department of Electrical Engineering and Institute of Communications Engineering, National Chiao Tung University, 1001 Ta-Hsueh Road, Hsinchu 300, Taiwan
[b] National Nano Device Laboratories, Hsinchu 300, Taiwan

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ABSTRACT

High-κ/metal-gate and vertical channel transistors are well-known solutions to continue the device scaling. This work extensively estimates the influences of the intrinsic parameter fluctuations on nanoscale fin-type field-effect-transistors and circuits by using an experimentally validated three-dimensional device and coupled device-circuit simulations. The dominance fluctuation source in threshold voltage, gate capacitance, cut-off frequency, delay time, and power has been found. The emerging fluctuation source, workfunction fluctuation, shows significant impacts on DC characteristics; however, can be ignored in AC characteristics due to the screening effect of the inversion layer.

1. Introduction

In nano-device-circuits and systems, the device variability is pronounced and becomes crucial for circuit design [1–9]. The most well-known fluctuation sources on transistors are the random-dopant-fluctuation (RDF) and process-variation-effect (PVE) [4,6,7]. The RDF comes from the manufacturing process, such as ion implantation, thermal annealing and so on. Fluctuations of device characteristics including are caused both by a fluctuation in the number of dopants and the particular random distribution of dopants in the channel region [7]. The inevitable variations of processing conditions, such as the resolution limit of lithography and the grainy nature of photo resist and gate, also impact the device dimensions. The gate length deviation and the line edge roughness are the dominating factors in PVE [4,6,7]. To suppress the impact of these variations, fin-type field-effect-transistors (FinFETs) [10–12] and high-κ/metal-gate technology [13] are promising. However, the use of metal as gate material may introduce another source of fluctuation, workfunction fluctuation (WKF). The grain orientation of metal is uncontrollable during growth period [14]; therefore, the device threshold voltage (V_{th}) will become a probabilistic distribution rather than a deterministic value. Approach has been noticed the workfunction fluctuation (WKF); unfortunately, only the device V_{th} fluctuation was concerned and the scope is limited to the planar transistors [14,15].

In studying the fluctuation of FinFETs, diverse approaches have recently been presented [10–12]; however, the attention is most drawn to the existence of RDF and PVE on transistors. A comprehensive understanding of these fluctuations including WKF on FinFETs and circuits is lacked. Therefore, this study explores the intrinsic device parameter fluctuations (WKF, PVE, and RDF) on 16-nm-gate silicon-on-insulator (SOI) FinFETs and digital circuits by an experimentally validated three-dimensional coupled device-circuit simulation technique [8,9]. The major variability sources in device's DC/AC and circuit's timing/power characteristics are explored for the first time. The vast study assesses the fluctuation on digital circuit performance and reliability, which can be in turn used to optimize nanoscale devices and circuits.

2. Simulation technique

Fig. 1a illustrates the explored 16-nm-gate SOI FinFETs with amorphous-based TiN/HfSiON gate stacks with an EOT of 1.2 nm [14]. The equivalent channel doping concentration is $1.48 \times 10^{18}\,cm^{-3}$. Fig. 1b–d illustrates the RDF-induced fluctuation, the simulation mainly follows our recent work [7–9]. The PVE-induced fluctuation is examined by V_{th} roll-off characteristics, as shown in Fig. 1e [7]. The physical models and accuracy of such large-scale simulation approach have been quantitatively calibrated by experimentally measured results [7,10]. For WKF in Fig. 1f, a Monte-Carlo approach is proposed for examining such effect, as shown in Fig. 1g. Based on the average grain size, 4 nm [14,15], the gate area is first partitioned into several parts. Then, the workfunction of each partitioned area (WK_i) is randomized following the properties of metal in Fig. 1h [14,15]. The effective device workfunction is then obtained and used for estimation of WKF-induced fluctuations. Fig. 1i is the explored inverter circuit, in which a coupled device-circuit simulation approach [8,9] is employed to ensure the best accuracy. Notably, the device dimension and V_{th} of both *n*-type and *p*-type transistors are the same to compare them on the same basis.

* Corresponding author. Address: Department of Electrical Engineering, National Chiao Tung University, 1001 Ta-Hsueh Road, Hsinchu 300, Taiwan. Tel.: +886 35712121x52974.
E-mail address: ymli@faculty.nctu.edu.tw (Y. Li).

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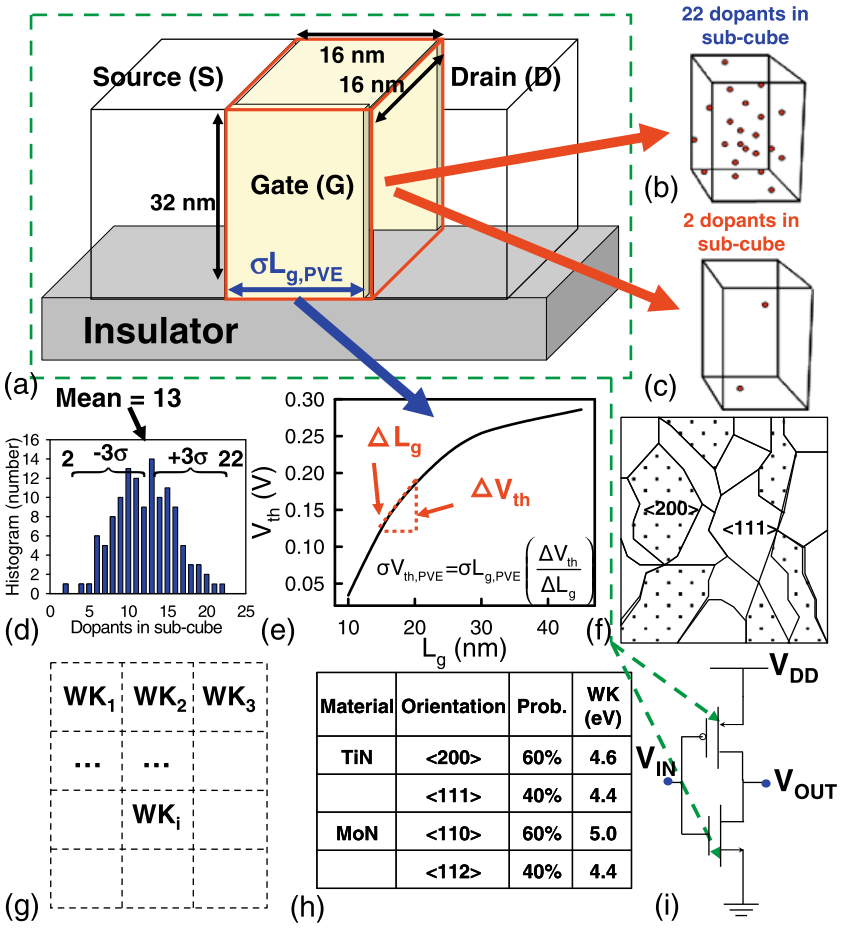

Fig. 1. (a) The explore SOI FinFET with RDF effect. The number of channel dopants in device may vary from 2 to 22, and the average number is 13(b–d). (e) The V_{th} roll-off characteristics for estimating PVE. (f) Metal-gate surface morphology. (g) In estimation of WKF, the gate area is partitioned into several pieces according to the average grain size. The workfunction of each partitioned area (WK_i) is a random value, whose probability follows (h). (i) The tested inverter circuit.

3. Results and discussion

Fig. 2a and b displays the components of σV_{th} for *n*-type and *p*-type planar MOSFETs and FinFETs, respectively. The total σV_{th}, $\sigma V_{th,total}$, are obtained from the statistical addition as shown in below:

$$(\sigma V_{th,total})^2 - (\sigma V_{th,PVE})^2 + (\sigma V_{th,WKF})^2 + (\sigma V_{th,RDF})^2 \quad (1)$$

The σVth,PVE, σVth,WKF, and σVth,RDF are the PVE-, WKF-, and RDF-induced σVth, respectively. The FinFET shows a significantly smaller σVth than the planar MOSFET due to its better channel controllability [10]. The RDF and WKF dominate the σVth in both n-type and p-type transistors. The σVth,WKF in p-type FinFETs becomes comparable to σVth,RDF due to the large deviation of workfunction. In Fig. 1h, the probability for the used material TiN (for NMOS) and MoN (for PMOS) are the same; however, the differences of workfunction in different grain orientation are quite different. The large deviation of workfunction in MoN enlarges the σVth,WKF of p-type FinFETs and makes the σVth,total of p-type FinFETs larger than the n-type FinFETs. Notably, the simulation result is still valid for lightly-doped transistors, in which the lightly-doped channel is employed for the suppression of RDF. With similar simulation methodology, the WKF possesses over 95% Vth fluctuation of σVth,total, which shows the significance of controlling WKF. Fig. 3 summarizes the gate capacitance fluctuations (σCg) with 0 V, 0.5 V and 1.0 V gate bias. Different to the results of Vth fluctuation, the WKF brought less impact on gate capacitance fluctuation. At low gate bias or negative gate bias, the accumulation layer screens the impact of WKF. Additionally, at low gate bias, the total capacitance decreases because of an increased depletion

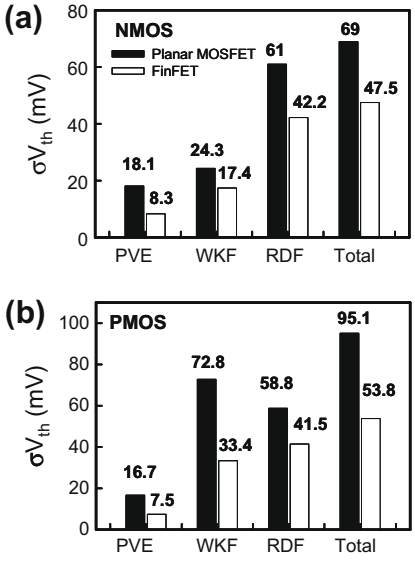

Fig. 2. The components of σV_{th} for (a) *n*-type and (b) *p*-type planar MSOFETs and SOI FinFETs.

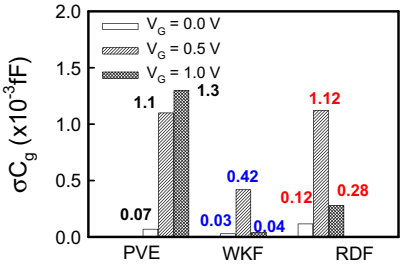

Fig. 3. The C_g fluctuation at $V_G = 0$, 0.5, and 1 V for 16-nm-gate FinFETs with intrinsic parameter fluctuations, WKF, PVE, and RDF.

region. The associated Cg fluctuation is small. As the VG increases, the inversion layer formed and the Cg is now given by the change of inversion charge with respect to surface potential. Therefore, the σCg becomes significant due to the intrinsic-parameter-fluctuated electrostatic potentials. If the high VG is achieved, the inversion layer is formed below the surface of the gate oxide and the total gate capacitance is mostly contributed by the gate oxide capacitance (Cox). Therefore, the variation of capacitance now again becomes the variation of capacitance of gate oxide (Cox). Under strong inversion, the gate capacitance is dominated by the inversion layer and a small change resulting from the WKF in the voltage across the MOS structure will induce a differential change in the inversion layer charge density. The WKF is therefore bringing less impact on the gate capacitance fluctuation because the inversion charge responds to the change in capacitor voltage (i.e., the WKF is now screened by the inversion layer). Similarly, in RDF, the impact of the individual dopants induced electrostatic potential variation is screened by the inversion layer itself. However, the screening effect of inversion layer is weakened by discrete dopants positioned near the channel surface. Therefore, the gate capacitance fluctuation is still obviously fluctuated at high gate bias. The results of this study show that the RDF and PVE dominate the gate capacitance fluctuations at all gate bias conditions, respectively. The impact of the WKF on Cg is reduced significantly at low and high gate voltage (VG) due to the screening effect. Notably, the PVE brings direct impact on gate length and therefore influences the gate capacitance. The PVE-induced gate capacitance fluctuation is independent of screening effect and should be noticed when the transistor operated in high gate bias.

Fig. 4a–c describes PVE-, WKF-, and RDF-induced the cuts-off frequency (FT = vsat/2πLg = gm/2πCg) characteristic fluctuation for the n-type transistors. gm, Cg and vsat are the transconductance, gate capacitance, and the saturation velocity, respectively. The solid lines are the nominal case; the dashed lines are the cases with intrinsic parameter fluctuation; the symbol lines are the averaged result. In Fig. 4b, the WKF-induced σFT diminished as the saturation of the carrier velocity occurs due to the screening effect of inversion layer of device, which screens the variation of surface electrostatic potential. The σFT then becomes significant at high-field because of the carrier scattering. The PVE-induced σFT, as plotted in Fig. 4a, is significant at high-field owing to the change of gate length. As for the RDF-induced σFT in Fig. 4c, the σFT does not diminish when the saturation of the carrier velocity occurs due to the randomness of carrier-impurity scattering events and carrier velocity variations. Similar to WKF, the screening effect also decreases the RDF-induced fluctuation; however, the screening effect may be broken by discrete dopant positioned near the channel surface. Notably, the nominal and the averaged values of FT are similar for the results of PVE and WKF. However, in RDF, the difference of the nominal and the averaged FT becomes significant as VG increases. The inset plots of Fig. 4c are the distribution of electron velocity for the nominal and the RDF-fluctuated cases. The discrete channel dopants induced a relatively negative potential in channel and then twisted the electric field nearby. The distribution of electron velocity is thus altered; therefore increases the vsat and averaged FT. The σFT is summarized in Fig. 4d, in which the RDF and PVE dominate the σFT. Different to the results of σVth, the WKF brought less impact on the AC characteristics.

Fig. 5a shows the normalized high-to-low delay time (t_{HL}) and low-to-high delay time (t_{LH}) fluctuations. The nominal values of delay time are shown in insets. The normalized fluctuation is the ratio of the standard deviation to the nominal value. The t_{HL} and t_{LH} dependent on the V_{th} for *n*-type and *p*-type transistors, respectively; therefore, the trend of σt_{HL} and σt_{LH} follow the trend of σV_{th}

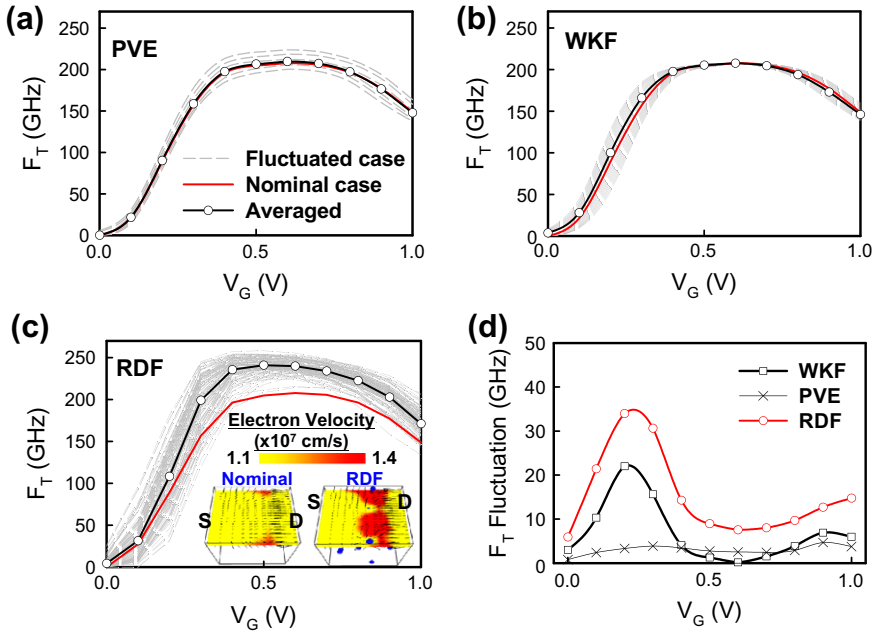

Fig. 4. The σF_T induced by (a) PVE, (b) WKF, and (c) RDF. (d) The summarized σF_T for the studied SOI FinFETs. The inset plots are nominal and RDF-fluctuated electron velocity.

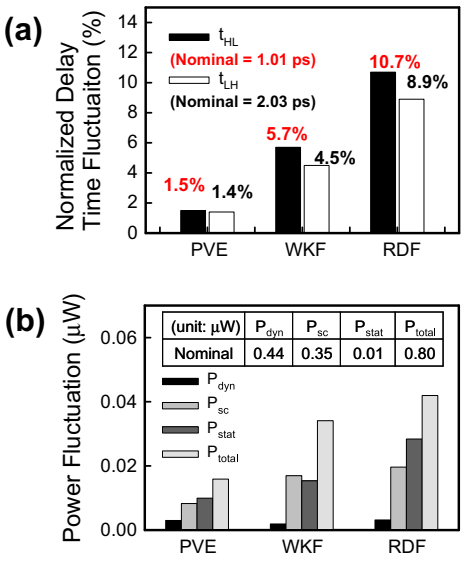

Fig. 5. (a) The normalized high-to-low and low-to-high delay time fluctuations for the explored circuits with WKF, PVE, and RDF. (b) The fluctuations of dynamic power, short-circuit power, static power, and total power, where the inset shows the nominal power.

for *n*-type and *p*-type transistors [9]. The major fluctuation source for timing characteristics are RDF and WKF. The overall normalized σt_{HL} and σt_{LH} of SOI FinFETs inverter are 12.3% and 10.1%, respectively, which are significant smaller than that of planar MOSFETs in our previous work (σt_{HL}:21.0% and σt_{LH}:20.5%) [9]. Fig. 5b estimates the power fluctuations for the studied FinFET inverters and the inset shows the nominal value of power. The total power (P_{total}) is consisting of the dynamic power ($P_{dyn} = C_{load}V_{DD}^2 f_{0->1}$), the short-circuit power ($P_{sc} = f_{0->1}V_{DD} \times \int I_{sc}(\tau)d\tau$), the static power ($P_{stat} = V_{DD} \times I_{leakage}$). The $f_{0->1}$ is the clock rate. I_{sc} is the short-circuit current. T is the switching period. $I_{leakage}$ is the leakage current. The P_{dyn} and P_{sc} are the two significant factors in total power consumption. In fluctuations of dynamic power (σP_{dyn}), the RDF and PVE dominate the dynamic power fluctuation. The WKF shows less impact due to the smaller AC fluctuation. Since the short-circuit power is defined by the time of existence of DC path between the power rails and the short-circuit current, the σP_{sc} depends on the σV_{th} of *n*-type and *p*-type FinFETs. The RDF and WKF thus dominate the σP_{sc}. The WKF plays a more important role than PVE in σP_{sc} because of the larger σV_{th} induced by workfunction difference. The static power fluctuation (σP_{stat}) is the most significant fluctuation source in power. The leakage current is an exponential function of V_{th} ($I_{leakage} \sim \exp(-qV_{th}/nkT)$); therefore, the σP_{stat} becomes significant even though the static power is not an important part in total power dissipation. The dominating fluctuation source in σV_{th} also implies the dominant sources of fluctuation, RDF and WKF. The total power fluctuation (σP_{total}) is obtained from $[(\sigma P_{PVE})^2 + (\sigma P_{WKF})^2 + (\sigma P_{RDF})^2]^{0.5}$. The statistic addition of individual fluctuation sources simplifies the variability analysis of nano-devices and circuits, significantly [6]. The σP_{total} is 0.042 μW, which is 5.2% ($\sigma P_{total}/P_{total} = 0.042/0.8$) of the total power. The power fluctuation may bring impacts on the reliability of circuits, such as temperature and in turn degrades the performance of devices and circuits.

4. Conclusions

This study explores the metal-gate device DC/AC variability and correspondent circuit's delay and power fluctuations. The dominant variability source in circuits has been studied. The RDF and WKF dominate σV_{th} for *n*-type and *p*-type FinFETs and therefore rule the σt_{HL} and σt_{LH} of the explored digital circuits. The overall normalized σt_{HL}, σt_{LH} and σP_{total} of SOI FinFETs inverter are 12.3%, 10.1%, and 5.2%, respectively. As for the device AC characteristics, the PVE and RDF are the major sources of fluctuation. The influence of the emerging fluctuation source, WKF, is negligible due to the screening effect of inversion layer. We are currently studying the fluctuations of lightly-doped FinFETs and the effects of fin aspect ratio and associated round-top fin structure on FinFETs and circuits.

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