經由非線性分析與功率消耗分析求致 Sigma-Delta Modulator ADC 之設計最佳化

計劃編號: 96-2221-E-009-225-MY3
計劃主持人: 陳福川
計劃執行單位: 交通大學 電控系

摘要

在第一年計畫中,我們的主要目標是經由非線性的分析去獲得非線性失真模型,爲了考慮到非線性的對於積分三角數位類比轉換器的影響,我們分析了關鍵幾個主要在積分三角數位類比轉換器中的非線性失真來源,也建立了其相關的非線性失真模型,也爲了達到在不同規格下可以獲得精確的電路功率消耗,在這篇論文中,也提供了精確的離散時間積分三角數位類比轉換器的功率消耗模型,在最後最佳化的過程中我們導入了非線性失真模型,功率消耗模型和雜訊功率模型,綜合了三個模型我們將可以設計出最佳化的設計規格以在最小的功率消耗下達成設計者所需要的 SNDR 解析度.

Abstract

During the first year of the project, our main goal is in deriving the distortion models caused by nonlinearity. In order to consider the nonlinear influences in ΣΔ modulator, this report provides the discussions about several dominating nonlinear sources in ΣΔ modulator, and built their distortion power models. In order to obtain the accurate power consumptions for different specifications, this report offers a model to estimate power consumption for discrete-time single-loop ΣΔ modulator. By integrating the distortion power forms, accurate power consumption models and the noise power models into the optimization work, these optimal design specifications can make the performance of ΣΔ modulator achieve the required *SNDR* while minimizing power consumption.

Keywords *: ADC, Sigma Delta modulator, SDM*

I. INTRODUCTION

ΣΔ ADC is very popular for many applications, and in order to decrease the time-cost for practical circuit design, it's important to know the circuit specifications before circuit design. There is so many issues and software which offer the synthesis environments to obtain the optimal specifications [2-5]. In general, the synthesis ways for ΣΔ modulator can be categorized mainly as that first. transistor-level simulation synthesis second, macromodel-simulation synthesis and third behavioral-simulation synthesis. The transistor-level synthesis has a highest accuracy, but it's too slow to allow efficient performance space exploration. Behavior- simulation synthesis has a better speed and acceptable accuracy, so this synthesis method is often employed by designers. Our proposed optimization method not only has acceptable accurate, but also faster than Behavior-simulation synthesis. [1] built the dominating noise power forms and obtained the optimal specifications for the required *SNR* . In addition to the noise power forms in [1], this paper involved the dominating nonlinear distortion power forms into optimization since low-distortion is an important factor in many applications of analog-to-digital conversion; for instance, HDTV(High Definition Television), STB(Set-Top Box) and high- quality digital camera, etc.

The dominated discussion about nonlinear distortion sources and accurate power consumption model are presented in section Ⅱ and section Ⅲ respectively. Conclusion is presented in section Ⅳ.

II. NONLINEAR DISTORTION MODELS

The nonlinear distortions in ΣΔ modulator are categorized into six parts in this section, there are four kinds of distortions related to integrators, which are settling distortion, nonlinear finite OTA gain distortion, nonlinear capacitance distortion and nonlinear switch- resistance distortion. Besides the above nonlinearities, DAC distortion and quantization distortion are discussed in this section. Although there are so many distortion sources in ΣΔ modulator, fortunately, due to the developments of process techniques and circuit design, so we only consider the nonlinearities of settling distortion, nonlinear finite OTA gain

distortion and DAC distortion in the optimization job, and the relative techniques are introduced after.

A. Settling Distortion

Settling distortion is the sole distortion which can be significantly affected by op-amp slew rate (*SR*) and gain-bandwidth (*GBW*). There was a great effort in [9] to model settling distortion. However the result in [9] reached a wrong conclusion, and it showed little insight about how *SR* and *GBW* are quantitatively related to settling distortion. Consider the integrator operates in the integration phase, there are two settling conditions depending on the absolute value of V_S.

1. Linear settling $\left(|V_S| < \frac{1}{a_1} \cdot SR \cdot \tau_2\right)$

We can represent integrator output voltage during the *n*th integration interval as

$$V_o(t) = V_o(nT-T) + a_1 V_S\left(1 - e^{\frac{-(t-nT+\frac{T}{2})}{\tau_2}}\right), nT - \frac{T}{2} < t < nT \quad (1)$$

where a_1 is the gain of the first stage integrator. V_S is the difference between feedback and input signal. T is the sampling period. τ_2 is the time constant in the integration phase [1].

2. Partial slewing $\left(\frac{1}{a_1} \cdot SR \cdot \tau_2 < |V_S|\right)$

$$V_o(t) = V_o(nT-T) + SR \cdot (t_0 - nT + \frac{T}{2}) + \left[a_1 V_S - SR \cdot (t_0 - nT + \frac{T}{2})\right]\left(1 - e^{\frac{-(t-t_0)}{\tau_2}}\right), \quad t > t_0 \quad (2)$$

where t_0 is the time instant when V_o rate becomes less than *SR*. The full slewing case is not considered here because it is not significant. Note that (1) and (2) at end of each integration interval can be rewritten as

$$V_O(nT) = V_O(nT-T) + a_1 V_S(1 - \beta \cdot e)\,), |V_S| \le V_L$$
$$V_O(nT) = V_O(nT-T) + a_1 V_S\left[1 - \frac{V_L}{V_S} \cdot \beta e^{|V_S|/V_L}\right], |V_S| > V_L \quad (3)$$

where $\beta = e^{-(T/(2\tau_2)+1)}$ and $V_L = SR\tau_2 / a_1$.

Let

$$g_i(V_S) = \begin{cases} a_1(1-\beta e) \ ; & |V_S| \le V_L \\ a_1\left(1 - \frac{V_L}{V_S}\beta e^{|V_S|/V_L}\right) \ ; & |V_S| > V_L \end{cases} \quad (4)$$

which is the integrator gain. Assume that $g_i(v)$ can be approximated by

$$p(v) = a_1 \cdot (\alpha_1 + \alpha_3 v^2 + \alpha_5 v^4) \quad (5)$$

we further analyze the 3rd and 5th harmonic powers as follows:

$$HD3_{Settling}(dB) = 20\log\left(\frac{1}{\sqrt{2}}\left(\frac{|\alpha_3| A_{VS}^3}{4}\right)\right)$$
$$= 20\log|\alpha_3| - 60\log OSR + 30.095 \quad (6)$$
$$HD5_{Settling}(dB) = 20\log|\alpha_5| - 100\log OSR + 48.15$$

From (6) we can see that *OSR* can effectively influence settling harmonic powers. The (7) reveals that α_3 and α_5 are functions of *T*, *GBW*, *R*, C_S and *SR*.

OSR	HD3(dB)	*SR* ($V/\mu s$)	*GBW* (MHz)
8	$20\log\|\alpha_3\|$ -24	≥ 500	≥ 380
16	$20\log\|\alpha_3\|$ -42	≥ 200	≥ 180
32	$20\log\|\alpha_3\|$ -60	≥ 120	≥ 70
50	$20\log\|\alpha_3\|$ -72	≥ 110	≥ 60
64	$20\log\|\alpha_3\|$ -78	≥ 100	≥ 50
96	$20\log\|\alpha_3\|$ -89	≥ 90	≥ 40

Table Ⅰ Minimum *SR* and *GBW* required w. r. t. *OSR*

B. Nonlinear Finite OTA Gain Distortion

An ideal OTA with infinite gain doesn't introduce any noise or distortion. Practical OTAs not only have the characteristics of finite DC gain, but also the gain is nonlinear.

A typical OTA's configuration schematic considering nonlinear DC gain. In this figure R_{out} of the output-stage transistors are functions of output voltage V_o. Hence, the nonlinearity of the gain is manifested by its dependency on amplifier output voltage V_o. This nonlinear gain introduces error components as distortions in the ΣΔ modulator output spectrum.

In order to model the nonlinear DC gain A_V, we tried various combination of A_o and V_{OS} to create a set of representative curves for the family of nonlinear DC gain curves. It trying to obtain a model for the family of nonlinear curves, we focus on OTAs under the 0.18μm process. The model we arrive at is of the form

$$A_V(V_o) = A_0(1 + q_2 V_o^2 + q_4 V_o^4)$$

$$q_2 = -\frac{1}{2} \cdot (0.443 \cdot \frac{A_0^{0.03}}{V_{os}^{1.2}})^2 \quad (7)$$

$$q_4 = -\frac{1}{24} \cdot (0.443 \cdot \frac{A_0^{0.03}}{V_{os}^{1.2}})^4 \quad (8)$$

The next work is to obtain the expressions to estimate harmonic distortions introduced by integrators with a nonlinear-finite-DC-gain OTA.

The final expression can be derived as

$$V_o^+ - V_o^- \cong \frac{C_S}{C_I}\cdot\{1+\frac{q_2}{A_0}[(V_o^+)^2+(V_o^-)^2+V_o^+V_o^-]$$
$$+\frac{q_4}{A_0}[(V_o^+)^4+(V_o^+)^3V_o^-+(V_o^+)^2(V_o^-)^2$$
$$+V_o^+(V_o^-)^3+(V_o^-)^4]\}\cdot V_S \qquad (9)$$

In (9) the nonlinear term is

$$\frac{C_S}{C_I}\cdot[\frac{q_2}{A_0}((V_o^+)^2+(V_o^-)^2+V_o^+V_o^-)+\frac{q_4}{A_0}((V_o^+)^4+(V_o^+)^3V_o^-$$
$$+(V_o^+)^2(V_o^-)^2+V_o^+(v_o^-)^3+(V_o^-)^4)]\cdot V_s \qquad (10)$$

In order to build a mathematical expression related to input signal magnitude for estimating the distortion caused by nonlinear OTA gain, $V_o^{\pm}$ and V_S must be expressed as functions of A_{in}. In single-loop second-order ΣΔ modulator, when a signal $Sin(wnT)$ apply to modulator input and quantization noise is not considered, V_S can be represented as

$$V_S(nT) = A_{in}\sin(wnT) - A_{in}\sin(w(n-2)T)$$
$$= A_{in}[(1-\cos(\frac{2\pi}{OSR}))\cdot\sin(wnT)$$
$$-\sin(\frac{2\pi}{OSR})\cdot\cos(wnT)] \qquad (11)$$

The output signal of the first integrator can be represented as [11]

$$V_o^{\pm} = A_{in}\sin(w(n\pm\frac{1}{2})T)$$
$$\cong A_{in}\left[\sin(wnT)\pm\sin(\frac{\pi}{2\cdot OSR})\cdot\cos(wnT)\right] \qquad (12)$$

Substituting (11) and (12) into (10), the harmonic distortion formulas are

$$HD3_{NFDCG} = A_{HD3\_1}\sin(3wnT)+A_{HD3\_2}\cos(3wnT) \quad (13)$$
$$HD5_{NFDCG} = A_{HD5\_1}\sin(5wnT)+A_{HD5\_2}\cos(5wnT) \quad (14)$$

$A_0 = 55.1dB$ $V_{OS} = 1V$	Theoretic (dB)	SIMULINK (dB)
Ain = 0.2V OSR = 24	$HD3_{NFDCG}$ = -137.1	$HD3_{NFDCG}$ = -139.2
Ain = 0.2V OSR = 60	$HD3_{NFDCG}$ = -145	$HD3_{NFDCG}$ = -148
Ain = 0.2V OSR = 100	$HD3_{NFDCG}$ = -149.5	$HD3_{NFDCG}$ = -152.1
Ain = 0.5V OSR = 24	$HD3_{NFDCG}$ = -113.2 $HD5_{NFDCG\_A}$ = -165.3 $HD5_{NFDCG\_B}$ = -143.1	$HD3_{NFDCG}$ = -115 $HD5_{NFDCG}$ = -147.7
Ain = 0.5V OSR = 60	$HD3_{NFDCG}$ = -121.2 $HD5_{NFDCG\_A}$ = -173.2 $HD5_{NFDCG\_B}$ = -151	$HD3_{NFDCG}$ = -123.6 $HD5_{NFDCG}$ = -156
Ain = 0.5V OSR = 100	$HD3_{NFDCG}$ = -125.6	$HD3_{NFDCG}$ = -127.1
	$HD5_{NFDCG\_A}$ = -177.6 $HD5_{NFDCG\_B}$ = -155.9	$HD5_{NFDCG}$ = -158

TABLE Ⅱ. Estimation results of theory and behavior simulation

where

$$A_{HD3\_1} = \frac{C_S}{C_I}\{-\frac{3\cdot q_2\cdot A_{in}^3}{4\cdot A_0}[1-\cos(\frac{2\pi}{OSR})]$$
$$+q4\cdot A_{in}^5[-\frac{5}{16}(1-\cos(\frac{2\pi}{OSR}))$$
$$-\frac{1}{8}\sin^2(\frac{\pi}{OSR})\cdot(1-\cos(\frac{2\pi}{OSR}))]\}$$

$$A_{HD3\_2} = \frac{C_S}{C_I}\{-\frac{3\cdot q_2\cdot A_{in}^3}{4\cdot A_0}\sin(\frac{2\pi}{OSR})$$
$$+q4\cdot\sin(\frac{2\pi}{OSR})\cdot A_{in}^5[-\frac{5}{4}$$
$$+\frac{5}{16}\sin(\frac{2\pi}{OSR})+\frac{1}{8}\sin^2(\frac{\pi}{OSR})]\}$$
$$A_{HD5\_1} = \frac{C_S}{C_I}\cdot\frac{q_4\cdot A_{in}^5}{A_0}[\frac{5}{16}+\frac{1}{8}\cdot\sin^2(\frac{\pi}{2\cdot OSR})$$
$$\cdot(1-\cos(\frac{2\pi}{OSR}))]$$
$$A_{HD5\_2} = \frac{C_S}{C_I}\cdot\frac{q_4\cdot A_{in}^5}{A_0}[\frac{5}{16}+\frac{1}{8}\cdot\sin^2(\frac{\pi}{2\cdot OSR})$$
$$\cdot\sin(\frac{2\pi}{OSR})] \qquad (15)$$

The power of the 3rd and 5th harmonic distortions are

$$HD3_{NFDCG}(dB) = 10\log\frac{(A_{HD3\_1}{}^2 + A_{HD3\_2}{}^2)}{2}$$
$$HD5_{NFDCG}(dB) = 10\log\frac{(A_{HD5\_1}{}^2 + A_{HD5\_2}{}^2)}{2} \qquad (16)$$

Using behavior simulation for two cases to verify the above distortion models, the simulation based on a second-order ΣΔ ADC with input bandwidth 0.1 MHz, $A_0 = 55.1$ dB and $V_{OS} = 1V$. The simulation results are listed in TABLE Ⅱ. In the table, $HD3_{NFDCG}$ represents

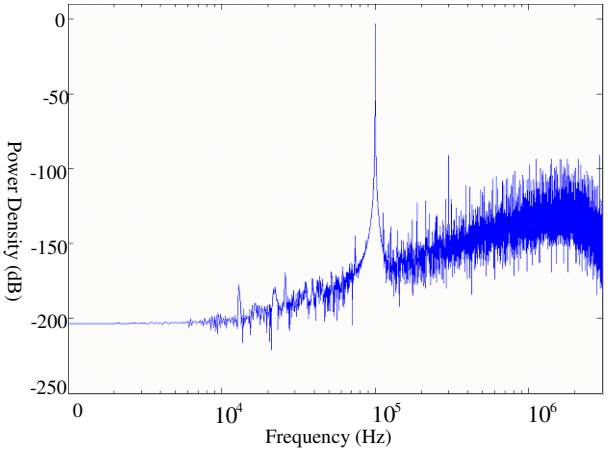

Fig. 1. Output spectrum of a second-order ΣΔ modulator with harmonic distortion

the power of the 3rd harmonic distortion, $HD5_{NFDCG\_A}$ and $HD5_{NFDCG\_B}$ represent the powers of the 5th harmonic distortions, $HD5_{NFDCG\_A}$ employ (7) and (8) to estimate q_2 and q_4, the original nonlinear coefficients q_2 and q_4 are employed in $HD5_{NFDCG\_B}$. The two tables show that $HD5_{NFDCG\_A}$ and simulation results for SIMULINK are not close, because it is (8) difficultly approach to q_4 closely. It is clearly observe that $HD5_{NFDCG\_B}$ and simulation results for SIMULINK are closer. Although $HD5_{NFDCG\_A}$ is not accurate, the power of HD5 can be neglected since it is too small and usually covered by noise floor. Fig. 1 shows the simulation results based on A_0=52.7dB, V_{OS}=1.38V, *OSR*=16 and $A_{in}=0.7$V. In TABLE Ⅱ, $HD5_{NFDCG}$ is too small and covered by noise floor when A_{in}=0.2V.

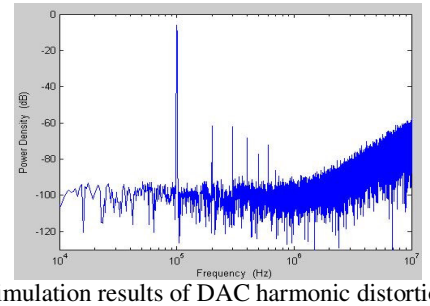

Fig. 2 Simulation results of DAC harmonic distortion

C. *Multi-bit DAC Distortion*

Any noise or distortion in the DAC response will directly appear at the output without benefiting from loop shaping. Since DAC distortion is related to component mismatch which is random in nature, the purpose of this subsection is to create a model to estimate average distortion power once the random property in component mismatch is determined.

Expressing the harmonics powers as their expected values, one obtains

$$E[HD2_{DAC}] \cong 20\log\Delta_{cap}\cdot\left|-0.125a^2A_{in}^2 + 0.010415a^4A_{in}^4 - 0.0003255a^6A_{in}^6\right|$$

$$E[HD3_{DAC}] \cong 20\log\Delta_{cap}\cdot\left|-0.02083a^3A_{in}^3 + 0.00130208a^5A_{in}^5\right|$$

$$E[HD4_{DAC}] \cong 20\log\Delta_{cap}\cdot\left|0.002604a^4A_{in}^4 - 0.00013021a^6A_{in}^6\right|$$

Simulation sees as Fig.2

D. *Quantization Distortion*

The quantization operation is inherently nonlinear because the quantizer error is determined from the quantizer input signal. For convenience, we usually model the quantizer as a linear model and approximate the quantization noise as a white noise. This approximation is made when the quantization error has the following properties, which we refer to collectively as the "input-independent additive white noise approximation" [15]:

Property 1. ε_n is statistically independent of the input signal or ε_n is uncorrelated with the input signal.

Property 2. ε_n is uniformly distributed in $[-\Delta/2, \Delta/2]$.

Property 3. ε_n is an independent identically distributed

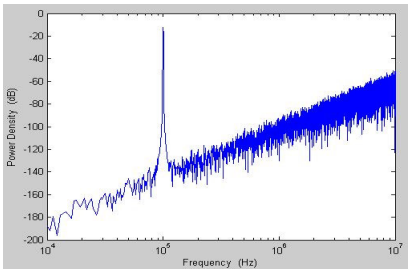

Fig. 3. PSD of second-order ΣΔ modulator with 5 quantization levels

sequence or ε_n has a flat power spectral density. where ε_n is the error sequence and Δ is the distance between output levels. Therefore, the quantization error from ΣΔ modulators is typically not white.

For dc, inputs the quantization error is periodic, generating idle channel tones or pattern noise. For

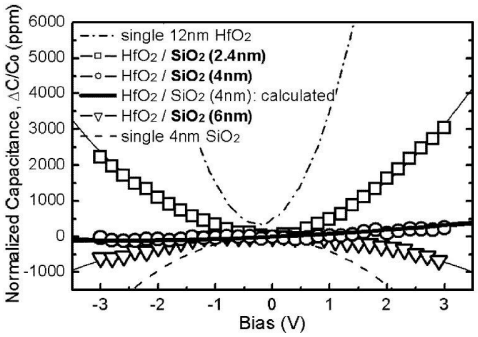

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Fig. 16. Normalized C-V curves (△C/C) of MIM capacitors with single $HfO_2(12nm)$, single $SiO_2(4nm)$ and HfO_2/SiO_2 stack.

inputs, the quantization error is also periodic, containing components harmonically related to the input frequency and amplitude. One can view this effect as a time-domain distortion and therefore argue that the converter actually has less resolution than rms measurements. From the properties described above, one can see that multi-bit quantizers are closer to the linear model than single-bit ones and the time-domain distortions of multi-bit quantizers can be ignored, as shown in Fig. 3. From Fig. 3, we can see that the quantization noise is almost white and harmonic distortion is unapparent, hence only the quantization noise is involved in final optimization.

E. Nonlinear Capacitance Distortion

Recently metal-insulator-metal(MIM) capacitor structure is the most popular capacitor fabrication in integrated circuits, which are widely used in analog, mixed-signal and RF circuits [16]. Due to MIM capacitors in integrate circuits occupy a large portion of chip area, hence the high-K dielectrics into MIM capacitors is highly expected in near future [17]. The stability of MIM capacitances are affected by three factors, which are bias voltage, operation frequency and temperature. Harmonic distortions occur at modulator output spectrum, while these nonlinearities appear at integrators in ΣΔ modulators. Fortunately, there are several popular high-K dielectric materials studied to substitute the conventional SiO_2 and Si_3N_4, which are Ta_2O_5, HfO_5 and . They suppress these nonlinearities effectively [18]. In addition to the above mentioned three materials, [19] provides a multi-layered dielectric, which is $HfO_2 - SiO_2$ stacked dielectric. Fig. 16 shows the capacitance variation versus bias voltage can be reduced by employing $HfO_2 - SiO_2$, the capacitance versus bias voltage is the most stable while $HfO_2(12nm)/SiO_2(4nm)$ is employed. Fig. 3 shows that capacitance is increased follow the rise of temperature. This structure dielectric also offers an excellent improvement to reduce the impact of temperature for HfO_5. Due to the existing technique of capacitors fabrication exhibits excellent linearity, hence the distortion cause by nonlinear capacitance in ΣΔ modulators can be neglected reasonable.

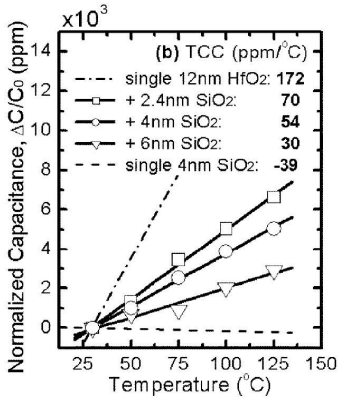
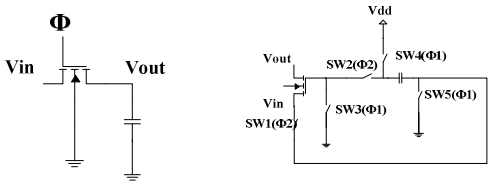


Fig.3 . Normalized capacitance vs. temperature



(a) (b)

Fig. 4. (a) A simple sample and hold circuit. (b). The bootstrapped switch

F. Nonlinear Switch Resistance Distortion

In ΣΔ modulators, the MOS switches in integrators introduce harmonic distortion since the resistances of the MOS switches depends on the voltages across the terminals. Fig. 4(a) shows a simple sample and hold circuit for NMOS [x], and its resistance is given by

$$R_{on} = \frac{1}{\mu_n C_{OX} \frac{L}{W}\left(V_{gs} - V_{tn}\right)} \tag{17}$$

where $V_{tn} = V_{t0} + \gamma\left(\sqrt{2|\phi_F| + V_{SB}} - \sqrt{2|\phi_F|}\right)$. shows that the resistance varies with V_{in} and the body effect (V_{SB}) also contribute nonlinearity, especially in low voltage. There several techniques for improving this nonlinearity were proposed [20], [21] and [22]. [20] mention a new sample-and-hold circuit, which is shown in Fig. 4(b). In order to

avoid that the resistance variation follows by V_{in}, this bootstrapped structure can fix V_{gs} in V_{dd}, hence the resistance of the switch can be given by

$$R_{on} = \frac{1}{\mu_n C_{OX} \frac{L}{W}(V_{dd} - V_{in})} \quad (18)$$

For the second nonlinear factor V_{SB}, [21], [22] and [23] also proposed several techniques to improve its effects. According to the above discussion, due to there are several existed methods to reduce this nonlinear phenomenon effectively, hence we don't involve the distortion into final optimization.

III. POWER CONSUMPTION ESTIMATION

The power consumption can be derived into the analog part and the digital part. The analog power consumption is mainly from OTAs of integrators, quantizer, and DAC. The digital power consumption is mainly from CMOS switches and clock generator.

Basic OTA structure	Single-stage telescope [x]	Folded cascade [x]	two-stage Miller -compensated [x]
k_{OTA}	2	4	7.76

Table Ⅵ k_{OTA} for three common OTA structures

The total power consumption of integrators in $\Sigma\Delta$ modulator can be presented as

$$POW_{\Sigma\Delta\_OTA} = V_{DD} \cdot k_{OTA} \cdot f_{cl2} \cdot \pi \cdot C_{L2} \cdot V_{reff} \cdot k_{\Sigma\Delta} \quad (19)$$

where, f_{cl2} is the *GBW* of the OTAs,

A common DAC branch in $\Sigma\Delta$ modulator is If the sampling period and integration period are both assumed to be $T/2$, the power consumption of an unit capacitor C_u in the multi-bit DAC is

$$POW_{DAC} = 2 \cdot k_{Cs} \cdot V_{ref}{}^2 \cdot C_S \cdot f_s \quad (20)$$

where k_{Cs} is the ratio of the summation of C_S in all stages to the C_S in the first stage.

For quantizer power consumption, [24] offers an good accuracy model as

$$POW_{Quantizer} = \frac{V_{DD}{}^2 \times L_{\min} \times (f_S + f_B)}{10^{(-0.1525 \times B + 4.838)}} \quad (21)$$

where $L_{\min}$ is the minimum channel length of the technology associated. According to the above discussions, the total analog power consumption of $\Sigma\Delta$ modulator is

$$POW_{ana\log} = POW_{OTA} + POW_{DAC} + POW_{Quantizer} \quad (22)$$

The digital power consumption is mainly from the clock generator The average dynamic power consumption of a CMOS inverter gate can be written as

$$POW_{dynamic} = f_S \cdot C_{Logic} \cdot V_{DD}^2$$

where C_{Logic} is the loading capacitors of CMOS logic gates. Assuming a clock generator has N_C CMOS inverters and all inverters have identical loading capacitance of C_{Logic}, then the dynamic power consumption of clock generator is approximately

$$POW_{CLOCK} \cong N_C \cdot f_S \cdot C_{Logic} \cdot V_{DD}^2 \quad (23)$$

Another important source of the digital power dissipation is from CMOS transmission gates in the switched-capacitor circuits.

The power consumption for all the transmission gates is

$$POW_{Switch} = N_S \cdot f \cdot C_{gate} \cdot V_{DD}^2 \quad (24)$$

Finally, the total digital power consumption is

$$POW_{digital} = POW_{CLOCK} + POW_{Switch} \quad (25)$$

The total power consumption is

$$POW_{total} = POW_{ana\log} + POW_{digital} \quad (26)$$

IV. CONCLUSIONS

Entering the nonlinear distortion power models into optimization which are not offered in [1] is the main contribution of this work. By combining these distortion power models with the noise power models in Appendix into optimization, the optimal design specifications are obtained. All the nonlinearity power also can be obtained after an complete optimization, and the dominating nonlinearity power can be reduced by adjusting the design specifications. Fourth, our optimization method can be hundreds of times faster than existing behavioral simulation based approaches.

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