經由非線性分析與功率消耗分析求致Sigma-Delta Modulator ADC 之設計最佳化

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Abstract —在第二年計畫中,我們的主要目標是經由非線性的分析去獲得OTA nonlinear DC-gain 非線性失真模型. OTA在SDM架構中爲重要元件. 隨著面積與供應電壓的下降, 一個放大器合適的增益將越來越重要. 如果增益太大, 則放大器會消耗更大的功率. 如果增益太小, 則諧波的問題會變嚴重. 然而目前沒有一個有效的方法去評斷增益爲何是最理想的.在本期刊中, 我們先使用nonlinear function去模擬OPA的DC-gain曲線, 接著使用此函式去產生SDM nonlinear distortion model. 而使用此模型可以知道再容許的Distortion値內, 需要多大的增益. 而非理想增益曲線以及SDM非線性諧波模型在本期刊中, 顯示他的behavior simulation 跟transistor level simulation.

***Index Terms* — sigma delta modulator, nonlinear distortion, op-amp DC-gain.**

I. Introduction

Sigma-delta modulators (SDM) based on switched-capacitor circuits have been suitable for high-resolution applications. Recently, low power designs become a very important trend for SDM applications. Since op-amps consume most power in SDM, it is crucial to determine a suitable op-amp DC-gain. If DC-gain is set too high, the op-amp can consume too much power; if DC-gain is too small, nonlinear distortion can become serious. However, there exists no efficient and systematic approach for selecting DC-gains.

Currently, there are two major approaches for selecting op-amp DC-gains. The first approach is *ad hoc* based [1-3], which usually suggests setting DC-gain at a sufficiently large value, e.g. 70 dB, so that nonlinear distortion can be small enough. This can be too conservative, since the DC-gain can actually be smaller for certain applications. The other approach for selecting op-amp DC-gain requires intensive simulations and subsequent computations [4-6]. In this approach, time-consuming Spice simulation is first used to identify the nonlinear DC-gain curve of a specific op-amp design, and then magnitude of distortion is computed from the nonlinear curve identified. If the computed distortion is too large or too conservative (too small), the op-amp design has to be modified so that DC-gain can be adjusted. Then, one needs to carry out the aforementioned simulation and computation again. This iterative process would continue until a suitable DC-gain is determined. So the existing approaches are either not accurate enough or not time-efficient.

In this paper we propose an accurate and efficient approach for selecting op-amp DC-gain. An essential first step in our method is the creation of a general model for nonlinear op-amp DC-gain curves. The importance of this nonlinear DC-gain model is that it eliminates the need for time-consuming Spice simulations described above. Then, the nonlinear DC-gain curve model can be employed to analytically derive the nonlinear distortion which appears at SDM output. Since the nonlinear distortion model is expressed in terms of DC-gain and other SDM parameters, it can be used to accurately compute the minimum required op-amp DC-gain such that the nonlinear distortion is kept under a tolerable value. The nonlinear DC-gain curve model and the nonlinear distortion model are verified by transistor level simulations. Their application to sigma-delta modulators is verified by behavior simulations.

II. OP-AMP NONLINEAR DC-GAIN CURVES

A. DC-Gain Distortion Can Be Severe

A second order SDM with OSR = 20, V_{OS} = 0.6, a 3-bit quantizer, a 1V sinusoidal input signal, and a relatively small DC-gain A_o = 50db, will see a severe DC-Gain distortion at about -61dB, which easily dominates other noises and distortions, e.g. quantization noise (-81 dB) and DAC distortion (-76 dB, without DEM), and results in a poor SNDR at 60 dB.

B. Modeling Nonlinear DC-Gain Curves

It is well known that the output resistance of op-amp output-stage-transistors is dependent on the output voltage V_o. This dependency results in nonlinear op-amp DC-gain when V_o changes, as is shown in Fig. 1. A typical nonlinear DC-gain curve can be approximated by the polynomial:

$$A_V(V_o) = A_0(1 + q_2V_o^2 + q_4V_o^4) \quad (1)$$

where $A_V(V_o)$ is the nonlinear DC-gain of op-amp, and A_o is the maximum DC-gain when V_o is in the neighborhood of 0V.

It is well known that $|V_{GSQ}|$ of the output-stage transistors and the maximum DC-gain A_o are the only two parameters which can affect the shape of the nonlinear curves $A_V(V_0)$. It is also

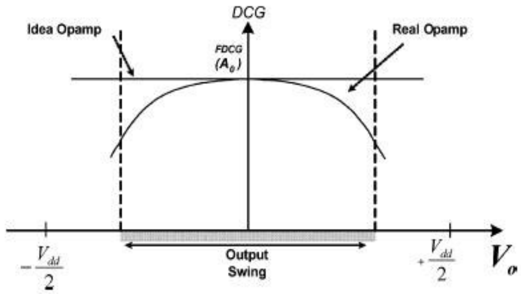

Fig. 1. DCG curve versus output voltage with the rail to rail voltage of VDD

well known that maximum output swing V_{OS} and $|V_{GSQ}|$ have germane relation with each other. Since V_{OS} makes much more sense for practical designers, we replace $|V_{GSQ}|$ by V_{OS}, and in the rest of this paper V_{OS} and A_O are the only two parameters which affect $A_V(V_o)$. In order to demonstrate the effects of V_{OS} and A_O on $A_V(V_o)$, Spice op-amp simulations in Fig. 2(a), (b) respectively show the effects that A_O and V_{OS} can have on the shape of DC-gain curves.

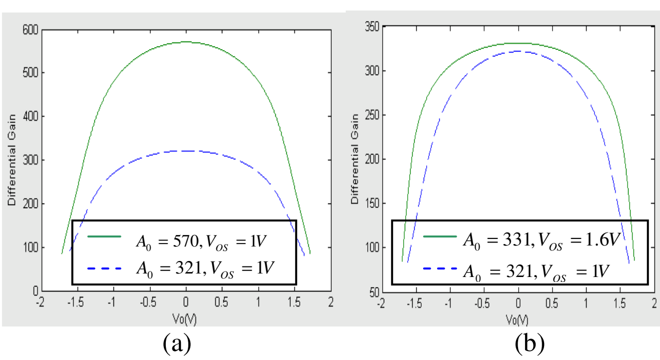

Fig. 2. (a) Two nonlinear DC-gain curves with identical V_{OS} but different A_O
(b) Two nonlinear DC-gain curves with similar A_O but different V_{OS}

In order to model the nonlinear gain $A_V(V_0)$, we tried various combination of A_O and V_{OS} to create a set of representative curves for the family of nonlinear DC-gain curves. Then, we endeavored to find out suitable q_2 and q_4 such that (1) can reasonably fit all of these curves. After intensive tries and errors, we come up with the q_2 and q_4 in (1) to be

$$q_2 \equiv -9 \cdot \left(\frac{A_O^{0.01}}{(1+V_{OS})^{2.6}}\right)^2 \tag{2}$$

$$q_4 \equiv -6 \cdot \left(\frac{A_O^{0.0001}}{(1+V_{OS})^{0.83}}\right)^4 \tag{3}$$

Although the q_2 and q_4 are obtained from tries and errors, the searching and testing time for them is more than one year. We are confident that the model (1) – (3) is sufficiently general and accurate, as is verified in the next subsection.

C. Verifying Nonlinear DC-Gain Curve Model

Comparisons of DC-gain curves from real op-amps and from our model (1) – (3) are shown in Fig. 3. The comparisons are

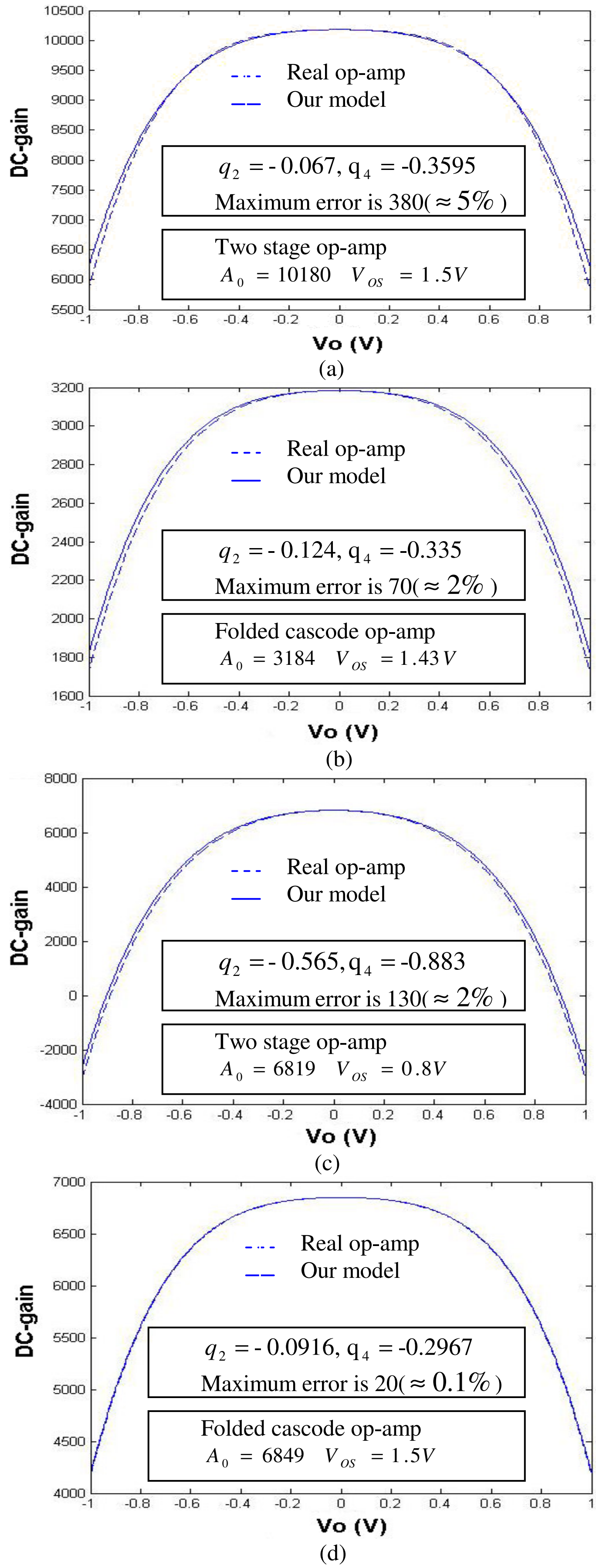

Fig. 3. Comparisons between op-amp nonlinear DC-gain curves from real op-amp (solid line) and from our model (dashed line)

deliberately planed to cover various op-amp structures and representative points in op-amp parameter space. The sub-figures in Fig. 3 are cross-related as follows:

1. (a) and (c) are two-stage op-amps, and (b) and (d) are folded cascode op-amps.
2. (a) and (b) have large difference in the values of A_O.
3. (c) and (d) differs mainly in V_{OS}.

For the four cases presented in Fig. 3, the errors between op-amp nonlinear DC-gain curves from real op-amps and from our model range from 0.1% to 5%. This demonstrates that our model (1) – (3) is sufficiently general and accurate.

III. SDM DISTORTION DUE TO THE NONLINEAR DC-GAIN OF THE OPERATIONAL AMPLIFIER

In section II, we analyze the op-amp nonlinear DC-gain phenomenon, and obtain a nonlinear DC-gain model (1) – (3). In this section, based on the model (1) – (3), we want to derive a nonlinear distortion model for single-loop 2nd order SDM output distortions caused by nonlinear DC-gain in op-amps. Fig.4 shows the block diagram of an ideal SDM. We will first discuss the property of V_S which is the input to the first integrator. Then the transfer characteristics of the integrator are analyzed, based on which the SDM nonlinear DC-gain distortion model is derived. Distortion models for other SDM structures can be obtained following the approach in this section.

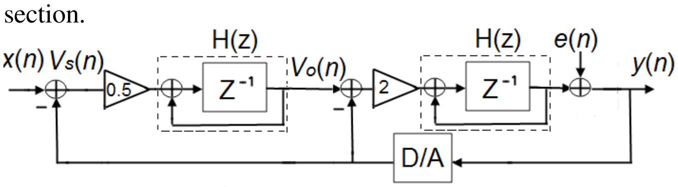

Fig. 4 Single-loop second-order ΣΔ modulator

A. Properties of V_S

In Fig. 4, the SC integrator input V_S can be expressed as

$$V_S(z) = (1 - z^{-2})X(z) - (1 - z^{-1})^2 E(z) \tag{4}$$

which includes the signal part and the noise part. The noise part can be ignored here. To analyze the signal part, with $x(n) = A_{in}\sin(wnT)$, the inverse z-transform is performed on (4), and one obtains

$$\begin{aligned} V_S(nT) &= A_{in}\sin(wnT) - A_{in}\sin(w(n-2)T)\cdot u(w(n-2)T) \\ &\approx -A_{in}\cdot\sin(\frac{2\pi}{OSR})\cdot\cos(wnT) \end{aligned} \tag{5}$$

Then, the amplitude of V_S can be approximated as

$$|A_{VS}| = |V_S(2nT)| = |A_{in}\sin(2wnT)| \cong 2A_{in}\cdot w\cdot T \tag{6}$$

B. Transfer Characteristics of the First Integrator

The sampling phase and integration phase of a switch capacitor integrator are shown in Fig. 5. In the following discussion, signals $V_O((n+1/2)T)$, $V_O((n-1/2)T)$ and $V_s(nT)$ will be respectively denoted by V_O^+, V_O^- and V_S. Suppose settling problem is ignored, which requires separate treatment. Then, the sampling phase is ideal, and the input/output characteristics of the integration phase can be completely described by the following three equations

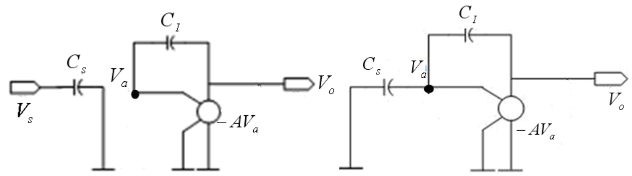

Fig. 5 Switch-capacitor integrator with nonlinear DC-gain op-amp

$$A_V(V_O) = A_O(1 + q_2 V_O^{\ 2} + q_4 V_O^{\ 4}) \tag{7}$$

$$V_O^{\ \pm} = -A_V(V_O^{\ \pm})\cdot V_a^{\ \pm} \tag{8}$$

$$C_I\cdot(V_o^+ - V_a^+) - C_S\cdot V_a^+ = C_I\cdot(V_o^- - V_a^-) + C_S\cdot V_S \tag{9}$$

Substituting (7) and (8) into (9), one obtains the following expression

$$\begin{aligned} &V_O^{\ +} - V_O^{\ -} \\ &= K_S\cdot\{1 + \frac{1}{A_O}\cdot[q_2\cdot((V_O^{\ +})^2 + (V_O^{\ +})(V_O^{\ -}) + (V_O^{\ -})^2) + (q_4 - q_2^{\ 2})\cdot((V_O^{\ +})^4 \\ &+ (V_O^{\ +})^3(V_O^{\ -})^1 + (V_O^{\ +})^2(V_O^{\ -})^2 + (V_O^{\ +})^1(V_O^{\ -})^3 + (V_O^{\ -})^4)] + \cdots\frac{1}{A_O^{\ \infty}}\}\cdot V_S \end{aligned} \tag{10}$$

where K_S is C_S / C_I. The problem with (10) is that the integrator output $V_O^{\pm}$ also appears at right-hand-side of (10). However, since $V_O^{\pm}$ can be shown to relate to V_S in (5) as follows

$$V_O^{\pm} \approx -\frac{K_S}{1 + \frac{1 + K_S}{A_O}}\cdot\frac{1}{\sqrt{4 - \frac{4\cdot K_S}{A_O}}\cdot\sin\frac{wT}{2}}\cdot\{A_{VS}\cdot\sin\left(w(n\pm\frac{1}{2})T\right)\} \tag{11}$$

the $V_O^{\pm}$ and V_S at right-hand side of (10) can be substituted by (11) and (5), resulting in

$$\begin{aligned} V_O^{\ +} - V_O^{\ -} = K_S\cdot\frac{1}{A_O}\{&\frac{3}{4 - \frac{4K_S}{A_O}}\cdot\left(\frac{K_S}{1 + \frac{1 + K_S}{A_O}}\right)^2\cdot A_{VS}^{\ 2}\cdot q_2\cdot\cot^2(\frac{1.5708}{OSR})\cdot\sin^2(wnT) \\ &+ \frac{5}{(4 - \frac{4K_S}{A_O})^2}\cdot\left(\frac{K_S}{1 + \frac{1 + K_S}{A_O}}\right)^4\cdot A_{VS}^{\ 4}\cdot(q_4 - q_2^{\ 2})\cdot\cot^4(\frac{1.5708}{OSR})\cdot\sin^4(wnT) \\ &+ \frac{10}{(4 - \frac{4K_S}{A_O})^2}\cdot\left(\frac{K_S}{1 + \frac{1}{A_O}}\right)^4\cdot A_{VS}^{\ 4}\cdot(q_4 - q_2^{\ 2})\cdot\cot^2(\frac{1.5708}{OSR})\cdot\cos^2(wnT)\cdot\sin^2(wnT) \\ &+ \frac{1}{(4 - \frac{4K_S}{A_O})^2}\cdot\left(\frac{K_S}{1 + \frac{1}{A_O}}\right)^4\cdot A_{VS}^{\ 4}\cdot(q_4 - q_2^{\ 2})\cdot\cos^4(wnT)\} \\ &\cdot\{A_{in}\sin(wnT) - A_{in}\sin(w(n-2)T)\cdot u((n-2)T)\} \end{aligned} \tag{12}$$

Equation (12) can be used to compute nonlinear DC-gain distortions appearing at 1st integrator output.

C. Nonlinear DC-gain Distortions at SDM Output

It is known that if the gain of the 2nd integrator equals one, i.e. $C_{S2}/C_{I2} = 1$, the same distortions appearing at 1st integrator output would appear at SDM output. Otherwise, some modification is needed on distortions at SDM output. Suppose 2nd integrator gain equals one. Then, the 3rd harmonic magnitudes in DC-gain disotritons can be computed from (12) as follows

$$A_{\sin\_3} = K_S \cdot \frac{1}{A_O} \cdot \frac{1}{16} \cdot \{[\frac{-12}{4-\frac{4K_S}{A_O}} \cdot \cot^2(\frac{1.5708}{OSR}) + \frac{4}{4-\frac{4K_S}{A_O}}] \cdot [\frac{K_S}{1+\frac{1+K_S}{A_0}}]^2 \cdot A_{VS}^2 \cdot A_{in} \cdot q_2 + [\frac{-25}{(4-\frac{4K_S}{A_O})^2} \cdot \cot^4(\frac{1.5708}{OSR}) + \frac{10}{(4-\frac{4K_S}{A_O})^2} \cdot \cot^2(\frac{1.5708}{OSR}) + \frac{3}{(4-\frac{4K_S}{A_O})^2}] \cdot [\frac{K_S}{1+\frac{1+K_S}{A_0}}]^4 \cdot A_{VS}^4 \cdot A_{in} \cdot (q_4 - q_2^2)\} \cdot \left[1-\cos(\frac{2\pi}{OSR})\right] \quad (13)$$

$$A_{\cos\_3} = K_S \cdot \frac{1}{A_O} \cdot \frac{1}{16} \cdot \{[\frac{-12}{(4-\frac{4K_S}{A_O})^2} \cdot \cot^2(\frac{1.5708}{OSR}) - \frac{4}{(4-\frac{4K_S}{A_O})^2}] \cdot [\frac{K_S}{1+\frac{1+K_S}{A_0}}]^2 \cdot A_{VS}^2 \cdot A_{in} \cdot q_2 + [\frac{-15}{(4-\frac{4K_S}{A_O})^2} \cdot \cot^4(\frac{1.5708}{OSR}) - \frac{10}{(4-\frac{4K_S}{A_O})^2} \cdot \cot^2(\frac{1.5708}{OSR}) + \frac{5}{(4-\frac{4K_S}{A_O})^2}] \cdot [\frac{K_S}{1+\frac{1+K_S}{A_0}}]^4 \cdot A_{VS}^4 \cdot A_{in} \cdot (q_4 - q_2^2)\} \cdot \left[\sin(\frac{2\pi}{OSR})\right] \quad (14)$$

The forms for magnitudes of 5th harmonics $A_{\sin\_5}$ and $A_{\cos\_5}$ can also be computed from (12), but are omitted here. Then the powers of the 3rd and 5th harmonic distortions are

$$HD3_{NFDCG}(dB) = 10\log\frac{(A_{\sin\_3}^2 + A_{\cos\_3}^2)}{2} \quad (15)$$

$$HD5_{NFDCG}(dB) = 10\log\frac{(A_{\sin\_5}^2 + A_{\cos\_5}^2)}{2} \quad (16)$$

The model (13)-(16) indicates that the DC-gain distortions at SDM output are related to C_I, C_S, A_{in}, A_O, V_{OS} and OSR. Some qualitative properties about how each parameter can affect distortion magnitude are obtained from (13) – (16) and listed in TABLE I.

TABLE I
The relationship between the each parameter and the harmonic distortions

	C_I ↑	C_S ↑	A_{in} ↑	A_0 ↑	V_{os} ↑	OSR ↑
Distortion magnitude	↓	↑	↑	↓	↓	↓

Some quantitative investigation based on (13) – (16) shows that A_O and OSR are the most influential parameters on SDM DC-gain distortions. Therefore, an interesting example about how (13) – (16) can be utilized is that if the four parameters are fixed at $A_{in} = 1\text{v}$, $V_{OS} = 0.8$, $C_S = 1\text{pF}$ and $C_I = 2\text{pF}$, then (13) – (16) can be employed to determine the minimum A_O and OSR required so that the DC-gain distortion can be kept under certain value. The results are tabulated in TABLE II.

TABLE II
Minimum required A_O and OSR

HD3 distortion power(dB)	HD5 distortion power(dB)	A_0	*OSR*
-70	-80	≧1000	≧16
-90	-100	≧3000	≧64
-110	-120	≧6400	≧256

Due to loop shaping, the DC-gain nonlinearity in the second integrator degrades the performance to a much lesser extent, allowing a more relaxed design [7]. Therefore, only the DC-gain distortion caused by first integrator is considered in this paper.

IV. TRANSISTOR LEVEL SIMULATION RESULT

The proposed model serves as a powerful tool for analyzing nonlinear DC-gain distortion for sigma delta modulators. In order to verify the accuracy of our model at transistor level, the circuit of a general integrator has been realized using classical two-stage architecture in Spice.

The specifications of the op-amp are A_O =80dB, V_{OS} =±1.5V, K_S =1, and the sinusoidal input frequency is 10k. Integrator output FFT is shown in Fig. 6. The total harmonic distortion (THD) is mainly determined by the third harmonic distortion (HD3) and the fifth harmonic distortion (HD5). It is indicated in Fig. 6 that HD3 and HD5 are -56.9dB and -67.3dB respective, and the HD3 and HD5 generated from our model are -63.9dB and -73.5978dB respective. The theoretical results and simulation results are close, and are listed in TABLE Ⅲ.

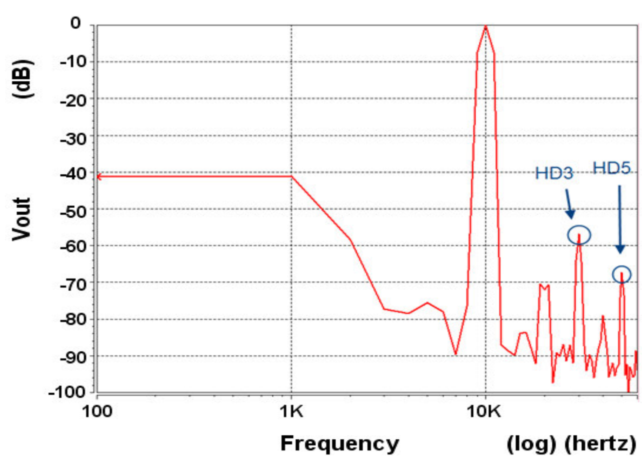

Fig. 6. Spice simulation FFT Results with K_S =1, A_O =80dB, V_{OS} =1.5V, and F_{in}=10k

TABLE Ⅲ
Comparison of theoretic result and Spice simulation

	Theoretic (dB)	Spice simulation (dB)
HD3	-63.9	-56.9
HD5	-73.5978	-67.3

V. BEHAVIOR MODEL SIMULATION RESULTS

A. Behavior Model of Nonlinear DC-Gain

We use a calculable behavior model to verify our SDM nonlinear DC-gain distortion model. The z-domain transfer function of a delayed integrator of sigma-delta modulator is

$$H(z) = g \cdot \frac{z^{-1}}{1-\alpha \cdot z^{-1}} \tag{17}$$

where g and α are the integrator gain and leakage [8].

B. Behavior Model of SDM with Nonlinear DC-Gain

Then, one can place the nonlinear DC-gain behavior model (17) into the complete sigma delta modulator behavior simulation scheme. The diagram is shown in Fig. 7.

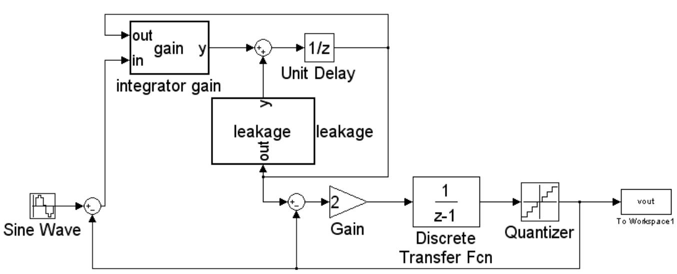

Fig. 7. Second-order SDM behavior model with nonlinear DC-gain

The behavior simulations are conducted for two different cases. The SDM output FFTs are shown in Fig. 8. The comparisons between simulation results and theoretical results are shown in TABLE IV. The results from both simulation cases are very close to those obtained from our DC-gain distortion model.

TABLE IV
Comparison of theoretic result and Simulink simulation

	Theoretic (dB)	Simulink(dB)
A_o = 10180, V_{os} = 1.5	HD3 = -93.72 HD5 = -105.42	HD3 = -92.55 HD5 = -104.2
A_o = 6819, V_{os} = 0.8	HD3 = -81.44 HD5 = -94.23	HD3 = -80.19 HD5 = -93.43

VI. CONCLUSION

In this paper, we derive first the model for op-amp nonlinear DC-gain curves, and then the model for DC-gain distortion at SDM output. The nonlinear DC-gain curve model is never seen in literature before. It can be useful and important for both industrial and academia applications. The completeness and precision of our DC-gain distortion model are also new and important contributions. Both models are intensively verified

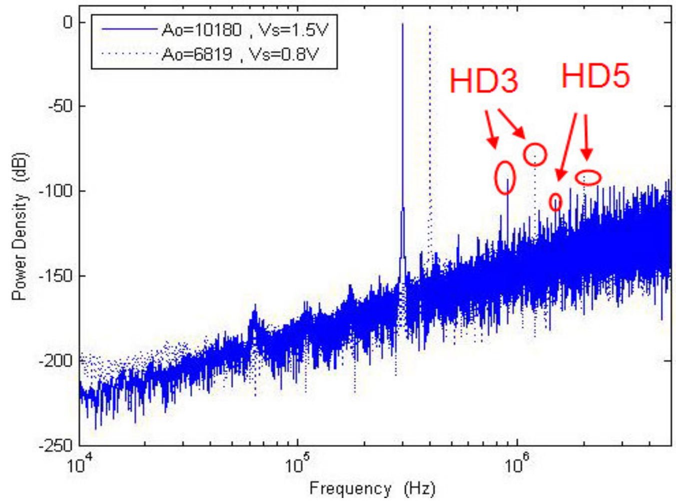

Fig. 8. The modulator's output PSD

by transistor-level and/or behavior simulations.

There are many different ways to apply the two models proposed in this paper, some of which have been suggested in section III. In particular, our models will be very useful in model-based ΣΔ modulator design optimization. Behavior-simulation-based ΣΔ modulator design optimization has been reported in [9]. In comparison, model-based optimization can be much faster and provide more insights about the system under design.

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