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□期中進度報告

經由非線性分析與功率消耗分析求致

Sigma-Delta Modulator ADC 之設計最佳化

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計畫參與人員：

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中　華　民　國　99 年　10　月 22　日

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摘 要

傳統高階積分三角調變器的設計上，主要是依賴行為模擬的方法。然而此方法實在相當耗時。本成果是第一個提出使用模組化設計的方法去設計積分三角調變器。在時間上，使用模組化的設計方法將會比使用行為模擬的方法快上萬倍。由於之前非理想雜訊及失真模型不完備，模組化設計的方法一直無法真正的去實現。現在，因為積分器充放電雜訊模型以及放大器的非線性直流增益諧波失真模型的推出，使得模組化設計方法得以實現。然而，使用模組化設計將會遭遇到雜訊相依的問題；本成果提出雜訊相依模型以便解決這個問題。除此之外，本成果也同時提出積分三角調變器最佳化設計流程。相對於兩篇積分三角調變器設計實例，模組化積分三角調變器最佳化設計將可以使用更短的時間去達到更高的訊號對雜訊以及失真比，同時降低積分三角調變器的功率消耗。

Design Optimization of Discrete-time Single-Loop Sigma-Delta ADCs via Nonideality and Power Analyses

Fu-Chuang Chen

***Abstract* — A conventional ΣΔ ADC design approach is a time consuming process and needs much trials and errors. An optimization algorithm for the discrete-time single-loop ΣΔ ADCs design is proposed. Circuit nonideality models are derived in output noise power forms through a systematic circuit imperfection study. A power model is also presented in order to estimate relative power consumption. These models reveal that design parameter variation can potentially affect several noises and errors in different ways, and may change system power consumption. This design complexity is qualitatively summarized into a table. Model completeness allows us to propose an optimization algorithm to search globally for a design parameter combination which meets SNR requirement while minimizing power consumption. Our optimization algorithm is tested against two published design results, and is verified by behavior simulations. Comparisons with behavioral-simulation-based optimization approaches are also made.**

Index Terms—**Sigma delta modulator, noise model, power model, optimization**

I. Introduction

ΣΔ modulators are widely used for high-resolution analog-to-digital conversion applications, achieving resolutions up to 12~20 bits. The earlier focus is on low to medium speed applications, such as audio [1, 2, 3], voice codec, and DSP chip [4]. Recently, ΣΔ ADCs have been applied to higher bandwidth signals, and low power designs are frequently emphasized. For example, in ×DSL [5, 6] applications, signals up to 2.2MHz must be handled. Since significantly increasing the sampling rate is difficult, designers either seek to increase the order or the cascade stages [7, 8, 9], or employ multi-bit quantization [10, 11], or both, in order to achieve the required dynamic range. DAC linearity can be improved due to process technology advances, making the multi-bit architecture more popular. New technologies also help reduce power consumption [12]. The ΣΔ modulator design is a complex and a time consuming process, because many coupled design parameters must be determined. Coming up with an acceptable design is very challenging with increasing design specification demands. Even an acceptable design may not be the best one. The paper proposes an optimization approach to increase automation and reduce complexity in single-loop ΣΔ ADCs design.

To propose an optimization algorithm for single-loop ΣΔ modulators, we need a complete set of important nonideality models and the power consumption model. Some issues concerning ΣΔ modulator noise and error modeling appeared in [2, 3, 13-22]. System simulation tools were proposed in [13] and [22]. The results in [14-16] are not expressed in noise power forms, so the relations between circuit parameters and noise powers are not clear. Reference [17] worked on the settling noise and the thermal noise, but certain settling error assumptions are not general enough to handle multi-bit cases. Results in [19] [20] focus on device noises such as thermal noise and flicker noise. Flicker noise is not considered in this work because it is affected by factors less correlated to the ΣΔ modulator circuit parameters treated in this paper. The available models discussed above are either incomplete, or not in the form we require. In section II, we will elaborate on settling noise, DAC noise, OTA thermal noise, and reference voltage thermal noise. We will also categorize all major nonidealities into five parts, and express their models in noise power forms under a multi-bit setup. Power consumption models for ΣΔ modulator analog, digital and multi-bit quantizer parts [23, 24, 25] will also be given.

An optimization design scheme is proposed in section III. It essentially combines system and circuit level designs, and optimizes all design parameters at the same time. This paper works on optimization of SNR, not SNDR. Nonlinear distortions are not considered in this paper. There exist applications where nonlinear distortions are often neglected. For example, in low-frequency, high resolution applications such as sensor signal conversion, people consider SNR only, and SNDR is not needed. The design optimization scheme is verified in section IV, and comparisons with behavior-simulation-based optimization schemes [48, 49] are also discussed. Conclusions are presented in section V. Then a nonlinear settling distortion analysis is given in the Appendix A to resolve issues in Section Ⅳ. Finally several modified noise power models for the circuit structure of [28] are provided in Appendix B.

II. Models of Nonidealities and Power

Proposing an optimization algorithm for searching design parameters which maximizes ΣΔ ADC SNR while minimizing power consumption is one of the primary purposes in this paper. Model completeness determines success of this goal. The ΣΔ modulator nonidealities are categorized into five parts in this section: finite OTA gain error, thermal noise, settling error, multi-bit DAC noise, and jitter noise. All nonideality

models are expressed in noise power forms, which can

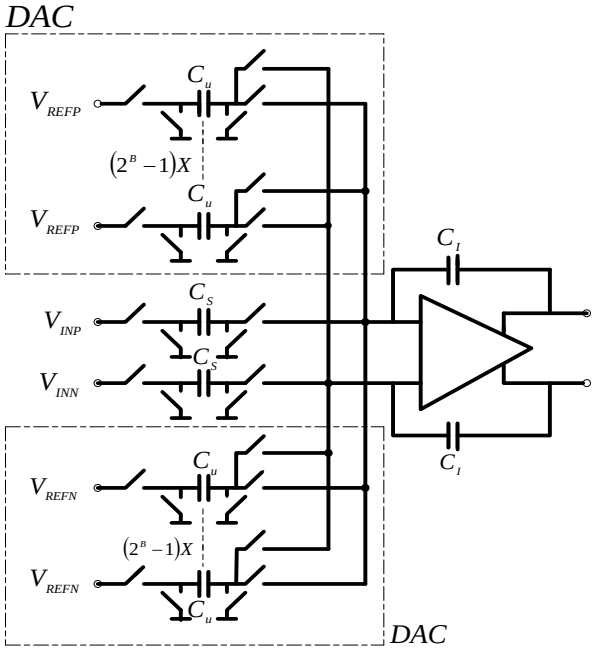


Fig. 1 Integrator and the DAC branches

directly add to ideal quantization noise power. All noise power models discussed in the following are based on the integrator scheme, as shown in Fig.1. In Fig. 1, C_u is the unit capacitor whose capacitance is $\frac{C_S}{2^B}$. The power consumption model is presented as the last part of this section.

A. Finite OTA Gain Error

For a general single-loop *n*th order ΣΔ modulator with finite OTA gain *A*, the modified quantization noise is expressed as [18]

$$P_{Q(\text{mod.})} \cong \frac{\Delta^2}{12}\cdot\left[\frac{\pi^{2n}}{(2n+1)\cdot OSR^{2n+1}}+\left(\frac{a_1}{A}\right)^2\cdot\frac{\pi^{2n-2}\cdot n}{(2n-1)\cdot OSR^{2n-1}}\right] = P_Q + P_{AV} \quad (1)$$

where P_Q is the original quantization noise, a_1 is the gain of the integrator at the first stage, and Δ is the quantizer step size. The P_{AV} in (1) is due to finite OTA gain, and can be considered as an additive quantization noise power.

B. Thermal Noise (Switch, OTA, Reference circuits)

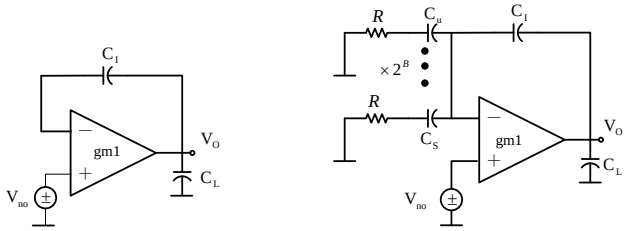
There are three thermal noise sources in the ΣΔ modulator, in MOS switches, OTAs and reference voltage. The analyses are shown separately as follows.

The total output switches thermal noise power from the switched capacitor integrator is [18, 23]

$$P_{sw} \cong \frac{1}{OSR}\cdot\left(\frac{8\text{kT}}{C_S}\right) \quad (2)$$

Half of P_{sw} is from the input branch, and the other half is from the DAC branch.

The OTA transistor thermal noise can be modeled as an equivalent noise source V_{no} at OTA input shown in Fig.2.



(a) sampling phase (b) Integration phase

Fig. 2 Equivalent circuits of sampling and integration phases

In deep submicron process $\text{V}_{\text{no}} \cong \frac{\alpha\cdot 10\text{kT}}{\text{gm1}}\ \text{V}^2/\text{Hz}$ [26], thermal noise power at integrator output in the sampling phase is

$$P_{OTA}(samp) \cong \text{V}_{\text{no}}\cdot\frac{GBW_{\text{samp}}}{A\cdot 2\pi}\cdot\frac{\pi}{2} = \frac{10\alpha\cdot\text{kT}}{4AC_L} \quad (3)$$

During the integration phase (Fig. 2(b)), the circuit looks like a non-inverting amplifier, with

$$\frac{\text{V}_{\text{O}}}{\text{V}_{\text{no}}}(s) \cong \left(\frac{2a_1+1+2sC_SR}{1+2sC_SR}\right) \Big/ \left(1+\frac{s}{GBW/A}\right) \quad (4)$$

The OTA noise power at the first integrator output can be expressed as

$$P_{OTA}(\text{int}) \cong \int_0^\infty \text{V}_{\text{no}}\cdot\left|\frac{\text{V}_{\text{O}}}{\text{V}_{\text{no}}}(f)\right|^2 df \quad (5)$$

Finally, the total OTA thermal noise power at the ΣΔ ADC output can be obtained as

$$P_{OTA} = \frac{1}{OSR}\cdot\left(\frac{1}{a_1}\right)^2\cdot\left(P_{OTA}(samp)+P_{OTA}(\text{int})\right) = \frac{1}{OSR\cdot a_1^2}\cdot\left(\frac{10\alpha\cdot\text{kT}}{4AC_L}+\int_0^\infty \text{V}_{\text{no}}\cdot\left|\frac{\text{V}_{\text{O}}}{\text{V}_{\text{no}}}(f)\right|^2 df\right) \quad (6)$$

Consider the bandgap reference circuit in Fig. 3 [27]. Reference output noise is nearly equivalent to OTA input referred noise [27], so it can be expressed as $\overline{V_{ref}^{\ 2}} \approx \text{V}_{\text{no}} = \frac{10\text{kT}\cdot\alpha}{\text{gm1}}$. Different integrator schemes can introduce reference noise in different ways [5, 11, 28]. The case shown in Fig. 4 is considered, where this noise is introduced only in the sampling phase. If the reference noise is unbuffered, its noise power at the ΣΔ ADC output can be derived as

$$P_{ref} = \frac{1}{OSR}\cdot\int_0^\infty \frac{\overline{V_{ref}^{\ 2}}}{1+4\pi^2R^2C_S^2f^2}df = \frac{\overline{V_{ref}^{\ 2}}}{OSR\cdot 4RC_S} \quad (7)$$

It's usual to add buffers between the bandgap circuits [29] and the DAC paths. Denote the 3dB buffer bandwidth as BW_b. If BW_b is smaller than $\frac{1}{4RC}$, P_{ref} in (7) is changed to be $P_{ref} = \overline{V_{ref}^{\ 2}}\cdot\frac{\pi\cdot BW_b}{2\cdot OSR}$. If BW_b is larger than $\frac{1}{4RC}$, (7) is applied.

C. Settling Error

As ΣΔ modulator sampling frequency increases, and

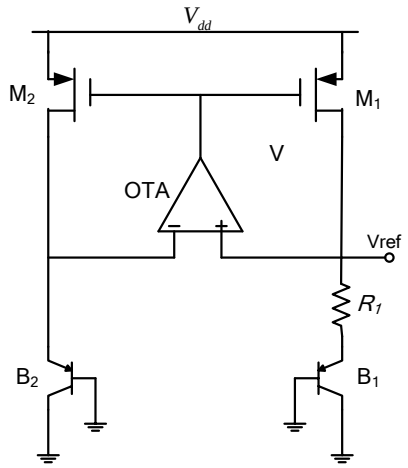


Fig. 3 A bandgap voltage reference circuit

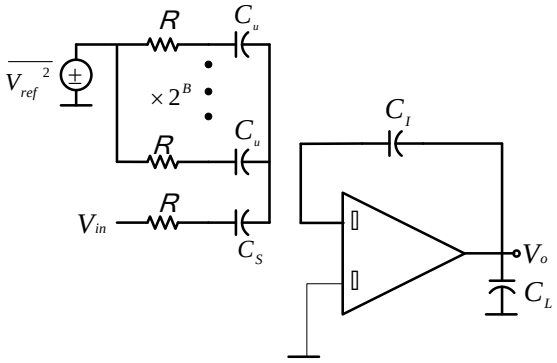


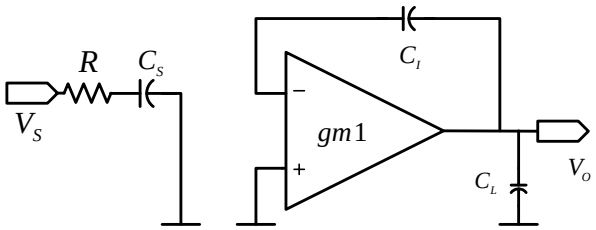
Fig. 4 Equivalent circuit while considering reference voltage noise

multi-bit quantization becomes a high resolution and high-speed application trend, the dynamic settling problem of switched capacitor integrator becomes a more dominant factor. Previous articles have mentioned the settling error [14, 21, 30]. References [14] and [30] provide behavior models, which are tedious and integrate poorly with noise-power models of other noises or errors. The noise-power model of [21] is very primitive since it assumes the p.d.f.(probability density function) settling error is uniformly distributed, and does not consider multi-bit quantization. We only consider the integrator at the first stage. Settling errors at later stages are less influential due to noise shaping.

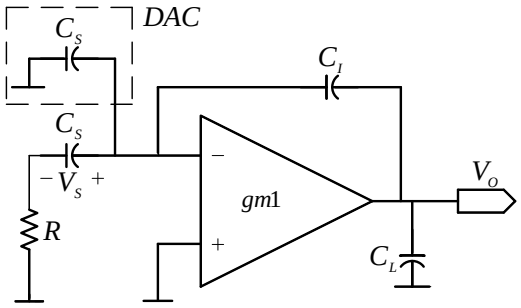
Now consider a switched capacitor integrator in Fig. 5. Assume the MOS switch has an on-resistance *R*, and gm1 is the transconductance of OTA. Let the output parasitic capacitor $C_L \cong \eta \cdot C_I$, where η is the parasitic percentage of bottom plate, assumed to be 20% [31]. In Fig. 5(a), the voltage V_S represents the difference between the sinusoid input signal and the feedback signal from DAC. It is sampled by C_S, C_S is charged in the half clock period $\frac{T}{2}$ to the voltage V_{CS}:

$$V_{CS} = V_S \cdot [1 - \exp(-\frac{T}{2 \cdot \tau_1})] \tag{8}$$

where $\tau_1 = R \cdot C_S$ is the time constant in the input branch. So the setting error during the sampling phase is:



(a) Sampling phase



(b) Integration phase

Fig. 5 Switched capacitor integrator diagrams

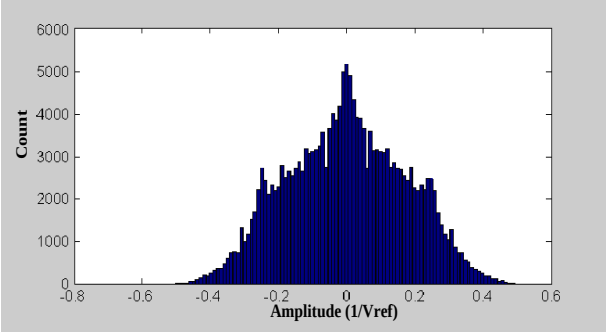


Fig. 6 Simulated results of V_S distribution

$$\varepsilon_1 = V_S \cdot \exp(-\frac{T}{2 \cdot \tau_1}) \tag{9}$$

In order to obtain settling noise power during the sampling phase from (9), we need to find the V_S statistical property. Simulations results (using SIMULINK) on a second-order ΣΔ modulator with $a_1 = 0.5$, $a_2 = 2$, 10-level quantization, reference voltage $V_{ref} = \pm 1V$, and a full scale sinusoidal input signal, are shown in Fig. 6. The result is close to a Gaussian distribution. Therefore, we assume V_S is Gaussian distributed with a zero mean. The standard deviations σ_{VS} of V_S under different quantizer levels are tabulated in Table I. We observed that when the quantizer level N increases, σ_{VS} decreases. From this table, the relation between standard deviation σ_{VS} and quantizer levels 2^B can be approximated by

$$2^B \cdot \sigma_{VS} \approx 1.4 \cdot |V_{ref}| \tag{10}$$

The settling noise can reasonably assumed to be white, and its power spectral density constant and distributed over $(-f_S/2, f_S/2)$ as

$$S_{\varepsilon 1} = \frac{1}{f_S} \cdot \left(\frac{1.4 \cdot V_{ref}}{2^B} \right)^2 \cdot \exp(\frac{-T}{\tau_1}) \tag{11}$$

Due to oversampling, noise power can be obtained by

Std. deviation (σ_{VS})	Variance	Quantizer level (N)	Bit number (B)
0.706	0.498	2	1
0.476	0.227	3	1.585
0.282	0.080	5	2.322
0.198	0.040	7	2.808
0.152	0.023	9	3.17
0.124	0.016	11	3.46
0.047	0.002	31	4.95

TABLE I Standard deviations of V_S v.s. different quantizer bit numbers

integrating (11) in the signal band $(-f_B, f_B)$, which is

$$P_{\varepsilon 1} = \frac{1}{OSR} \cdot \left(\frac{1.4 \cdot V_{ref}}{2^B} \right)^2 \cdot \exp(\frac{-T}{\tau_1}) \tag{12}$$

Next, we consider the integration phase shown in Fig.5 (b), where the 2^B unit capacitors are combined into C_S, and the 2^B DAC switches are neglected. The charge stored in sampling capacitor will be added to the integration capacitor and this charge current is supplied by OTA. So when the slew rate and gain bandwidth are not large enough, the settling error ε_2 will be produced. The statistical properties of V_S have been summarized in Table I. Then, according to Fig. 7, three types of settling conditions can happen in the integrator output during this phase, and the corresponding voltage errors of these three conditions are [14]

1. Linear settling: When the initial change rate of the integrator output voltage (V_o) is smaller than the OTA slew rate (SR).

$$\varepsilon_2 = a_1 \cdot |V_S| \cdot \exp(\frac{T}{2 \cdot \tau_2}),$$

$$\text{when} \quad 0 < |V_S| < \frac{1}{a_1} \cdot SR \cdot \tau_2 \tag{13}$$

2. Partial slewing: The initial change rate of V_o is larger than SR, but it gradually decreases until it is below the slew rate.

$$\varepsilon_2 = SR \cdot \tau_2 \cdot \exp(\frac{a_1 \cdot |V_S|}{SR \cdot \tau_2} - \frac{T}{2\tau_2} - 1),$$

$$\text{when} \quad \frac{1}{a_1} \cdot SR \cdot \tau_2 < |V_S| < (\frac{T}{2} + \tau_2) \frac{SR}{a_1} \tag{14}$$

3. Fully slewing: The initial change rate of V_o is larger than SR, and it maintains above SR in the $T/2$ interval.

$$\varepsilon_2 = a_1 \cdot |V_S| - SR \cdot \frac{T}{2}$$

$$\text{when} \quad |V_S| > \frac{SR}{a_1} (\frac{T}{2} + \tau_2) \tag{15}$$

where SR is the slew rate of OTA, and $\tau_2 = \frac{1 + 2\pi \cdot GBW \cdot R \cdot C_S}{2\pi \cdot GBW}$ [32] is the time constant in the integration phase, with GBW being the equivalent gain bandwidth in the integration phase. The capacitor loading in OTA output during this phase is heavier than in the sampling phase, and is [23]

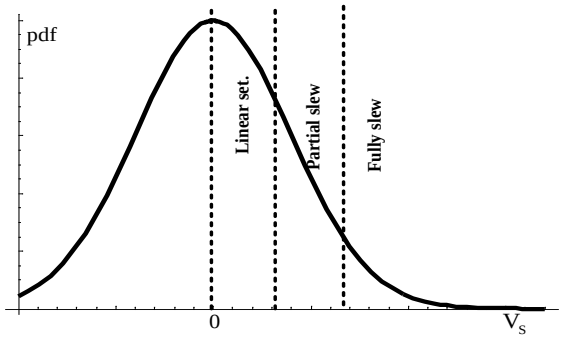


Fig. 7 Three types of settling conditions in integration phase

$$C_{L2} = 2C_S + C_L \cdot \frac{C_I + (2C_S)}{C_I} \tag{16}$$

the GBW is given by

$$GBW = \frac{\text{gm1}}{C_{L2} \cdot 2\pi} \tag{17}$$

In order to estimate settling noise in this phase, we must analyze the occurrence probability for each of the three conditions defined by (13)-(15). The probability of V_S in the linear settling region is

$$\Pr_{lin} = \int_0^{\frac{1}{a_1} \cdot SR \cdot \tau_2} \frac{2}{\sqrt{2\pi} \cdot \sigma_{VS}} \exp(\frac{-V_S^2}{2 \cdot \sigma_{VS}^2}) dV_S$$

$$= Erf[\frac{SR\tau_2}{\sqrt{2} a_1 \sigma_{VS}}] \tag{18}$$

Let $\varepsilon_{2\max}$ be the maximum linear settling error, and it can be obtained by substituting $|V_S| = \frac{1}{a_1} \cdot SR \cdot \tau_2$ into equation (13). Since V_S is approximately Gaussian, it is reasonable to assume that the linear settling error in (13) also has a Gaussian distribution in $(-\varepsilon_{2\max}, \varepsilon_{2\max})$. So the average linear settling noise power in the integration phase is approximately

$$P_{lin} \approx \frac{\varepsilon_{2\max}^2}{9} = \frac{1}{9} \left(SR \cdot \tau_2 \exp(\frac{-T}{2\tau_2}) \right)^2 \tag{19}$$

Before calculating the partial settling probability, we must check the possibility of this condition. If $\frac{1}{a_1} \cdot SR \cdot \tau_2 \geq 2V_{ref}$, a partial and fully slewing condition does not need to be considered. If $\frac{1}{a_1} \cdot SR \cdot \tau_2 < 2V_{ref}$, partial slewing probability is

$$\Pr_{par} = Erf[\frac{SR(T + 2\tau_2)}{2\sqrt{2} a_1 \sigma_{VS}}] - Erf[\frac{SR\tau_2}{\sqrt{2} a_1 \sigma_{VS}}] \tag{20}$$

Now we calculate noise power under the partial slewing condition. The pdf of V_S is

$$f_{par}(V_S) = \frac{1}{\Pr_{par}} \cdot \frac{2}{\sqrt{2\pi} \cdot \sigma_{VS}} \exp(\frac{-V_S^2}{2 \cdot \sigma_{VS}^2}) \tag{21}$$

$$\text{when} \quad \frac{1}{a_1} \cdot SR \cdot \tau_2 < |V_S| < (\frac{T}{2} + \tau_2) \frac{SR}{a_1} \cdot$$

The ε_2 here is no longer Gaussian distributed, and its pdf

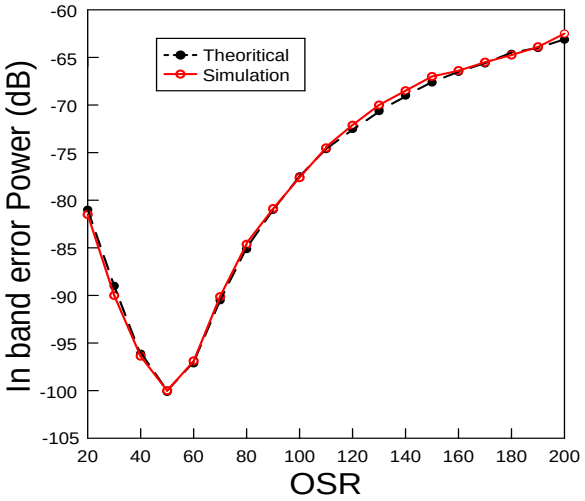


Fig. 8 Comparison of our theoretical result with behavior simulation result

can be computed from

$$f_{par}(\varepsilon_2) = f_{par}(V_S) \cdot \frac{dV_S}{d\varepsilon_2} \tag{22}$$

where $\frac{dV_S}{d\varepsilon_2}$ can be obtained by (14), and its value is $\frac{SR\tau_2}{a_1\varepsilon_2}$. Then the average noise power of partial slewing is

$$P_{par} = \int_{\varepsilon_2|V_S=\frac{1}{a_1}SR\tau_2}^{\varepsilon_2|V_S=(\tau_2+\frac{T}{2})\frac{SR}{a_1}} f_{par}(\varepsilon)\cdot\varepsilon^2 d\varepsilon$$

$$= \int_{V_S=\frac{SR\tau_2}{a_1}}^{V_S=\left(\tau_2+\frac{T}{2}\right)\frac{SR}{a_1}} f_{par}(V_S)\cdot\varepsilon_2{}^2 dV_S \tag{23}$$

Finally, we analyze the settling noise in a fully slewing condition using the same procedure. First, if $(\tau_2+\frac{T}{2})\frac{SR}{a_1} > 2V_{ref}$, this condition will never occur. If $(\tau_2+\frac{T}{2})\frac{SR}{a_1} < 2V_{ref}$, then the fully slewing probability is

$$\Pr_{ful} = Erf[\frac{2V_{ref}}{\sigma_{VS}}] - Erf[\frac{SR(T+2\tau_2)}{2\sqrt{2}a_1\sigma_{VS}}] \tag{24}$$

The pdf of V_S when $|V_S| > (\tau_2+\frac{T}{2})\frac{SR}{a_1}$ is

$$f_{ful}(V_S) = \frac{1}{\Pr_{ful}} \cdot \frac{2}{\sqrt{2\pi}\cdot\sigma_{VS}} \exp(\frac{-V_S{}^2}{2\cdot\sigma_{VS}{}^2}) \tag{25}$$

The pdf of ε_2 is

$$f_{ful}(\varepsilon_2) = f_{ful}(V_S)\cdot\frac{dV_S}{d\varepsilon_2} \tag{26}$$

So, the average noise power of fully slewing is

$$P_{ful} = \int_{\varepsilon_2|V_S=(\tau_2+\frac{T}{2})\frac{SR}{a_1}}^{\varepsilon_2|V_S=2V_{ref}} f_{ful}(\varepsilon)\cdot\varepsilon^2 d\varepsilon$$

$$= \int_{V_S=\left(\tau_2+\frac{T}{2}\right)\frac{SR}{a_1}}^{V_S=2V_{ref}} f_{ful}(V_S)\cdot\varepsilon_2{}^2 dV_S \tag{27}$$

The total average settling noise in the integration phase can be obtained by (18), (19), (20), (23), (24) and (27) as

$$P_{\varepsilon_2} = \frac{P_{lin}\cdot\Pr_{lin} + P_{par}\cdot\Pr_{par} + P_{ful}\cdot\Pr_{ful}}{OSR} \tag{28}$$

In order to verify the result in (28), we use SIMULINK

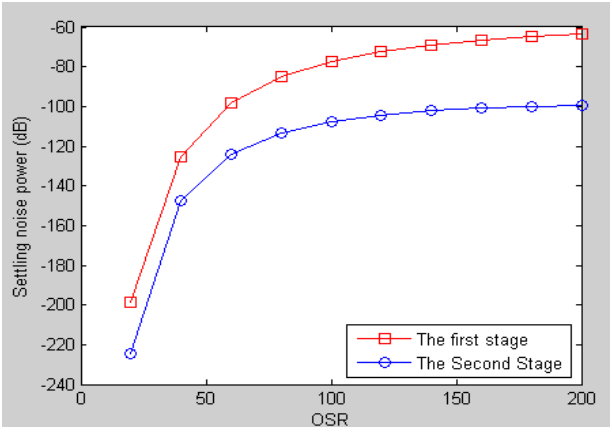


Fig. 9 Settling noise power for the first and the second stage integrators vs. *OSR*

to build a second-order ΣΔ modulator with a 4-bit quantizer. The behavioral settling model in [14] is used. We assume that $a_1 = 0.5$, $R = 300\Omega$, $C_S = 1.7$ pF, $GBW = 100$ MHz, $f_B = 300$ kHz and $SR = 100$ V/μs, and use a 300 kHz sinusoidal input signal. In an ideal behavior simulation with a sinusoidal input, the error ε_2 can not be observed at modulator output, because ε_2 is highly correlated with V_S, so that ε_2 is compensated in the steady state by the integrator. However, adding a small noise to the input signal can eliminate the effects of feedback and integration. The theoretical noise power is obtained by adding the theoretical settling noise power from (28) to the theoretical quantization noise power. The simulated and theoretical noise powers are both shown in Fig. 8 vs. *OSR*. The two lines are closely related. When *OSR* < 50, quantization noise dominates. When *OSR* > 50, settling noise dominates. Notice that increasing *SR* and *GBW* will reduce settling noise and increase *SNR*, but will also increase analog power consumption and the design challenges.

In conclusion, if ε_2 is independent of V_S, our settling noise model is correct and accurate. This model can be conservative if it is use in the design optimization discussed in Section III and IV, resulting in larger *SR* and *GBW*. However, the *SR* and *GBW* obtained from our design are still much smaller than those used in [5], as is discussed in Section IV. In addition, if we take into account the settling distortion issue (see Section IV and Appendix A), this conservativeness may be indeed needed.

C.1 Settling error of second stage

In integration phase, the settling error power for the second stage integrator is much smaller than that in the first stage, so generally it is not considered. This noise source appears at D2 in Fig. 10. The standard deviation of V_s for the second stage can be approximated by

$$\sigma_{VS} \approx \frac{1.06\cdot|V_{ref}|}{2^B} \tag{29}$$

In general, the design specifications for the 1st and 2nd stage integrators are different, so the overall settling error power for the 2nd stage integrator $P_{\varepsilon_2\_2nd}(overall)$ can be obtain by substituting it's specifications into (16)~(27). Due to noise shaping, the total noise power in signal

bandwidth is

$$P_{\varepsilon 2\_2nd} = \int_{-f_{in}}^{f_{in}} \frac{P_{\varepsilon_2\_2nd}(overall)}{f_S} \cdot 4Sin^2\left(\frac{f}{f_S}\pi\right) df \qquad (30)$$

where $4Sin^2\left(\frac{f}{f_S}\pi\right)$ is the noise transfer function for D2 [40]. The larger the OSR, the more effective noise shaping is. For the case that 1st and 2nd stage integrators are identical, Fig. 9 compares 1st and 2nd stage settling noise powers vs. *OSR*, which shows that the second-stage settling error is at least 22 to 36 dB less than that of the first stage.

D. Multi-bit DAC noise

There are several advantages in using a multi-bit structure, which are discussed in [33, 34]. Due to CMOS process variations, there can be mismatches in the 2^B unit capacitors C_u of a *B*-bit DAC shown in Fig. 4. Assume that each unit capacitor distribution is Gaussian [35] around a nominal value. Let the normalized capacitance be

$$c_i = \frac{C_i}{\sum_{k=1}^{2^B} C_k}, \quad 1 \le i \le 2^B \qquad (31)$$

where C_i is the capacitance of the ith unit capacitor. Define the deviation of c_i as $e_i = c_i - c_m$, where

$$c_m = \frac{\sum_{i=1}^{2^B} c_i}{2^B} \qquad (32)$$

Then voltage error caused by unit capacitor mismatches is given by [23]

$$e_{dac}(k) = \mathrm{V}_{ref}\left(\sum_{i=1}^{x(k)} e_i - \sum_{i=x(k)+1}^{2^B} e_i\right) \qquad (33)$$

where $x(k)$ represents the number of 1's in the feedback thermometer code at the time step k. The $e_{dac}(k)$ can be treated as an additive Gaussian noise in the ΣΔ modulator feedback path, the variance of which is

$$\begin{aligned}\sigma^2[e_{dac}] &= V_{ref}{}^2\left(x(k)\cdot\sigma^2[e_i] + (2^B - x(k))\cdot\sigma^2[e_i]\right)\\ &= V_{ref}{}^2 \cdot 2^B \cdot \sigma^2[e_i]\\ &= V_{ref}{}^2 \cdot 2^B \cdot \sigma_{cap}{}^2 \end{aligned} \qquad (34)$$

where σ_{cap} is the standard deviation of unit capacitor. Assuming the $e_{dac}(k)$ is also white, the average DAC noise power at the modulator output becomes

$$P_{dac} = \frac{1}{OSR} \cdot V_{ref}{}^2 \cdot 2^B \cdot \sigma_{cap}{}^2 \qquad (35)$$

In order to reduce DAC error due to unit capacitor mismatch, several techniques have been proposed. The most efficient among these is the Data Weighted Averaging (DWA) [36], and it is shown in [37] that the DWA effect is a first-order noise shaping of the DAC noise. If the DWA is employed, the average DAC noise power at the modulator output is modified to be

$$P_{dac}(DWA) \cong V_{ref}{}^2 \cdot 2^B \cdot \sigma_{cap}{}^2 \cdot \frac{\pi^2}{3 \cdot OSR^3} \qquad (36)$$

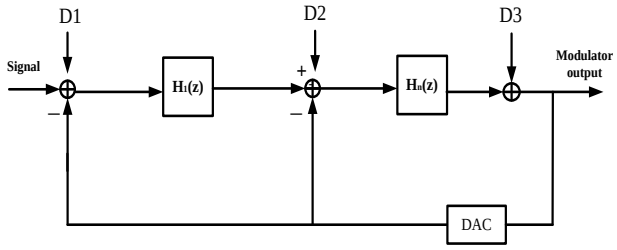


Fig. 10 Main nonidealities sources in the sigma delta modulator

Equations (33) and (34) will be used to estimate the DAC noise power in the optimization process.

E. Clock Jitter Effects

As both the signal bandwidth and the required output SNR increase, clock jitter problems become more obvious. Jitter is usually defined as a random variation in clock signal period around the ideal value, and the value of jitter can be reasonably assumed as a Gaussian random variable with zero mean and standard deviation σ_{jit}. If there is some variation in clock high time, the input signal will be sampled at the wrong instant and receive a consequent voltage error. For a sinusoidal input signal with maximum amplitude A_{in} and frequency f_{in}, if it is sampled by a clock which has a jitter variation, then the voltage error is [2]

$$\Delta V \cong 2\pi \cdot f_{in} \cdot A_{in} \cos(2\pi \cdot f_{in} \cdot t)\Delta T \qquad (37)$$

where ΔT is the variation of clock period with standard deviation σ_{jit}. Then the jitter noise power becomes

$$P_{jitter} = \frac{(2\pi \cdot f_{in} \cdot A_{in})^2}{2} \cdot \frac{\sigma_{jit}{}^2}{OSR} \qquad (38)$$

We consider the worst case in this work. That is, f_{in} and A_{in} are replaced by f_B and V_{ref} respectively. More discussions about tolerable σ_{jit} will be given in the next section.

We summarize the nonideality modeling as follows. The leakage noise due to finite OTA gain can be considered as an additional quantization noise, so the total quantization noise will be higher than theoretical quantization noise, appearing at D3 in Fig. 10. All other nonidealities in the first stage are modeled at D1 in Fig. 10, because we have modeled them as input-referred noise in the integrator input.

F. Relative Power Model

In order to understand how ΣΔ modulator power consumption is related to different circuit parameters, we must derive the power dissipation equation. Some derivations of this are based on the results presented in [23, 24, 25]. It is difficult to estimate real system level power consumption, so our goal is not to estimate the absolute value of the power, but to find how power changes with circuit parameters, it is called the relative power consumption. Typically, ΣΔ ADC power consumption is categorized into analog and digital parts. The power dissipation in the quantizer is also considered. We analyze

the analog part first. The analog power dissipation in a $\Sigma\Delta$ modulator is mainly from OTA, and is proportional to the product of several parameters:

$$POW_{OTA} \sim k_{OTA} \cdot V_{DD} \cdot \pi \cdot C_{L2} \cdot GBW \quad (39)$$

where k_{OTA} is the number of current branches of OTA and V_{DD} is the power supply. The k_{OTA} depends on the topology of OTA. The first integrator is the most important in terms of noise. Hence, all succeeding integrators are normally scaled down progressively to reduce the power consumption and die area. Consider that the sum of the relative scaling factors used in all the integrators of the $\Sigma\Delta$ is $k_{\Sigma\Delta}$. Then the analog power consumption equals $k_{\Sigma\Delta} \cdot POW_{OTA}$, where $k_{\Sigma\Delta}$ is proportional to the order n of the $\Sigma\Delta$ modulator. Assuming that the scaling factor is 0.5, then from (39), the total analog power consumption is :

$$POW_{analog} \cong k_{\Sigma\Delta} \cdot POW_{OTA} \sim \left(\sum_{i=0}^{n-1} (0.5)^i \right) \cdot k_{OTA} \cdot V_{DD} \cdot \pi \cdot C_{L2} \cdot GBW \quad (40)$$

Since the analog power consumption is related to n, V_{DD}, C_{L2} and GBW, they are important circuit parameters to be determined in the design flow.

Next, we discuss digital power consumption. Digital power consumption is mainly from MOS switch operation, and is proportional to the product of another set of parameters:

$$POW_{SW} \sim n \cdot 2^B \cdot C_{Switch} \cdot V_{DD}{}^2 \cdot 2 \cdot f_B \cdot OSR \quad (41)$$

where $2 \cdot f_B \cdot OSR$ is equal to the sampling frequency, and C_{Switch} is the total gate capacitance of switches. The value of C_{Switch} is inversely proportional to the switch-on resistance R [38], so we define the relative digital power as

$$POW_{digital} \sim n \cdot 2^B \cdot \frac{1}{R} \cdot V_{DD}{}^2 \cdot f_S \quad (42)$$

Next we discuss quantizer power consumption. In the multi-bit ADC, a simple power estimation formula for Nyquist ADC [25] is

$$P_{quantizer} = \frac{V_{DD}{}^2 \times L_{\min} \times (f_S + f_B)}{10^{(-0.1525B+4.838)}} \quad (43)$$

where $L_{\min}$ is the minimum channel length of the technology associated. According to the above discussion, the total relative power is defined as

$$Power = K_1 \times POW_{analog} + K_2 \times POW_{digital} + P_{quantizer} \quad (44)$$

where K_1 and K_2 are adjusted to make *Power* (in mW) comparable in magnitude with real power dissipations. After comparing with power measurements reported in [5, 11], we set $K_1 = 0.03651$ and $K_2 = 3.6877 \times 10^{-10}$. Both [5] and [11] are based on 0.18-μm CMOS technology. For other CMOS technologies, the K_1 and K_2 may be set to other appropriate values.

Dynamic element matching (DEM) [36, 37, 47] is based on scrambling the use of the unit elements in a multi-bit DAC to average out nonlinearity and turn distortion into noise. In general, the DEM logic grows exponentially in complexity, size, and power dissipation as the internal quantizer bit increases. And the power consumption of 120DEM depends on CMOS technology. Due to many possible variations in DEM designs, we do not try to calculate the power consumption for any specific type of DEM scheme. Instead, picking a medium value, we assume DEM power is $0.6 \times Power$ if DEM is employed.

	B ↑	OSR ↑	n ↑	R ↑	GBW ↑	C_S ↑	SR ↑
P_Q (1)	↓	↓	↓	—	—	—	—
P_{AV} (1)	↓	↓	↓	—	—	—	—
$P_{\varepsilon 1}$ (12)	↓	↑	—	↑	—	↑	—
$P_{\varepsilon 2}$ (28)	↓	↑	—	—	↓	↑	↓
P_{dac} (35)	↑	↓	—	—	—	—	—
P_{jitter} (38)	—	↓	—	—	—	—	—
P_{sw} (2)	—	↓	—	—	—	↓	—
P_{OTA} (6)	—	↓	—	—	↑	—	—
P_{ref} (7)	—	↓	—	↓	↓	↓	—
Power (44)	↑	↑	↑	↓	↑	↑	↑

TABLE II Summary of noise-power and power-rating variations when design parameters increase

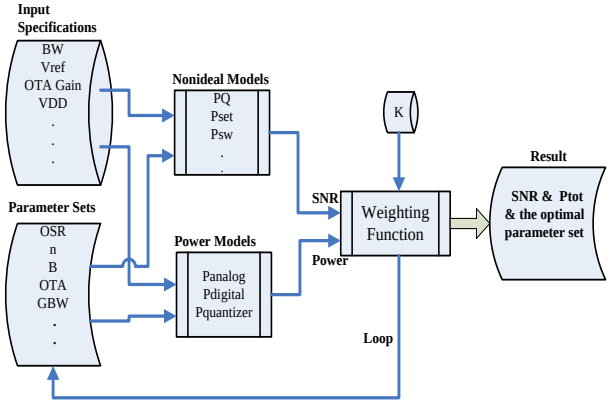


Fig. 11 Proposed optimization algorithm for the $\Sigma\Delta$ modulator design

III. The Design Optimization Scheme

Power and nonideality models derived in section II are employed to propose a design optimization algorithm, to search for optimal parameter combinations. Before the discussions, we formally define the peak *SNR* at $\Sigma\Delta$ ADC output as

$$SNR = \frac{(2A_{in})^2 / 2}{P_Q + P_{AV} + P_{\varepsilon 1} + P_{\varepsilon 2} + P_{dac} + P_{jitter} + P_{sw} + P_{OTA} + P_{ref}} \quad (45)$$

Table II summarizes the facts from models in section II. Table II shows qualitatively how noise and power are affected when a particular design parameter increases, and it reveals that the $\Sigma\Delta$ ADC design task is very complex. Basically we identify *B*, *OSR*, *n*, *R*, *GBW*, C_S and *SR* as the optimization process design parameters.

In the following we propose an design optimization algorithm to help designers reach an optimal design quickly. It is based on the error and power models described in section II. The complete flow of the

optimization methodology is shown in Fig. 11. The input signal bandwidth (Hz) and the output signal SNR (dB) are treated as design specifications. We modify the figure-of-merit (FOM) [40] function by multiplying a variable *K* to the *SNR* term of FOM, to become our weighting function.

$$\mathrm{WF} = K \cdot SNR_{\mathrm{dB}} + 10\log\left(\frac{f_B}{Power}\right) \quad (46)$$

The design optimization algorithm basically searches through the entire parameter space to find the set of design parameters which maximize the Weighting Function. By maximizing the Weighting Function we can increase *SNR* (45) and reduce *Power* (44) at the same time.

The constant *K* serves as the relative weighting between *SNR* and *Power*. Typically, if we prefer high resolution designs, we set *K* higher and *SNR* plays a more important role than *Power*; on the other hand, if we prefer low power designs, we can set *K* lower. After an design optimization process, the set of design parameters resulting in the largest Weighting Function value is the outcome and is evaluated. If not acceptable, the *K* is adjusted and the design optimization process is repeated. The parameter searching space is specified to be

- *OSR* : 8 ~ 128
- *B* : 1 ~ 6 (if > 3, DEM is required)
- *n* : 1 ~ 3
- *R* : 100 Ω ~ 300 Ω
- *GBW* : 50 MHz ~ 500 MHz
- *SR* : $50\,{}^{V}\!/_{\mu S}$ ~ $500\,{}^{V}\!/_{\mu S}$
- C_S : 1 pF ~ 10 pF

The parameters σ_{cap} and V_{ref} depend on the technology, so they are set before the design optimization. The tolerable value of jitter standard deviation σ_{jit} can be specified after the optimization process. During the design optimization process, the gain coefficients a_i are specified according to the rules provided in [43].

IV. Simulation Results

In order to demonstrate the accuracy and practicability of our method, we apply it to two published design cases [5, 28]. In addition, we compare our method with existing behavior-simulation-based optimization schemes [48, 49].

A. ΣΔ *ADC for ADSL-CO Applications*

To compare with the design of [5], the design optimization algorithm uses the same specifications as those in [5]. They are:

- Peak *SNR* : 82 dB
- Signal bandwidth : 276 kHz

The OTA gain A is set at 60 dB and the V_{ref} is set at 0.9 V for a 1.8 V power supply in 0.18-μm CMOS technology. The matching of capacitor σ_{cap} is set at 0.04% for the MIM capacitance. The results published in [5] and those obtained from our methodology are all listed in Table III, which includes three design optimization results corresponding to *K*=0.3, *K*=0.6, and *K*=0.7. From Table III, when *K*=0.6, the result of *SNR* = 83.3 dB satisfies the specification, although the *Power* = 3.7 mW is higher than *Power* = 3.0 mW when *K*=0.3. The results from higher *K* are also reported. When *K*=0.7, the power consumption is dramatically larger at 26.2 mW, due to the fact that the DEM is employed and *B* is larger. We choose the case *K*=0.6 (with *SNR*=83.3) as our design. The *SNR* generated from the SIMULINK behavior simulation is also included in Table III.

circuit parameters	**in [5]**	***K*=0.3**	***K*=0.6**	***K*=0.7**	**Unit**
OSR	96	40	50	60	-
B	3	2	2	4	-
n	2	2	2	2	-
R	300	300	300	300	Ω
C_S	1.7	1	1	2	pF
C_{L2}	7.2	5.8	5.8	7.8	pF
GBW	**400**	70	**90**	150	MHz
SR	**500**	120	**160**	50	V/μs
σ_{jit}	15	15	15	15	Ps
SNR	82.8	81.5	83.3	96.7	dB
SNR(SIMULINK)	82.3	80.8	83.1	95.5	dB
Power	15	3.0	3.7	26.2	mW

TABLE III Comparisons of our design results with those in [5]

Noise	in [5]	K =0.3	K =0.6	K =0.7
P_Q	- 109.8 dB	- 84.9 dB	- 89.8 dB	- 105.8 dB
P_{AV}	-141.1dB	- 123.6 dB	- 126.5 dB	- 141.0 dB
$P_{\varepsilon 1}$	- 196.5 dB	- 681.7 dB	- 551.5 dB	- 258.4 dB
$P_{\varepsilon 2}$	- 119.3dB	- 103.9dB	- 104.5dB	- 120.0 dB
P_{sw}	- 96.9 dB	- 90.8 dB	- 91.8 dB	- 95.6dB
P_{ref}	- 114.7dB	- 101.0dB	- 103.1 dB	- 109.1 dB
P_{OTA}	- 117.0 dB	- 110.9 dB	- 111.9 dB	- 115.7 dB
P_{dac}	- 80.8dB	-81.4dB	- 82.3dB	- 105.6dB
P_{total}	- 80.7dB	- 79.4 dB	-81.2dB	-94.6dB

TABLE IV The corresponding noise powers for the design parameters listed in Table III

	Ref [5]	***K*=0.3**	***K*=0.6**	***K*=0.7**	**Unit**
POW_{analog}	64.6	6.65	8.55	28.5	-
$POW_{digital}$	3.1×10^{10}	6.4×10^{9}	8.02×10^{9}	3.85×10^{10}	-
$POW_{quantizer}$	1.29	0.38	0.48	1.15	mW

TABLE V List of the details of power consumption

The design of [5] is also listed in Table III. The *SNR* and *Power* of [5] listed in Table III are computed from our models. The *SR* and *GBW* used in [5] are considerably larger than those of our design. According to Table Ⅷ in the Appendix A, the values *SR* = $500\,{}^{V}\!/_{\mu S}$ and *GBW* = 400MHz are barely enough for *OSR* = 8, but are more than adequate for *OSR* = 16. Since the *OSR* in [5] is designed to be 96, the *SR* and *GBW* values used in [5] are too large

compared with the minimum required values at *SR* = $90^{V}/_{\mu S}$ and *GBW* = 40MHz listed in Table Ⅷ, resulting in power consumption four times that of our design (15mW vs. 3.7mW). The *SR* and *GBW* in our design are adequate, with (*SR*, *GBW*) = (160, 90) compared with the minimum required (110, 60) listed in Table Ⅷ.

Table IV shows the corresponding noise powers for the four design cases shown in Table III. In the design of [5], and in our designs for *K*=0.6, the dominating noise power is P_{dac}. Our optimization process may help to distribute noise power more evenly among different noise categories, resulting in a larger gap between P_{dac} and P_{total}, where P_{total} is the sum of in band noise powers. The gap between P_{dac} and P_{total} from [5] is very small. Our optimization algorithm may also help designers consider less aggressive design parameters first, e.g., setting *B* = 2 instead of 3. When *K*=0.7, the optimization algorithm sets *B* to be 4, so the DEM technique is employed, and DAC noise is suppressed to -105.6 dB. Accordingly the P_{sw} at -95.6 dB becomes the dominating noise power. Finally, we want to report a case not listed in Tables III and IV. Suppose we change our rule to enable DEM when *B* is equal to or larger than 3. Then, for the case *K*=0.6, the algorithm sets *B* to be 3 (from 2), P_{dac} is reduced to -111.2 dB (from -82.3 dB), and *SNR* is raised to 97.2 dB (from 83.3 dB). But the power consumption is increased to 16.9 mW (from 3.7 mW).

Table V lists the power consumption details. From (38), we can see that the POW_{analog} is proportional to the *GBW* and C_{L2}. The C_{L2} (16) is proportional to the sampling capacitance C_S. From Table III, we can see that the *GBW* of [5] is larger than that of *K*=0.3, *K*=0.6 and *K*=0.7 and C_S of [5] is larger than that of *K* = 0.3 and *K* = 0.6 (almost the same with *K* = 0.7). Hence, the POW_{analog} of [5] is the largest among the four cases. From (40), we can see that the $POW_{digital}$ is proportional to the 2^B and *OSR*. It is also inversely proportional to the on-resistance *R*. The quantizer power $POW_{quantizar}$ (41) is related to *OSR* and *B*. The larger the *OSR* and *B* are, the larger the quantizer power $POW_{quantizar}$. In Table III the *Power* of [5] is four times larger compared with that of *K*=0.6. This is due to the design of [5] employs larger *GBW*, *OSR*, C_S, and *B*, resulting in larger POW_{analog}, $POW_{digital}$ and $POW_{quantizar}$.

B. ΣΔ *ADC for Broadband Applications*

To compare with the design of [28], the design optimization algorithm uses the same specifications as those in [28]. They are:

- Peak *SNR* : 95 dB
- Signal bandwidth : 1.25 MHz

The DAC architecture in [28] (shown in Fig. 12) is different from the one shown in Fig. 1. Therefore, the noise powers P_{sw}, P_{OTA} and $P_{\varepsilon 1}$ must be modified, and

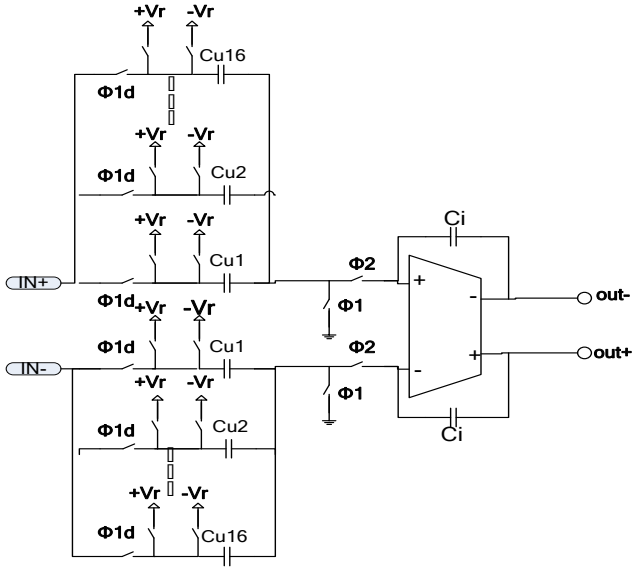


Fig. 12 The DAC architecture in [28]

circuit parameters	in [28]	*K*=0.3	*K*=0.6	*K*=1	Unit
OSR	24	20	28	40	-
B	4	3	3	3	-
n	3	3	3	3	-
R	220	300	300	200	Ω
C_{μ}	200	225	225	300	fF
C_{L2}	8.5	5	5	6.7	pF
GBW	220	120	240	400	MHz
SR	145	75	150	250	V/μs
σ_{jit}	9	9	9	9	Ps
SNR	94.1	89.7	94.5	98	dB
SNR(SIMULINK)	94.6	90.3	95.8	99.1	dB
Power	300	118	167	303	mW

TABLE Ⅵ Comparisons of our design results with those in [28]

Noise	in [28]	K =0.3	K =0.7	K =1
P_Q	-104 dB	-92.5 dB	-102.7 dB	-113.6 dB
P_{AV}	-170 dB	-160 dB	-168 dB	-175.7 dB
$P_{\varepsilon 1}$	-1680 dB	-1314 dB	-948 dB	-755 dB
$P_{\varepsilon 2}$	-101 dB	-94.8dB	-104.2 dB	-104 dB
P_{sw}	-96.6 dB	-93.4 dB	-94.8 dB	-97.6 dB
P_{ref}	-100 dB	-93 dB	-97.4 dB	-102 dB
P_{OTA}	-119.3 dB	-116 dB	-117.5 dB	-120.3 dB
P_{dac}	-94.1 dB	-95.3 dB	-99.7 dB	-104 dB
P_{total}	-90.6 dB	-86.4dB	-90.9 dB	-94.2 dB

TABLE Ⅶ The corresponding noise powers for the design parameters listed in Table Ⅵ

the modifications are summarized in Appendix B. Other noise powers forms are the same as those in Sec. Ⅱ, except that C_S is replaced by $2^B \cdot C_u$.

From TABLE Ⅵ, when K=1, *SNR*=96 dB satisfies the

specification in [28]. Compared with the design in Case A, several points are worth mentioning. Although our *GBW* and *SR* in Case A are much smaller than the published ones [5], they are larger than the published ones [28] in Case B. This helps to avoid the impression that our method produces extreme results. Table Ⅳ shows that the dominating noise power in Case A is P_{dac}, while Table Ⅶ shows that in Case B the dominating power is P_{sw}. A reason is that the DEM is employed in Case B, but not in Case A.

C. *Comparisons with Existing Optimization Schemes*

Behavioral simulation based optimization strategy is popular for ΣΔ ADC design [48, 49]. The comparisons between our method and general behavioral simulation methods are summarized as follows.

1. Our method can be hundreds of times faster. We compare the CPU times required for each method to generate the SNR for a specific point in the parameter space (Measurement platform: Intel Pentium D, 2.8GHz CPU). To make a fair comparison, both methods are implemented under Matlab-Simulink environment. For our approach, the SNR in (45) is computed by a Matlab program (originally implemented in *Mathmatica*). The CPU time is 62.5 ms. For behavior simulation approach, a 16384 point simulation is run under Simulink, and the total CPU time is 13.01 seconds, Our method is 208.2 times faster.

2. The optimization result from behavior simulations provides only the total noise power, while our method can generate each individual noise power as is listed in Table IV and Table Ⅶ, which provides greater insights and can serve several practical purposes. For example, suppose the design objective is not met even after the optimization process. The simulation approach might shed little clue about how things can be tackled. On the other hand, our result would indicate which noise power is the dominating one, and a different technology can be adopted to reduce that particular noise.

3. The disadvantage of our method is low flexibility, because equations may be modified every time when the topology is changed. In contrast, it is generally straightforward to simulate various ΣΔ modulator architectures by properly linking building blocks into appropriate forms.

V. Conclusion

The main contributions of this work are described in the following. First, a settling error model of the switched capacitor integrators in ΣΔ modulators is constructed using statistical analysis. This model considers settling errors in both the sampling and integration phases, represented in noise-power form. We also derive the DAC noise-power model. Additionally, we make modifications to existing noise-power models of other noises, particularly to thermal noise models. The noise-power models of all major noises and errors are established in Section II, and the SNR is defined in (45) accordingly. Second, based on nonideality models and the relative power model, we propose an optimization algorithm in Section III. In contrast to the complexity and difficulty encountered in the conventional ΣΔ modulator design approach, this algorithm can completely and efficiently search the entire design parameters space to find the parameter set which satisfies the specifications, while achieving the lowest power consumption. Third, the complete models allow for analytical evaluation of design results, whether they are generated from our algorithm or designed elsewhere. For example, information provided in Table IV and V can reveal which noise or power is the dominating factor. Then, the models in Section II can help find design parameters behind the dominating factor. Fourth, our optimization method can be hundreds of times faster than existing behavioral simulation based approaches.

This paper works on optimization of SNR, not SNDR. For radio and communication applications, maximize SNDR becomes an important issue. We are currently working on creating a complete set of nonlinear distortion models, so that SNDR optimization can be realized.

Appendix A: Settling Distortion Model

In a ΣΔ modulator, nonlinear distortions can be categorized into op-amp gain nonlinearity distortion [18, 23, 46], settling distortion [18, 42, 46], nonlinear capacitances distortion [18, 23], quantizer nonlinearity distortion [34], nonlinear switch resistance distortion [23, 32] and DAC distortion [34, 37, 44, 45]. It can be verified that settling distortion is the sole distortion which can be significantly affected by op-amp slew rate (*SR*) and gain-bandwidth (*GBW*). There was a great effort in [46] to model settling distortion. However the result in [46] reached a wrong conclusion, and it showed little insight about how *SR* and *GBW* are quantitatively related to settling distortion. In this appendix, we provide a comprehensive model for settling distortion. This model is used in section IV to explain why the *SR* and *GBW* in [5] are too large, but the *SR* and *GBW* obtained in our design are adequate.

Consider the integrator operates in the integration phase. As discussed in section II, there are three settling conditions depending on the absolute value of V_S.

1. Linear settling $\left(|V_S| < \frac{1}{a_1}\cdot SR\cdot\tau_2\right)$:

We can represent integrator output voltage during the *n*th integration interval as

$$V_o(t) = V_o(nT-T) + a_1 V_S\left(1-e^{\frac{-(t-nT+\frac{T}{2})}{\tau_2}}\right), \quad nT-\frac{T}{2} < t < nT \tag{47}$$

2. Partial slewing $\left(\frac{1}{a_1}\cdot SR\cdot\tau_2 < |V_S|\right)$:

$$V_o(t) = V_o(nT-T) + SR\cdot\left(t_0 - nT + \frac{T}{2}\right) + \left[a_1 V_S - SR\cdot\left(t_0 - nT + \frac{T}{2}\right)\right]\left(1-e^{\frac{-(t-t_0)}{\tau_2}}\right), \quad t > t_0 \tag{48}$$

where t_0 is the time instant when V_o rate becomes less than *SR*. The full slewing case is not considered here

because it is not significant. Note that (47) and (48) at end of each integration interval can be rewritten as

$$\begin{aligned} V_o(nT) &= V_o(nT-T) + a_1 V_S\left(1 - e^{-\left(\frac{T}{2\tau_2}+1\right)} \cdot e\right) \\ &= V_o(nT-T) + a_1 V_S(1-\beta \cdot e), \quad |V_S| \le V_L \\ V_o(nT) &= V_o(nT-T) + a_1 V_S\left[1 - \frac{SR\tau_2}{a_1 V_S} \cdot e^{-\left(\frac{T}{2\tau_2} - \frac{a_1|V_S|}{SR\tau_2}+1\right)}\right] \\ &= V_o(nT-T) + a_1 V_S\left[1 - \frac{V_L}{V_S} \cdot \beta e^{|V_S|/V_L}\right], |V_S| > V_L \end{aligned} \tag{49}$$

where $\beta = e^{-(T/(2\tau_2)+1)}$ and $V_L = SR\tau_2 / a_1$.

Let

$$g_i(V_S) = \begin{cases} a_1(1-\beta e) \ ; & |V_S| \le V_L \\ a_1\left(1 - \frac{V_L}{V_S}\beta e^{|V_S|/V_L}\right) ; & |V_S| > V_L \end{cases} \tag{50}$$

which is the integrator gain. Assume that $g_i(v)$ can be approximated by

$$p(v) = a_1 \cdot (\alpha_1 + \alpha_3 v^2 + \alpha_5 v^4) \tag{51}$$

We use the least square method to determine the coefficients α_1, α_3 and α_5 such that the cost function

$$\begin{aligned} q &= \sum_{j=1}^{n}\left[g_i(x_j) - p(x_j)\right]^2 \\ &= \sum_{j=1}^{n}\left[g_i(x_j) - a_1\alpha_1 - a_1\alpha_3 x_j^{\ 2} - a_1\alpha_5 x_j^{\ 4}\right]^2 \end{aligned} \tag{52}$$

is minimized over a specific interval, and the solution is found to be

$$\begin{bmatrix} \alpha_1 \\ \alpha_3 \\ \alpha_5 \end{bmatrix} = \begin{bmatrix} \frac{225}{64\cdot V_h} & \frac{-525}{32\cdot V_h^{\ 3}} & \frac{945}{64\cdot V_h^{\ 5}} \\ \frac{-525}{32\cdot V_h^{\ 3}} & \frac{2205}{16\cdot V_h^{\ 5}} & \frac{-4725}{32\cdot V_h^{\ 7}} \\ \frac{945}{64\cdot V_h^{\ 5}} & \frac{-4725}{32\cdot V_h^{\ 7}} & \frac{11025}{64\cdot V_h^{\ 9}} \end{bmatrix} \begin{bmatrix} \int_0^{V_L}(1-\beta e)\,dV_S + \int_{V_L}^{V_h}(1-\frac{V_L}{V_S}\beta e^{|V_S|/V_L})\,dV_S \\ \int_0^{V_L}(1-\beta e)\cdot V_S^{\ 2}\,dV_S + \int_{V_L}^{V_h}(1-\frac{V_L}{V_S}\beta e^{|V_S|/V_L}) V_S^{\ 2}\,dV_S \\ \int_0^{V_L}(1-\beta e)\cdot V_S^{\ 4}\,dV_S + \int_{V_L}^{V_h}(1-\frac{V_L}{V_S}\beta e^{|V_S|/V_L}) V_S^{\ 4}\,dV_S \end{bmatrix} \tag{53}$$

where V_h is the distribution range of the first integrator input V_S. The amplitudes of the third and fifth harmonics of the modulator output are:

$$A_3 \cong \frac{|\alpha_3| A_{VS}^3}{4} \quad ; \quad A_5 \cong \frac{|\alpha_5| A_{VS}^5}{16} \tag{54}$$

where A_{VS} is the amplitude of V_S. However, in [46], A_{in} instead of A_{VS} is employed in (54), where A_{in} is the amplitude of a sinusoidal modulator input signal. It is intuitively clear that using A_{in} is not correct, and our simulation shows that (54) is correct and precise. Next we are to obtain an expression for A_{VS}.

$$V_S(z) = X(z) - Y(z) \tag{55}$$

In a second-order ΣΔ modulator, modulator output signal *Y(z)* is the time delay version of *X(z)* plus high-pass filtered (noise shaped) quantization noise E(z). Therefore,

$$Y(z) = z^{-2}X(z) + (1-z^{-1})^2 E(z) \tag{56}$$

Combining (55) and (56), $V_S(z)$ can be written as

$$V_S(z) = X(z)\left[1 - z^{-2}\right] - (1-z^{-1})^2 E(z) \tag{57}$$

Ignoring the quantization noise and taking the inverse z-transform, one obtains

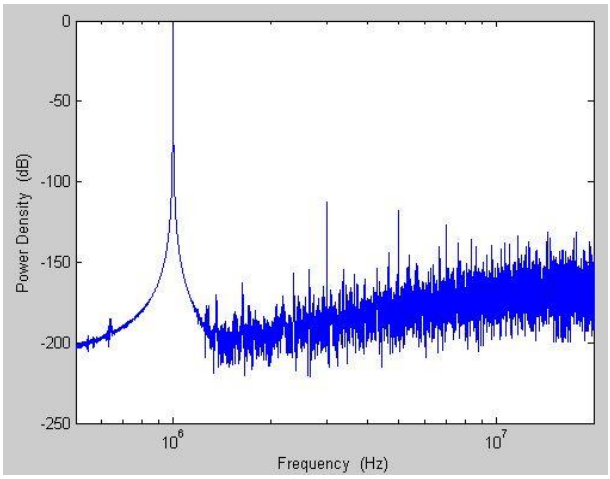


Fig. 13 Output spectrum of a second-order sigma-delta modulator with harmonic distortion

$$\begin{aligned} V_S(t) &= x(t) - x(t-2T)u(t-2T) \\ &= A_{in}\sin(\omega t) - A_{in}\sin(\omega(t-2T))\cdot u(t-2T) \end{aligned} \tag{58}$$

Then, the amplitude of V_S can be obtained as

$$A_{VS} = V_S(2T) = A_{in}\sin(\omega \cdot 2T) \cong 2A_{in}\cdot\omega\cdot T \tag{59}$$

Note that A_{VS} is not related to quantizer bit number *B* which can only affect the level of noise floor *E*(ω). The result (59) has been verified by behavior simulation under different *B* values.

In order to verify the result in (54), we use SIMULINK to build a second-order ΣΔ modulator with a multi-bit quantizer. The behavioral settling model in [14] is employed. We assume that *SR* = 70 $V/\mu S$, *GBW* = 100MHz, *R* = 300Ω, *OSR* = 16, f_B = 1MHz and C_S = 2pF, and a 1MHz sinusoidal input signal is used. After performing FFT to the output data of the ΣΔ modulator, we obtain the simulated PSD (Power Spectrum Density) which is shown in Fig. 13. It shows that HD3 is -112.5dB and HD5 is -117.5dB. The theoretical harmonic powers calculated from (53) and (54) are HD3 = -112.4dB and HD5 = -117.3dB. The simulated and theoretical results are very close, and this confirms that our settling distortion model is reasonably precise.

In order to provide insight on how settling distortions are related to circuit and system parameters, we further analyze the 3rd and 5th harmonic powers as follows:

$$\begin{aligned} HD3(dB) &= 20\log\left(\frac{1}{\sqrt{2}}\left(\frac{|\alpha_3|A_{VS}^3}{4}\right)\right) \\ &= 20\log|\alpha_3| - 60\log OSR + 30.095 \\ HD5(dB) &= 20\log|\alpha_5| - 100\log OSR + 48.15 \end{aligned} \tag{60}$$

From (60) we can see that *OSR* can effectively influence settling harmonic powers. The (53) reveals that α_3 and α_5 are functions of *T*, *GBW*, *R*, C_S and *SR*. Using the parameters designed in Section IV with f_S = 50MHz, *R* = 300ohm, C_S = 2pF, and setting *GBW* and *SR* at *GBW* = 250MHz and *SR* = 250 $V/\mu S$, we plot $20\log|\alpha_3|$ vs. *SR* in Fig. 14 and $20\log|\alpha_3|$ vs. *GBW* in

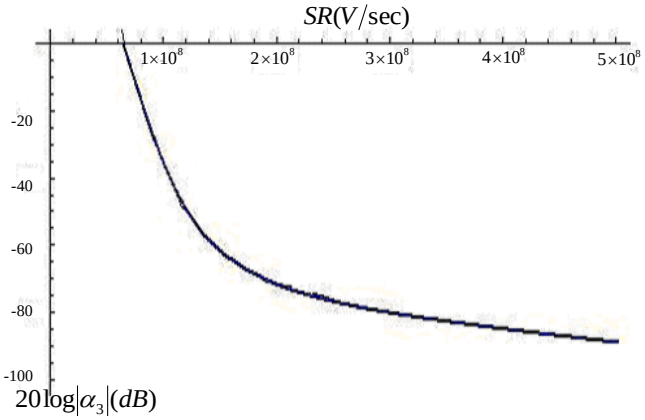


Fig. 14 $20\log|\alpha_3|$ vs. *SR*

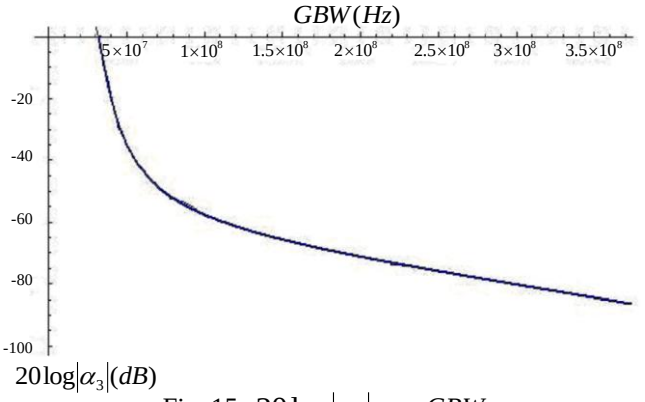


Fig. 15 $20\log|\alpha_3|$ vs. *GBW*

OSR	**HD3(dB)**	***SR*** $(V/\mu s)$	***GBW*** **(MHz)**
8	$20\log\|\alpha_3\|$ -24	≥ 500	≥ 380
16	$20\log\|\alpha_3\|$ -42	≥ 200	≥ 180
32	$20\log\|\alpha_3\|$ -60	≥ 120	≥ 70
50	$20\log\|\alpha_3\|$ -72	≥ 110	≥ 60
64	$20\log\|\alpha_3\|$ -78	≥ 100	≥ 50
96	$20\log\|\alpha_3\|$ -89	≥ 90	≥ 40

Table Ⅷ Minimum *SR* and *GBW* required w.r.t. *OSR*

Fig. 15.

In general, harmonic distortion less than -110dB can be ignored because it is below the noise floor of modulator output spectrum. From (60), Fig. 14 and Fig. 15, we can obtain the minimum required *SR* and *GBW* w.r.t. a specific *OSR*. The results are summarized in Table Ⅷ. It is clear from Table Ⅷ that as *OSR* decreases, *SR* and *GBW* have to increase dramatically so that the effect of settling distortion can be contained. This can be explained by (59), since *T* increases when *OSR* decreases.

APPENDIX B

For Case B in Section Ⅳ, the $P_{\varepsilon 1}$, P_{sw} and P_{OTA} are modified as follows.

1. $P_{\varepsilon 1}$

The total charge transmitted to all unit capacitors C_u in sampling phase is

$$Q = N_p \cdot [V_{in+} - (V_{in+} - V_r) \cdot e^{(-\frac{T}{2 \cdot R \cdot C_u})}] \cdot C_u + N_n \cdot [V_{in+} - (V_{in+} + V_r) \cdot e^{(-\frac{T}{2 \cdot R \cdot C_u})}] \cdot C_u \quad (61)$$

where N_p and N_n represents the number of unit capacitors connected to V_r and $-V_r$ respectively, and $N_p + N_n = 2^B$. The (61) can be simplified to

$$Q = [V_{in+} + V_S \cdot e^{(-\frac{T}{2 \cdot R \cdot C_u})}] \cdot 2^B \cdot C_u \quad (62)$$

where $V_S = \frac{(N_P - N_n)}{2^B} \cdot V_r - V_{in+}$, so the settling error during the sampling phase is $\varepsilon_1 = V_S \cdot e^{(-\frac{T}{2 \cdot R \cdot C_u})}$. The noise power can be easily derived as:

$$P_{\varepsilon 1} = \frac{1}{OSR} \cdot \left(\frac{1.4 \cdot V_{\text{ref}}}{2^B} \right)^2 \cdot e^{(-\frac{T}{2 \cdot R \cdot C_u})} \quad (63)$$

Since C_u is much smaller than C_S, the settling error during the sampling phase in (61) is much smaller than that in (12). If B is high enough, $P_{\varepsilon 1}$ can even be neglected.

2. P_{sw}

The integrator and the feedback DAC are combined by splitting up C_S in [5] into 2^B parallel unity capacitors C_u, so the KT/C noise from input branch in Fig.1 can be excluded, and the total noise power become half that of (2), which is:

$$P_{sw} \cong \frac{1}{OSR} \cdot \left(\frac{4kT}{C_S} \right) \quad (64)$$

Here an assumption for (62) is $C_S = 2^B \cdot C_u$.

3. P_{OTA}

Equation (4) is modified to become

$$\frac{V_O}{V_{no}}(s) \cong \left(\frac{a_1 + 1 + sC_uR}{1 + sC_uR} \right) \Big/ \left(1 + \frac{s}{GBW/A} \right) \quad (65)$$

The noise power still can be obtained from (6), with (4) replaced by (65).

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