The Impact of Gate-Oxide Breakdown on Common-Source Amplifiers With Diode-Connected Active Load in Low-Voltage CMOS Processes

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***Abstract*—The influence of gate-oxide reliability on common–source amplifiers with diode-connected active load is investigated with the nonstacked and stacked structures under analog application in a 130-nm low-voltage CMOS process. The test conditions of this work include the dc stress, ac stress with dc offset, and large-signal transition stress under different frequencies and signals. After overstresses, the small-signal parameters, such as small-signal gain, unity-gain frequency, phase margin, and output dc voltage levels, are measured to verify the impact of gate-oxide reliability on circuit performances of the common-source amplifiers with diode-connected active load. The small-signal parameters of the common-source amplifier with the nonstacked diode-connected active-load structure are strongly degraded than that with the stacked diode-connected active-load structure due to a gate-oxide breakdown under analog and digital applications. The common-source amplifiers with diode-connected active load are not functionally operational under digital application due to the gate-oxide breakdown. The impact of soft and hard gate-oxide breakdowns on the common-source amplifiers with nonstacked and stacked diode-connected active-load structures has been analyzed and discussed. The hard breakdown has more serious impact on the common-source amplifiers with diode-connected active load.**

***Index Terms*—Analog integrated circuit, common-source amplifier, dielectric breakdown, gate-oxide reliability, hard breakdown, soft breakdown.**

I. Introduction

THE REDUCTION of power consumption has become increasingly important to portable products such as mobile phone, notebook, and Flash memory. In general, the most common and efficient way to reduce the power consumption in CMOS very-large-scale-integrated (VLSI) circuits is to reduce the power supply voltage. To reduce the power consumption in the CMOS VLSI systems, the standard supply voltage trends to scale down from 2.5 to 1 V. Thus, the gate-oxide thickness of the MOS transistor becomes thin to reduce nominal operation voltage (power supply voltage). In general, the VLSI productions have a lifetime of ten years, but the thin gate-oxide thickness of the MOS transistor has many problems, such as gate-oxide breakdown, tunneling current, and hot carrier effect, that will degrade the lifetime of the MOS transistor. Therefore, improving the gate-oxide reliability of MOS transistor and investigating the effect of gate-oxide breakdown on CMOS circuit performances become more important in the nanometer CMOS technology.

The occurrence of gate-oxide breakdown during the lifetime of CMOS circuits cannot be completely ruled out. The exact extrapolation of time to breakdown at operating conditions is still difficult since the physical mechanism governing the MOSFET gate dielectric breakdown is not yet fully modeled. It was less of a problem for the old CMOS technologies, which had a thick gate oxide. However, because the probability of gate-oxide breakdown strongly increases with the decreasing oxide thickness [1], [2], the CMOS circuit in nanoscale technologies could be insufficiently reliable. The defect generation leading to gate-oxide breakdown and the nature of the conduction after gate-oxide breakdown have been investigated [1]–[12], which point out that the gate-oxide breakdown will degrade the small-signal parameters of the MOS transistor, such as transconductance g_m and threshold voltage $V_{\rm TH}$. Recently, some studies on the impact of MOSFET gate-oxide breakdown on circuits have been reported [3]–[12]. In [3], it was demonstrated that the digital circuits would remain functional beyond the first hard gate-oxide breakdown. A soft gate-oxide breakdown event in dynamic CMOS digital circuit relying on the uncorrected soft nodes may result in some failure of the circuit [4]. The gate-oxide breakdown on RF circuit has been studied [5]. The impact of gate-oxide breakdown on SRAM stability was also investigated [6], [7]. Some designs of analog circuits [13], [14] and mixed-voltage I/O interface [15], [16] indicate that gate-oxide reliability is a very important design consideration in CMOS integrated circuits. The impact of MOSFET gate-oxide reliability on the CMOS operational amplifiers had been investigated and simulated [17], [18]. The performances of analog circuits strongly depend on the I–V characteristics of MOSFET devices because the small-signal parameters of MOSFET device are determined by the biasing voltage and current of MOSFET devices. The small-signal gain and the frequency response of analog circuits in CMOS processes are determined by the transconductance g_m and the output resistance r_o of MOSFET devices which can be expressed by

$$g_m = \mu C_{\rm ox}\frac{W}{L}(V_{\rm GS}-V_{\rm TH}) = \frac{2I_D}{(V_{\rm GS}-V_{\rm TH})} \tag{1}$$

$$r_o = \frac{V_A}{I_D} \tag{2}$$

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where μ is the mobility of carrier, L denotes the effective channel length, W is the effective channel width, $C_{\rm ox}$ is the gate-oxide capacitance per unit area, $V_{\rm TH}$ is the threshold voltage of MOSFET device, $V_{\rm GS}$ is the gate-to-source voltage of MOSFET device, V_A is the Early voltage, and current I_D is the drain current of MOSFET device. Comparing (1) and (2), the drain current I_D is the key factor for analog circuits in CMOS process. Therefore, the performances of analog circuits in CMOS processes are dominated by the drain currents of MOSFET devices. The drain current I_D of MOSFET device operated in saturation region can be expressed by

$$I_D = \frac{1}{2}\mu C_{\rm OX}\frac{W}{L}(V_{\rm GS} - V_{\rm TH})^2. \tag{3}$$

The channel-length modulation and the body effect of MOSFET devices are not included in (3). The threshold voltage and the gate-to-source voltage of MOSFET device are the important design parameters in (3). However, the gate-oxide overstress of MOSFET will degrade the device characteristics of MOSFET. Therefore, gate-oxide breakdown can be expected to have a serious impact on the performances of analog circuits in nanoscale CMOS technology.

In this paper, the influence of gate-oxide reliability on common-source amplifiers with diode-connected active load is investigated with the nonstacked and stacked structures in a 130-nm low-voltage CMOS process under the dc stress, ac stress with dc offset, and large-signal transition stress. The small-signal gain, phase margin, unity-gain frequency, and output dc voltage level of the two common-source amplifiers are measured and compared under the different stresses in analog and digital applications. The impact of soft and hard breakdowns on these two amplifiers has been discussed and analyzed.

II. Analog Amplifiers

The common-source amplifier is a basic unit in many typical analog circuitry cells such as level converter and output stage. The common-source amplifiers with the nonstacked and stacked diode-connected active-load structures are used to verify the impact of MOSFET gate-oxide reliability on CMOS analog amplifier. The complete circuits of the common-source amplifiers with the nonstacked and stacked diode-connected active-load structures are shown in Fig. 1(a) and (b). The common-source amplifiers have been fabricated in a 130-nm low-voltage CMOS process. The normal operating voltage and the gate-oxide thickness ($t_{\rm ox}$) of all MOSFET devices in these two common-source amplifiers are 1 V and 2.5 nm, respectively, in a 130-nm low-voltage CMOS process. The device dimensions of two amplifiers are shown in Table I. The body terminals of all the NMOS and PMOS transistors are connected to ground and power supply voltage, respectively. The small-signal gain $A_{V\_\rm Nonstacked}$ of the common-source amplifier

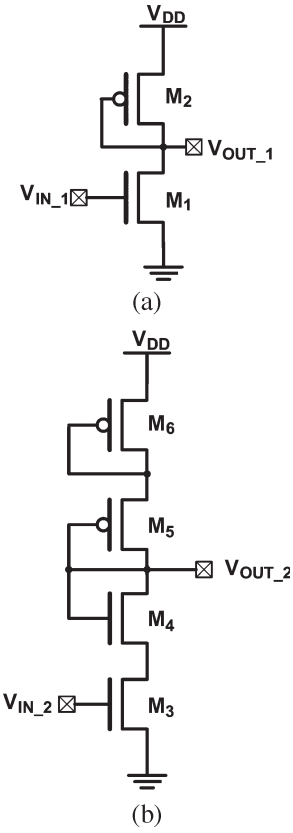


Fig. 1. Complete circuits of the common-source amplifiers with the (a) nonstacked and (b) stacked diode-connected active-load structures.

TABLE I
Device Dimensions of the Common-Source Amplifiers With the Nonstacked and Stacked Diode-Connected Active-Load Structures

Device	Dimension	Device	Dimension
M_1	8μ/1μ	M_4	2μ/1μ
M_2	1μ/1.5μ	M_5	1μ/1μ
M_3	1.8μ/1μ	M_6	1μ/1μ

with the nonstacked diode-connected active-load structure is given by

$$A_{V\_\rm Nonstacked} = -\frac{g_{m1} - SC_{\rm GD1}}{g_{o1}+g_{o2}+g_{m2}+S(C_{\rm GD1}+C_{\rm GS2}+C_L)} \tag{4}$$

where g_o and g_m are the output conductance and transconductance of MOS transistor, respectively. In the MOSFET device, $C_{\rm GS}$ is the parasitic capacitance between the gate and source nodes, and $C_{\rm GD}$ is the parasitic capacitance between the gate and drain nodes. C_L is the output capacitive load. The small-signal gain $A_{V\_\rm Stacked}$ of the common-source amplifier with the stacked diode-connected active-load structure can be written as

$$A_{V\_\rm Stacked} = -\frac{g_{o3}(g_{m3}-SC_{\rm GD3})}{(SC_{\rm GD3}+g_{o3}+g_{\rm oz})\left[(SC_L+g_{\rm ox}//g_{\rm oy})-g_{\rm oz}g_{o3}\right]} \tag{5}$$

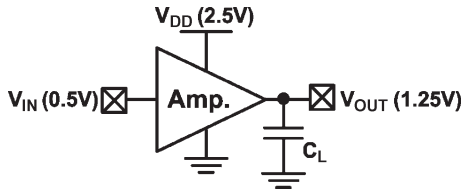


Fig. 2. Measured setup for the common-source amplifiers with the nonstacked and stacked diode-connected active-load structures under dc stress to investigate the impact of gate-oxide reliability on circuit performances.

where $g_{\rm ox}$, $g_{\rm oy}$, and $g_{\rm oz}$ are equal to $g_{m5}+g_{o5}+\mathrm{SC}_{\rm GS5}$, $g_{m6}+g_{o6}+\mathrm{SC}_{\rm GS6}$, and $g_{m4}+g_{o4}+\mathrm{SC}_{\rm GS4}$, respectively. Before overstress, the small-signal gains of the common-source amplifiers with the nonstacked and stacked diode-connect active-load structures are 17.5 and 13.2 dB, respectively. The body effect of the NMOS and PMOS transistors in the common-source amplifiers with the nonstacked and stacked diode-connect active-load structures is not included in (4) and (5). The phase margin of the two common-source amplifiers is more than 60° under an output capacitive load of 10 pF. Comparing the common-source amplifiers with the nonstacked and stacked diode-connected active-load structures, the impact of gate-oxide reliability on the CMOS common-source amplifier has been investigated under analog and digital applications.

III. Overstress Test

The impact of gate-oxide reliability on common-source amplifier needs a long-term operation, which may need many years, to measure the performance degradation under the gate-oxide degradation of MOSFET device. In order to accelerate the gate-oxide degradation and to understand the impact of gate-oxide reliability on common-source amplifiers with the nonstacked and stacked diode-connected active-load structures, the common-source amplifiers with the nonstacked and stacked diode-connected active-load structures are statically stressed at supply voltage $V_{\rm DD}$ of 2.5 V. Because the MOS transistors in analog circuits usually work in the saturation region, the gate-oxide breakdown is more likely to occur in conventional time-dependent dielectric breakdown (TDDB). High $V_{\rm GS}$, $V_{\rm GD}$, and $V_{\rm DS}$ of the MOSFET are set to get a fast and easy-to-observe breakdown occurrence in investigating the impact of gate-oxide reliability on the common-source amplifier with diode-connected active load. The advantages of using static stress are the known and well-defined distributions of the voltages in the common-source amplifiers with diode-connected active load and better understanding of the consequences of this stress. After the overstresses, the small-signal parameters of the common-source amplifiers with nonstacked and stacked diode-connected active-load structures are reevaluated on the same operation condition under the dc stress, the ac stress with dc offset, and the large-signal transition stress.

A. DC Stress

The common-source amplifiers with the nonstacked and stacked diode-connected active-load structures are continuously operated in this dc overstress, as shown in Fig. 2. The power supply voltage $V_{\rm DD}$ and the output capacitive load C_L of the common-source amplifiers with nonstacked and stacked diode-connected active-load structures are set to 2.5 V and 10 pF, respectively. The input nodes $V_{\rm IN\_1}$ and $V_{\rm IN\_2}$ are biased to 0.5 V in order to set the output dc voltage level at 1.25 V under the power supply voltage of 2.5 V. During this dc overstress, the small-signal gain and the unity-gain frequency of the common-source amplifiers with the nonstacked and stacked diode-connected active-load structures are measured. When those parameters are measured, the input signal of dc (0.5 V) at input nodes $V_{\rm IN\_1}$ and $V_{\rm IN\_2}$ is replaced by the ac small signal of 200-mV sinusoidal signal (peak-to-peak amplitude) with a dc voltage of 0.5 V. The dependence of the small-signal gain on the stress time of the common-source amplifiers with the nonstacked and stacked diode-connected active-load structures under the dc stress is shown in Fig. 3. The small-signal gain of the common-source amplifier with the nonstacked diode-connected active-load structure is degraded by the gate-oxide breakdown. Moreover, the common-source amplifier with the nonstacked diode-connected active-load structure does not maintain its amplified function with continuous stress condition under the dc stress when the stress time is increased. The small-signal gain of the common-source amplifier with the stacked diode-connected active-load structure is not changed under the same stress condition even through the stress time of up to 2000 min. The measured waveforms of the input and output signals in the common-source amplifier with the nonstacked diode-connected active-load structure on the different stress times are shown in Fig. 4(a)–(c). Fig. 5 shows the dependence of the unity-gain frequency on the stress time of the common-source amplifiers with the nonstacked and stacked diode-connected active-load structures under the dc stress. The bandwidth of the common-source amplifier with nonstacked diode-connected active-load structure on the stress time is decreased, but that of the common-source amplifier with the stacked diode-connected active-load structure is almost not changed after the stress. The phase margin of the common-source amplifier with the nonstacked diode-connected active-load structure on the stress time is varied with gate-oxide breakdown, but that is still stable (phase margin $> 45°$). The dependence of the output

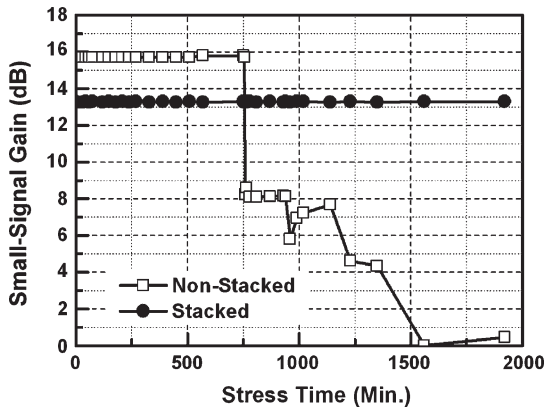
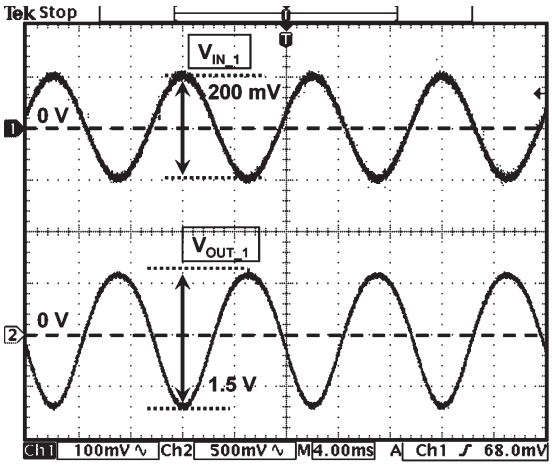
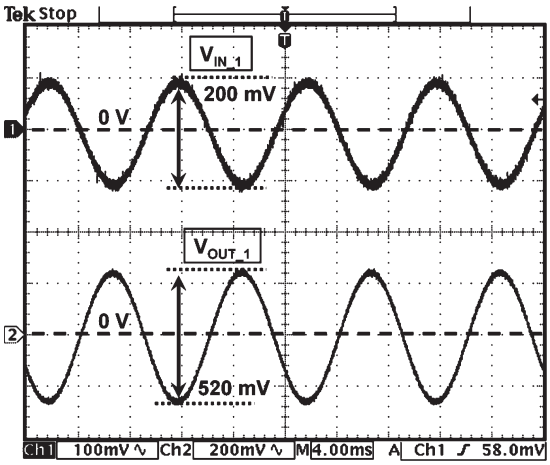


Fig. 3. Dependence of the small-signal gain on the stress time of the common-source amplifiers with the nonstacked and stacked diode-connected active-load structures under the dc stress.



(a)



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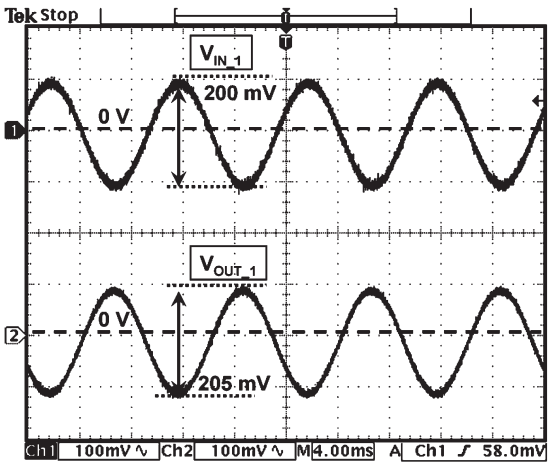


(c)

Fig. 4. Input and output signal waveforms on the different stress times of the common-source amplifier with the nonstacked diode-connected active-load structure under the dc stress. (a) Stress time = 0 min. (b) Stress time = 980 min. (c) Stress time = 2000 min.

dc voltage level on the stress time of the common-source amplifiers with the nonstacked and stacked diode-connected active-load structures under the dc stress is shown in Fig. 6. The output dc voltage level of the common-source amplifier with the nonstacked diode-connected active-load structure on

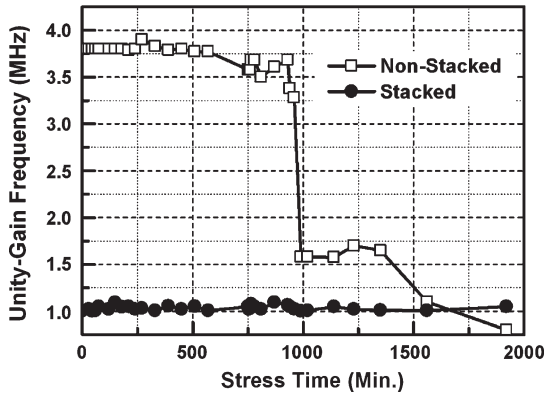


Fig. 5. Dependence of the unity-gain frequency on the stress time of the common-source amplifiers with the nonstacked and stacked diode-connected active-load structures under the dc stress.

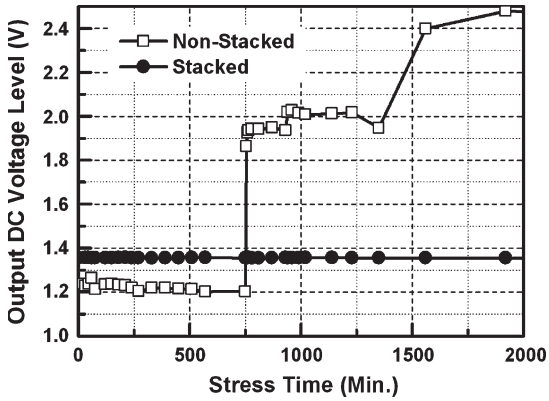


Fig. 6. Dependence of the output dc voltage level on the stress time of the common-source amplifiers with the nonstacked and stacked diode-connected active-load structures under the dc stress.

the stress time will be closed to the power supply voltage of 2.5 V, but that of the common-source amplifier with the stacked diode-connected active-load structure is not changed after the stress.

The reason why the circuit performances of the common-source amplifier with the nonstacked diode-connected active-load structure, such as small-signal gain, unity-gain frequency, and output dc voltage level, are degraded by the overstress is summed up that the gate-oxide breakdown will degrade the transconductance (g_m), the threshold voltage $(V_{\rm TH})$, and the output conductance (g_o) of the MOS transistor. In (4), if the small-signal parameters g_m, $V_{\rm TH}$, and g_o of the MOS transistor are degraded by the gate-oxide breakdown, the small-signal gain will be changed. From (4), the dominant pole of the common-source amplifier with the nonstacked diode-connected active-load structure can be written as

$$\omega_{p\_\rm Nonstacked} = \frac{g_{m2} + g_{o1} + g_{o2}}{C_{\rm GS2} + C_{\rm GD1} + C_L} \tag{6}$$

which is dominated by transconductance g_{m2} and output capacitive load C_L. Therefore, the unity-gain frequency of the common-source amplifier with the nonstacked diode-connected active-load structure will be degraded by the gate-oxide breakdown. In this test condition, if the transistors M_1 and M_2 of the common-source amplifier with the nonstacked

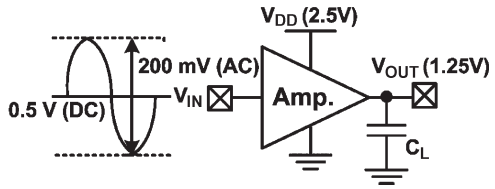


Fig. 7. Measured setup for the common-source amplifiers with the nonstacked and stacked diode-connected active-load structures under ac stress with dc offset to investigate the impact of gate-oxide reliability on circuit performances.

diode-connected active-load structure are designed to operate in saturation region, the output dc voltage level of the common-source amplifier with the nonstacked diode-connected active-load structure can be expressed as

$$V_{\mathrm{OUT\_1(DC)}} = V_{\mathrm{DD}} - V_{\mathrm{TH}(M_2)} - \sqrt{\frac{\left(\frac{W}{L}\right)_{M_1}}{\left(\frac{W}{L}\right)_{M_2}}}\left(V_{\mathrm{IN\_1}} - V_{\mathrm{TH}(M_1)}\right). \quad (7)$$

In (7), the output dc voltage level $V_{\mathrm{OUT\_1(DC)}}$ is a function of $V_{\mathrm{TH}(M_1)}$ and $V_{\mathrm{TH}(M_2)}$. Therefore, the output dc voltage level of the common-source amplifier with the nonstacked diode-connected active-load structure will be changed with gate-oxide breakdown after the stress.

B. AC Stress With DC Offset

The common-source amplifiers with the nonstacked and stacked diode-connected active-load structures are continuously tested in this stress of ac small-signal input and dc offset, as shown in Fig. 7. The input nodes $V_{\mathrm{IN\_1}}$ and $V_{\mathrm{IN\_2}}$ of the common-source amplifiers with the nonstacked and stacked diode-connected active-load structures are biased to the ac small-signal input of 200-mV sinusoidal signal (peak-to-peak amplitude) with a dc offset voltage of 0.5 V under the different frequencies of 100 Hz, 500 kHz, and 1 MHz. The power supply voltage V_{DD} and the output capacitive load C_L of the common-source amplifiers with nonstacked and stacked structures are set to 2.5 V and 10 pF, respectively. The measurement setup is used to investigate the relationship between the gate-oxide breakdown and the different frequencies of input signals in the CMOS analog-circuit applications.

The dependence of the small-signal gain in the common-source amplifiers with the nonstacked and stacked diode-connected active-load structures on the stress time under the stress of the ac small-signal input with dc offset is shown in Fig. 8. The circuit performances of the common-source amplifier with the stacked diode-connected active-load structure are not degraded by the stress of the ac small-signal input with dc offset. In the common-source amplifier with the nonstacked diode-connected active-load structure, the high-frequency input signal causes a slow degradation on the small-signal gain, but the low-frequency input signal causes a fast degradation on the small-signal gain under the stress of the ac small-signal input with dc offset. The other small-signal performances in the common-source amplifier with the nonstacked diode-connected active-load structure under the stress of the ac small-signal

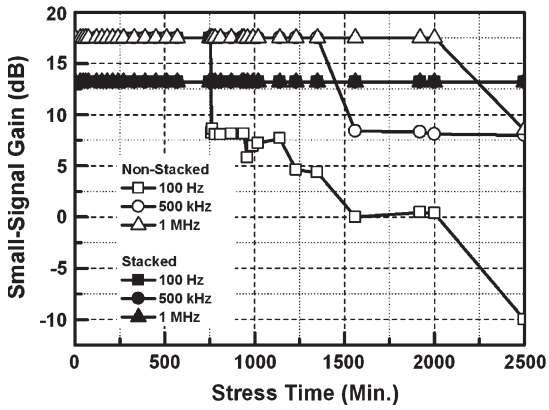


Fig. 8. Dependence of the small-signal gain on the stress time of the common-source amplifiers with the nonstacked and stacked diode-connected active-load structures under the stress of the ac small-signal input with dc offset.

input with dc offset have the same change trend as that under the dc stress, but the different frequencies of the input signal will cause the different degradation times. These measured results are consistent to that reported in [19]. The frequency dependence of t_{BD} (time to breakdown) is reasonably understood in terms of the redistribution of the breakdown species from the anodic interface toward the oxide bulk. These two different frequency regimes correspond to two extreme distributions. When the frequency is very high, the concentration of "breakdown species" is expected to be low. The distribution strongly peaked at both interfaces. This presumably explains the reduction of degradation. On the contrary, in the low frequency, concentration is expected to be high and to have a uniform distribution throughout the oxide film. This leads to faster degradation process [19]. Therefore, the small-signal performance of the nonstacked common-source amplifier with different frequencies of the input signals will cause different degradation times under the stress of the ac small-signal input with dc offset.

C. Large-Signal Transition Stress

Many research results indicated that the high and low output voltage levels of the CMOS digital complementary logic circuits under large-signal transition stress were not degraded by the gate-oxide breakdown [2], [18]. Only the maximum operation frequency of the CMOS digital complementary logic circuits was decreased with gate-oxide breakdown, but the impact of gate-oxide breakdown on the inverter with active load (common-source amplifier) is still not studied. Therefore, the common-source amplifiers with the nonstacked and stacked diode-connected active-load structures are used to investigate the impact of gate-oxide reliability on CMOS inverter with active load under the large-signal transition stress. The common-source amplifiers with the nonstacked and stacked diode-connected active-load structures are continuously tested in this stress of large-signal transition, as shown in Fig. 9. The input nodes $V_{\mathrm{IN\_1}}$ and $V_{\mathrm{IN\_2}}$ of the amplifiers with the nonstacked and stacked diode-connected active-load structures are biased at a dc of 0.5 V, the output capacitive load C_L is set

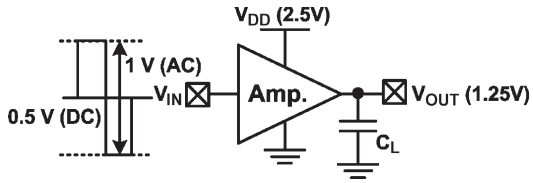


Fig. 9. Measured setup for the common-source amplifiers with the nonstacked and stacked diode-connected active-load structures under large-signal transition stress to investigate the impact of gate-oxide reliability on circuit performances.

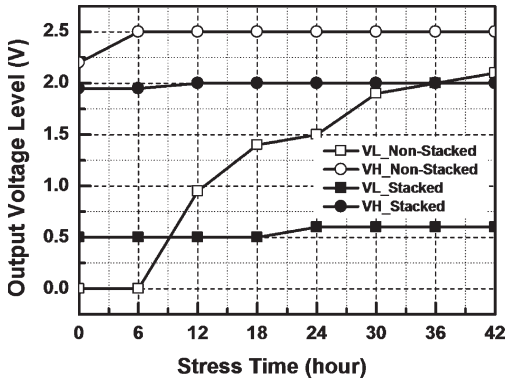
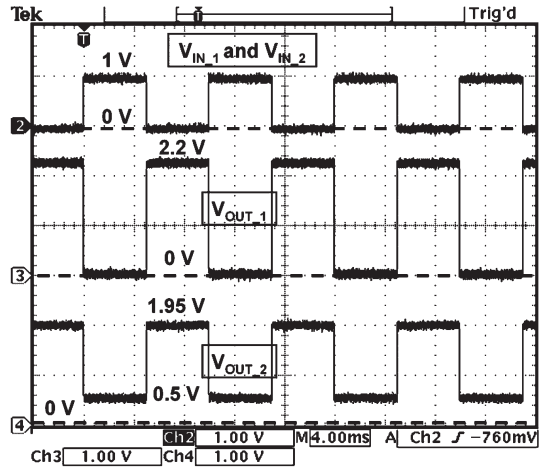


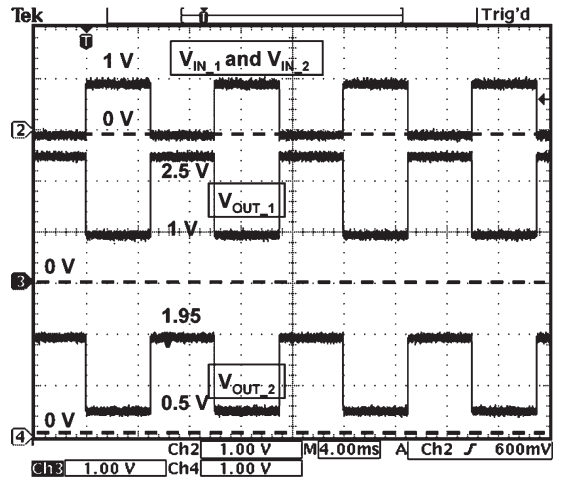
Fig. 10. Dependences of the high and low output voltage levels (VH and VL) at the output nodes of the common-source amplifiers with the nonstacked and stacked diode-connected active-load structures on the stress time under stress of large-signal transition.

to 10 pF, and the power supply voltage $V_{\rm DD}$ is set to 2.5 V. The input square voltage from 0 to 1 V with a frequency of 100 Hz is applied to the input node of the common-source amplifiers with the nonstacked and stacked diode-connected active-load structures under the large-signal transition stress. The square voltage of input signal from 0 to 1 V will not induce the damage on the input devices M_1 and M_3 of the common-source amplifiers with the nonstacked and stacked diode-connected active-load structures because the voltage across the input devices $(V_{\rm GS})$ of the common-source amplifiers is lower than 1 V in this measurement.

The dependences of the high and low voltage levels at the output node on the stress time are shown in Fig. 10, where the common-source amplifiers with the nonstacked and stacked diode-connected active-load structures are stressed by the large-signal transition. The high and low output voltage levels of the common-source amplifiers with the nonstacked and stacked diode-connected active-load structures under the stress of large-signal transition are increased when the stress time is increased. The measured waveforms of the input and output signals of the common-source amplifiers with the nonstacked and stacked diode-connected active-load structures on the different stress times under the large-signal transition stress are shown in Fig. 11(a)–(c). The impact of gate-oxide breakdown on the common-source amplifier with the nonstacked diode-connected active-load structure is more serious than that of the common-source amplifier with the stacked diode-connected active-load structure under the large-signal transition stress. The maximum operation frequency of the common-source amplifiers with the nonstacked and stacked



(a)



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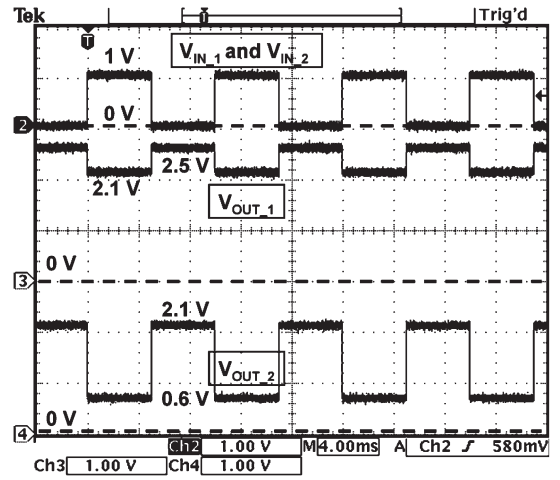

(c)

Fig. 11. Input and output signal waveforms on the different stress times of the common-source amplifier with the nonstacked and stacked diode-connected active-load structures under the large-signal transition stress. (a) Stress time = 0 h. (b) Stress time = 12 h. (c) Stress time = 42 h.

structures has the same change trend as that of the CMOS digital complementary logic circuits under the large-signal transition stress. The measured results of the large-signal transition stress have some difference with the results of the prior

TABLE II
COMPARISONS OF THE COMMON-SOURCE AMPLIFIERS WITH THE NONSTACKED AND STACKED DIODE-CONNECTED ACTIVE-LOAD STRUCTURES AMONG THE THREE OVERSTRESS CONDITIONS

Stress Conditions	Performances	Non-Stacked	Stacked
DC Stress	Small-Signal Gain	Seriously Degraded	No Change
	Unity-Gain Frequency	Seriously Degraded	No Change
	Output DC Voltage Level	Seriously Degraded	No Change
AC Stress with DC Offset	Small-Signal Gain	• High Frequency → Slow Degraded Rate • Low Frequency → High Degraded Rate	No Change
Large-Signal Transition Stress	High and Low Output Voltage Levels	Seriously Degraded	Degraded

research works [2], [18], because the high and low output voltage levels of the common-source amplifiers with the nonstacked and stacked diode-connected active-load structures are controlled by diode-connected transistors M_2, M_4, M_5, and M_6, respectively. For example, the high output level of the common-source amplifier with the nonstacked diode-connected active-load structure can be expressed as

$$VH_{\_\mathrm{Nonstacked}} = V_{\mathrm{DD}} - \left|V_{\mathrm{TH}(M_2)}\right|. \tag{8}$$

The low output level of the common-source amplifier with the nonstacked diode-connected active-load structure can be written as

$$VL_{\_\mathrm{nonstacked}} = 2(V_{\mathrm{IN\_1}} - V_{\mathrm{TH}(M_1)}) - \sqrt{\left[4\left(V_{\mathrm{IN\_1}} - V_{\mathrm{TH}(M_1)}\right)^2 - 4\frac{\left(\frac{W}{L}\right)_{M_2}}{\left(\frac{W}{L}\right)_{M_1}}\left(V_{\mathrm{DD}} - \left|V_{\mathrm{TH}(M_2)}\right|\right)\right]}. \tag{9}$$

The threshold voltage (V_{TH}) of the MOS transistor will be degraded by the gate-oxide breakdown, so that the $V_{H\_\mathrm{nonstacked}}$ and V_{L_stacked} of the common-source amplifier with the nonstacked diode-connected active-load structure will be changed under the stress of large-signal transition. In the CMOS digital complementary logic circuits, either pull-up or pull-down MOS transistors will be turned ON under the logic high or low steady state, respectively. The logic high and low steady states of the CMOS digital complementary logic circuits are independent of the dimension and threshold voltage of the MOS transistors. Therefore, the voltage levels of the logic high and low steady states in the CMOS digital complementary logic circuits will not be degraded by the gate-oxide breakdown.

IV. DISCUSSIONS

The summary of overstress results under three overstress conditions (dc, ac, and large-signal transition stresses) is listed in Table II. The gate-oxide breakdown will degrade the transconductance (g_m), the output conductance (g_o), and the threshold voltage (V_{TH}) of MOSFET devices. After the overstress, the performances of the common-source amplifier with the nonstacked diode-connected active-load structure under the dc, the ac with dc offset, and the large-signal transition stresses are seriously degraded by the gate-oxide breakdown, and those of the common-source amplifier with stacked diode-connected active-load structure are only slightly degraded under the large-signal transition stress. As a result, the performance degradation of the common-source amplifier with the nonstacked diode-connected active-load structure is more serious than that of the common-source amplifier with the stacked diode-connected active-load structure. The small-signal performance of the common-source amplifier is very sensitive to the dc operation point; thus, the gate-oxide breakdown will cause the g_m, V_{TH}, and g_o degradations and extra gate-leakage current of the MOS transistor to induce the change of the dc operation point in the common-source amplifier. Considering the common-source amplifier with the nonstacked diode-connected active-load structure, if the parameters g_{m1} and g_{m2} are variable factors in (1), the sensitivities of (1) to the parameters g_{m1} and g_{m2} are expressed as

$$S_{g_{m1}}^{A_{V\_\mathrm{Nonstacked}}} = \frac{g_{m1}}{g_{m1} - SC_{\mathrm{GD1}}} \tag{10}$$

$$S_{g_{m2}}^{A_{V\_\mathrm{Nonstacked}}} = \frac{g_{m2}}{g_{o1} + g_{o2} + g_{m2} + S(C_{\mathrm{GD1}} + C_{\mathrm{GS2}} + C_L)}. \tag{11}$$

In (10) and (11), the parameters g_{o1} and g_{o2} can be ignored because they are smaller than one. The parasitic capacitances C_{GD1} and C_{GS2} of the MOS transistors are not considered. The sensitivities of (10) and (11) to the parameters g_{m1} and g_{m2}, respectively, are approximately one. Therefore, the gate-oxide breakdown of the MOS transistors has a serious impact on the circuit performances of analog circuits. As a result, the gate-oxide reliability is a very important design issue in the nanometer CMOS process. The gate-oxide reliability can be improved by the stacked structure in the common-source amplifier under small-signal input and output applications. The common-source amplifier with the stacked diode-connected active-load structure can work in high supply voltage depending on the stacked number of transistor that is used to control the voltages (V_{GS}, V_{GD}, and V_{DS}) across the transistor and to avoid the gate-oxide breakdown.

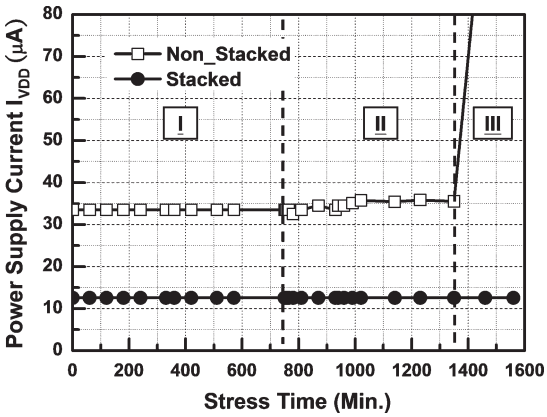

Fig. 12. Measured dependence of the power supply current $I_{\rm VDD}$ of the common-source amplifiers with the nonstacked and stacked diode-connected active-load structures on stress time under dc stress.

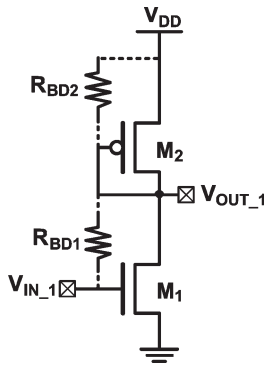

Fig. 13. Complete circuit of the common-source amplifier with the nonstacked diode-connected active-load structure, including the gate-oxide breakdown model.

V. Effect of Hard and Soft Breakdowns on the Performances of Common-Source Amplifiers

A. DC Stress

The measured dependence of power supply current $I_{\rm VDD}$ in two amplifiers on stress time has been measured and recorded, as shown in Fig. 12, under the dc stress. Because the power supply current $I_{\rm VDD}$ of the common-source amplifier with the stacked diode-connected active-load structure is not degraded after the dc stress, the gate-oxide degradation of MOSFET has not occurred in this measurement. However, the power supply current $I_{\rm VDD}$ of the common-source amplifier with the nonstacked diode-connected active-load structure is degraded during the dc stress. Based on the prior proposed method [11], [20], the gate-oxide breakdown of MOSFET device can be modeled as resistance. Only the gate-to-diffusion (source or drain) breakdown was considered, since this represents the worst case situation. Breakdown to the channel can be modeled as a superposition of two gate-to-diffusion events. Typical hard-breakdown leakage has close-to-linear I–V behavior and an equivalent resistance of $\sim 10^3 - 10^4\ \Omega$, while typical soft-breakdown paths have high-nonlinear power-law I–V behavior and an equivalent resistance above $10^5 - 10^6\ \Omega$ [11]. The oxide breakdown has not occurred in the gate-to-source side of M_1 device in the common-source amplifier with the nonstacked diode-connected active-load structure because the voltage across the gate-to-source side of M_1 device is smaller than 1 V in the amplifier. The complete circuit of the common-source amplifier with the nonstacked diode-connected active-load structure, including the gate-oxide breakdown model, is shown in Fig. 13. The breakdown resistances of $R_{\rm BD1}$ and $R_{\rm BD2}$ can be used to simulate the impact of hard and soft breakdowns on the performances of the common-source amplifier with the nonstacked diode-connected active-load structure. Comparing the measured results among Figs. 3, 5, 6, and 12, the dependence of power supply current $I_{\rm VDD}$ (nonstacked) on stress time in Fig. 12 can be separated by three regions (I, II, and III regions) due to the gate-oxide breakdown. This result has some differences on the impact of gate-oxide breakdown on the performances of analog and digital circuits. When the performances of the common-source amplifier with the nonstacked diode-connected active-load structure are degraded due to the gate-oxide breakdown, the power supply current $I_{\rm VDD}$ is not immediately increased. The relationship between the power supply current $I_{\rm VDD}$ and the gate-oxide breakdown that occurred on M_1 and M_2 devices under the three regions in the common-source amplifier with the nonstacked diode-connected active-load structure can be modeled by the following.

Region I) No gate-oxide breakdown occurred on M_1 and M_2 devices.
Region II) Hard breakdown occurred on M_2 device.
Region III) Hard breakdown occurred on M_1 and M_2 devices.

In Region I, the gate-oxide breakdown of MOSFET device is more likely to occur as the TDDB. In this region, the small-signal performance and the power supply current $I_{\rm VDD}$ of the common-source amplifier with the nonstacked diode-connected active-load structure have very small variations on the stress time under dc stress. The gate-oxide breakdown has not occurred on M_1 and M_2 devices.

In Region II, the power supply current $I_{\rm VDD}$ was not changed, but the small-signal performances of the common-source amplifier with the nonstacked diode-connected active-load structure were seriously degraded. The reason why the power supply current $I_{\rm VDD}$ of the common-source amplifier was not changed is due to the gate-oxide breakdown on M_2 device. The simulated dependence of power supply current $I_{\rm VDD}$ under different breakdown resistances $R_{\rm BD1}$ and $R_{\rm BD2}$ is shown in Fig. 14. The power supply current $I_{\rm VDD}$ of the common-source amplifier with the nonstacked diode-connected active-load structure is dominated by the M_1 device. Because the gate-oxide breakdown on M_1 device has not occurred, the power supply current $I_{\rm VDD}$ of the common-source amplifier is limited under the dc stress. The simulated dependence of small-signal gain and output dc voltage level of the common-source amplifier with the nonstacked diode-connected active-load structure under different resistances $R_{\rm BD2}$ is shown in Fig. 15. Based on the prior proposed method [11], the impact of soft breakdown that occurred on M_2 device has less influence on circuit performances. The hard breakdown that occurred on

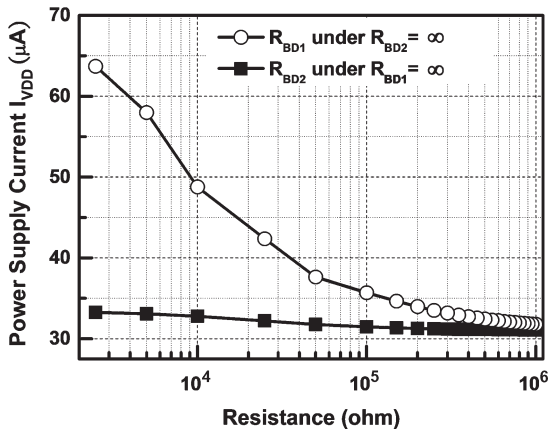

Fig. 14. Simulated dependence of the power supply current $I_{\rm VDD}$ of the common-source amplifier with the nonstacked diode-connected active-load structure under different resistances of $R_{\rm BD1}$ and $R_{\rm BD2}$.

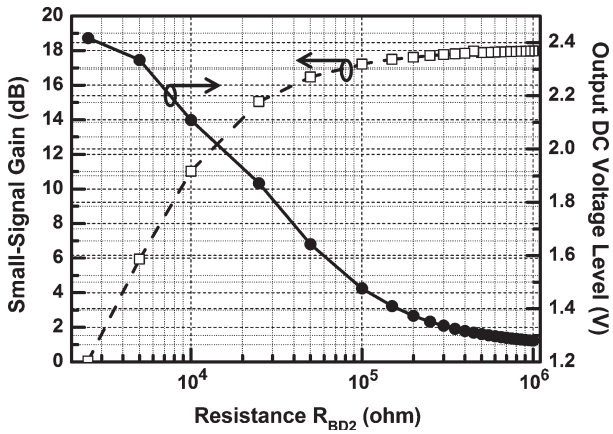

Fig. 15. Simulated dependence of small-signal gain and output dc voltage level of the common-source amplifier with the nonstacked diode-connected active-load structure under different resistances $R_{\rm BD2}$.

M_2 device causes the serious degradations on the performances of the common-source amplifier with the nonstacked diode-connected active-load structure, but the power supply current $I_{\rm VDD}$ was not changed under the dc stress. These simulated results can be used to confirm and understand that the hard breakdown only occurred on the M_2 device of the common-source amplifier with the nonstacked diode-connected active-load structure during the dc stress in Region II.

In Region III, the power supply current $I_{\rm VDD}$ and the small-signal performances of the common-source amplifier with the nonstacked diode-connected active-load structure are seriously degraded under dc stress. The hard breakdown occurred on both the M_1 and M_2 devices under the dc stress in Region III.

Comparing Regions I, II, and III under dc stress, the degradation on power supply current $I_{\rm VDD}$ is dominated by gate-oxide breakdown on M_1 device. The gate-oxide breakdown that occurred on M_2 device is a dominated factor to degrade the performances of the common-source amplifier with the nonstacked diode-connected active-load structure. As a result, the hard breakdown has more serious impact on the performances of common-source amplifier.

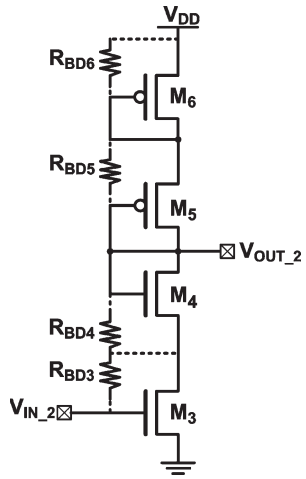

Fig. 16. Complete circuit of the common-source amplifier with the stacked diode-connected active-load structure, including the gate-oxide breakdown model after large-signal transition stress.

B. Large-Signal Transition Stress

In order to investigate and understand the impact of hard and soft breakdowns on the performances of the common-source amplifiers with the nonstacked and stacked diode-connected active-load structures under large-signal transition stress, the complete circuits, including the gate-oxide breakdown model, are shown in Figs. 13 (nonstacked) and 16 (stacked), respectively. In these two amplifiers, the gate-oxide breakdown does not occur on the gate-to-source sides of M_1 (in Fig. 13) and M_3 (in Fig. 16) devices under large-signal transition stress because the voltages across the gate-to-source sides of M_1 and M_3 devices are smaller than 1 V, respectively. The static and the dynamic currents in two amplifiers under digital operation are increased after the gate-oxide breakdown [3]. The hard gate-oxide breakdown has occurred on the common-source amplifier with nonstacked diode-connected active-load structure after overstress. The soft gate-oxide breakdown has occurred on the common-source amplifier with stacked diode-connected active-load structure after overstress. The simulated dependence of high and low output voltage levels (VH and VL) of the common-source amplifiers with the nonstacked diode-connected active-load structures under the different resistances $R_{\rm BD1}$ and $R_{\rm BD2}$ is shown in Fig. 17. The high output voltage level (VH) and the low output voltage level (VL) of the common-source amplifier with nonstacked diode-connected active-load structure are degraded by oxide breakdown that occurred on M_1 and M_2 devices, respectively. Comparing Figs. 10 and 17, the breakdown location in the common-source amplifier with the nonstacked diode-connected active-load structure has occurred on the M_2 device after large-signal transition stress.

The impact of gate-oxide breakdown on the performance of the common-source amplifier with the stacked diode-connected active-load structure can be simulated and investigated by the same method to find the breakdown location. Fig. 18 shows the simulated dependence of the high and low output voltage levels (VH and VL) of the common-source amplifier with the stacked diode-connected active-load structure under the

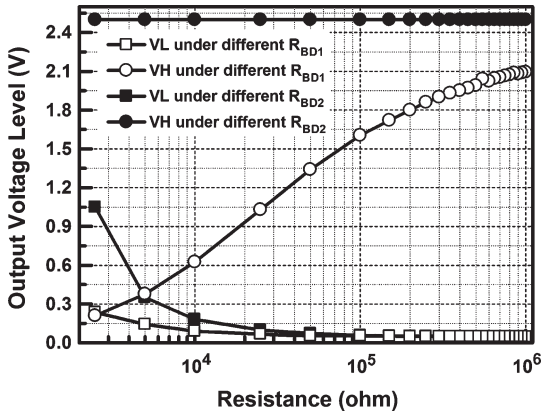

Fig. 17. Simulated dependence of high and low output voltage levels (VH and VL) of the common-source amplifier with the nonstacked diode-connected active-load structure under different resistances of $R_{\rm BD1}$ and $R_{\rm BD2}$ after large-signal transition stress.

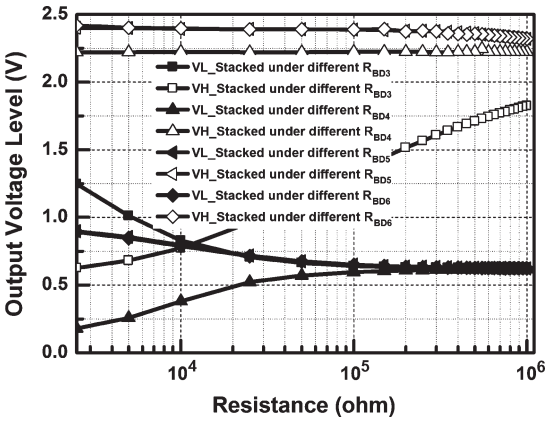

Fig. 18. Simulated dependence of high and low output voltage levels (VH and VL) of the common-source amplifier with the stacked diode-connected active-load structure under different resistances of $R_{\rm BD3}$, $R_{\rm BD4}$, $R_{\rm BD5}$, and $R_{\rm BD6}$ after large-signal transition stress.

different resistances of $R_{\rm BD3}$, $R_{\rm BD4}$, $R_{\rm BD5}$, and $R_{\rm BD6}$, respectively. The different breakdown locations cause different performance degradations of the common-source amplifier with the stacked diode-connected active-load structure under large-signal transition stress. Comparing Figs. 10 and 18, the breakdown location in the common-source amplifier with the stacked diode-connected active-load structure has occurred on M_5 or M_6 device under large-signal transition stress. The high and low output voltage levels (VH and VL) of the common-source amplifier with the stacked diode-connected active-load structure are increased when the stress time is increased. The common-source amplifier with the stacked diode-connected active-load structure has slow degradation rate because the voltage across MOSFET device is smaller than that of the common-source amplifier with the nonstacked diode-connected active-load structure. The hard breakdown has more serious impact on the performances of the common-source amplifier with nonstacked diode-connected active-load structure. The stacked structure can be used to improve the reliability of analog circuits in nanoscale CMOS technology.

VI. Conclusion

The impact of gate-oxide reliability on the CMOS common-source amplifiers with the nonstacked and stacked diode-connected active-load structures has been investigated and analyzed under the dc stress, the ac stress with dc offset, and the large-signal transition stress. The small-signal parameters of the common-source amplifier with the nonstacked diode-connected active-load structure are seriously degraded than that with the stacked diode-connected active-load structure by gate-oxide breakdown under dc, ac, and large-signal transition stresses. The stacked structure can be used to improve the reliability of analog circuit in nanoscale CMOS process. The impact of soft breakdown, hard breakdown, and breakdown location on the circuit performances of the common-source amplifiers with the nonstacked and stacked diode-connected active-load structures has been investigated and analyzed. The hard gate-oxide breakdown has more serious impact on the performances of the common-source amplifier with the diode-connected active load.

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