Work Function Tunability of Refractory Metal Nitrides by Lanthanum or Aluminum Doping for Advanced CMOS Devices

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***Abstract*—A lanthanum (La)-doped HfN is investigated as an n-type metal gate electrode on SiO_2 with tunable work function. The variation of La concentration in $(Hf_xLa_{1-x})N_y$ modulates the gate work function from 4.6 to 3.9 eV and remains stable after high-temperature annealing (900 °C to 1000 °C), which makes it suitable for n-channel MOSFET application. An ultrathin high-k dielectric layer was formed at the metal/SiO_2 interface due to the $(Hf_xLa_{1-x})N_y$ and SiO_2 interaction during annealing. This causes a slight reduction in the effective oxide thickness and improves the tunneling current of the gate dielectric by two to three orders. We also report the tunability of TaN with Al doping, which is suitable for a p-type metal gate work function. Based on our results, several dual-gate integration processes by incorporating lanthanum or aluminum into a refractory metal nitride for CMOS technology are proposed.**

***Index Terms*—High-k gate dielectric, metal gate, MOSFET, work function tuning, $(Hf_xLa_{1-x})N_y$, $(Ta_xAl_{1-x})N_y$.**

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I. Introduction

As THE devices are aggressively scaled down for sub-45-nm CMOSFET technology nodes, the poly-silicon (poly-Si) gate depletion and boron penetration problems associated with conventional doped poly-Si gates need to be addressed. The metal gate is an attractive replacement for the poly-Si gate because it eliminates both gate depletion and boron penetration problems, and provides a lower gate sheet resistance [1]. It has been reported that metal gates with work functions close to the Si conduction and valence band edges are desired for the optimal design of bulk Si n- and p-MOSFETs, respectively [2]. Refractory metal nitrides (MN_x) such as TaN, TiN, HfN, and WN have been widely studied for gate electrode application [3], [4]. They are suitable to replace the poly-Si gate because of their thermal stability, excellent scalability, and compatibility with high-k dielectrics. Unfortunately, the work functions of most MN_x materials are close to the mid-gap position of Si after high-temperature annealing [5]. Possible reasons for this include Fermi level pinning [6], [7], the reaction between metal and dielectric, or the presence of oxygen vacancies at the metal gate/dielectric interface [8], [9]. In this paper, we report the work function tunability of MN_x (TaN and HfN) by incorporating lanthanum (La) and aluminum (Al). The compatibility of this work function tuning method with conventional high-temperature source/drain annealing is also investigated. Based on our results, we further propose several dual metal gate integration processes by incorporating lanthanide and aluminum into the gate stack with a refractory metal nitride gate electrode.

II. Experimental Details

(100) n- and p-doped $(6 \times 10^{15}\ cm^{-3})$ Si substrates were used in the MOS fabrication process. After active area definition and standard RCA clean, a thermal SiO_2 with four thicknesses (35 Å, 55 Å, 75 Å, and 95 Å) or a sputtered HfO_2 (50 Å) was deposited, wherein the thicknesses were evaluated by an ellipsometer. Subsequently, either $(Hf_xLa_{1-x})N_y$ or $(Ta_xAl_{1-x})N_y$ gate, followed by an *in situ* TaN capping layer, was deposited to complete the gate stack. The concentration of La in $(Hf_xLa_{1-x})N_y$ was controlled by varying the sputter

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TABLE I
PROCESS FLOW FOR MOS DEVICE FABRICATION

* Active area definition and RCA cleaning;
* Thermal oxidation SiO_2 with 4 thicknesses, or ~50 Å PVD HfO_2;
* 500 Å $(Hf_xLa_{1-x})N_y$ or $(Ta_xAl_{1-x})N_y$ gate reactive co-sputtering; For $(Hf_xLa_{1-x})N_y$ case, different La% was obtained by changing DC power for HfLa target with fixed Ar/N_2 flow rate (25/5 sccm) and DC power for Hf target (200 W); For $(Ta_xAl_{1-x})N_y$ case, different Al% was obtained by changing DC power for Al target with fixed flow rate of Ar/N_2 (25/5 sccm) and DC power for Ta target (450 W).
* In-situ TaN capping layer (1000 Å);
* Gate patterning;
* PMA (900°C, 950°C 30 sec or 1000°C 2 sec in N_2 ambient);
* Forming gas anneal (FGA) 30 min @420°C.

power ratio between the HfLa target and the Hf target. It is noteworthy that a HfLa target ($\mathrm{Hf:La} = 1:1$, atomic concentration) instead of a La target was used for $(\mathrm{Hf}_x\mathrm{La}_{1-x})\mathrm{N}_y$ deposition to reduce the moisture absorption of pure La [10]. For the $(\mathrm{Ta}_x\mathrm{Al}_{1-x})\mathrm{N}_y$ gate, the concentration of Al was controlled by varying the power ratio between the Ta target and the Al target. Post metallization annealing (PMA) splits were conducted by rapid thermal annealing at 900 °C to 1000 °C in N_2 ambient to study the thermal stability of the metal gates. The detailed process flow for this work is shown in Table I. The atomic concentrations of the ternary nitride gates were determined by X-ray photoelectron spectroscopy. Quantum-mechanical effects were taken into account when simulating the measured capacitance–voltage (C–V) curves for flatband voltage (V_{FB}) and effective oxide thickness (EOT) extraction.

III. EXPERIMENTAL RESULTS AND DISCUSSION

A. Lathanide (LA) Doped MN_x, $(M_xLa_{1-x})N_y$, for n-MOS

Fig. 1 shows the Auger electron spectroscopy (AES) analysis of $(\mathrm{Hf}_{0.70}\mathrm{La}_{0.30})\mathrm{N}_y$ composition in a MOS structure. There is an obvious difference in the N concentration at the TaN layer and the $(\mathrm{Hf}_{0.70}\mathrm{La}_{0.30})\mathrm{N}_y$ layer, which implies that N bonding with the HfLa alloy could be easier than that with the Ta metal. It is seen that an additional 900 °C anneal to the initial forming gas anneal (FGA) does not cause a significant change to the depth profile of the gate stack, highlighting the thermal stability of the gate stack at high annealing temperatures.

The modulation of V_{FB} with varying La concentration in $(\mathrm{Hf}_x\mathrm{La}_{1-x})\mathrm{N}_y/\mathrm{SiO}_2$/p–Si capacitors is shown in Fig. 2. The V_{FB} shifts toward the negative direction with the increase in La composition for $(\mathrm{Hf}_x\mathrm{La}_{1-x})\mathrm{N}_y$ gate electrodes. In addition, the excellent fit of the simulated C–V curve to the measured C–V curves confirms that the SiO_2/Si substrate interface quality was not degraded with La incorporation.

Fig. 3 shows the relationship between V_{FB} and EOT, which was obtained from the C–V curves of $(\mathrm{Hf}_x\mathrm{La}_{1-x})\mathrm{N}_y/\mathrm{SiO}_2$/p–Si capacitors by varying the SiO_2 thicknesses. Based on the following equation:

$$\Phi_M = \Phi_{\mathrm{Si}} + V_{\mathrm{FB}} - \frac{Q_{\mathrm{OX}}}{C_{\mathrm{OX}}} \tag{1}$$

where Φ_M and Φ_{Si} are the work functions of the metal gate and the Si substrate, respectively, Q_{OX} is the equivalent oxide charge per unit area, and C_{OX} is the oxide capacitance, the Φ_M's of $(\mathrm{Hf}_x\mathrm{La}_{1-x})\mathrm{N}_y$ with different La compositions were extracted and shown in Fig. 3. It can be seen that with the increase in La composition for the $(\mathrm{Hf}_x\mathrm{La}_{1-x})\mathrm{N}_y$ gate, the Φ_M decreases continuously down to a value of 3.91 eV for the $(\mathrm{Hf}_{0.61}\mathrm{La}_{0.39})\mathrm{N}_y$ gate.

From the V_{FB} versus EOT plot in Fig. 3, we found that the magnitude of Q_{OX} does not significantly change for $(\mathrm{Hf}_x\mathrm{La}_{1-x})\mathrm{N}_y$ metal gates with different La compositions. However, the polarity of Q_{OX} changes from positive to negative with increasing La composition. The extracted EOTs for all the gate stacks were also found to be thinner than the original SiO_2 thicknesses. Fig. 4 shows the cross-sectional transmission electron microscopy (TEM) for a $(\mathrm{Hf}_{0.70}\mathrm{La}_{0.30})\mathrm{N}_y/\mathrm{SiO}_2/\mathrm{Si}$ gate stack after 900 °C 30-s PMA. It is seen that the formation of an interfacial layer occurred between the metal gate and the underlying SiO_2 after high-temperature anneal. In addition, the SiO_2 physical thickness (~23.5 Å) after annealing was found to be thinner than the deposited SiO_2 thickness. The depth profile by energy-dispersive X-ray spectroscopy (EDX) for the same gate stack [Fig. 5(a)] shows the intermixing of La and Hf with the original SiO_2 layer. In contrast, Fig. 5(b) shows the $\mathrm{HfN/SiO_2}$ gate stack, whereby no obvious Hf diffusion into the SiO_2 layer was detected. Therefore, the interfacial layer formed was probably a metal silicate with a higher k value. This explains the reduction of EOT as extracted by C–V curves. In addition, the intermixing of La (or Hf) with SiO_2 may also be the root reason for the change of Q_{OX} polarity (as shown in Fig. 3) due to the introduction of negative charges in the dielectric layer. These phenomena were also observed when other lanthanide elements were incorporated into another refractory metal nitride, i.e., TaN [12]. Fig. 6 shows that La incorporation in $(\mathrm{Hf}_x\mathrm{La}_{1-x})\mathrm{N}_y$ improves the leakage current by approximately two to three orders when compared with a conventional poly-Si/SiON stack. This was attributed to the increase in dielectric physical thickness due to the high-k layer formation (metal silicate) between the gate electrode and the SiO_2 layer.

Fig. 7 summarizes the work function values of $(\mathrm{Hf}_x\mathrm{La}_{1-x})\mathrm{N}_y$ metal gates with varying La composition under different annealing conditions. It can clearly be seen that the work function of the HfN metal gate is continuously modulated from 4.6 to 3.9 eV by changing the La composition in the $(\mathrm{Hf}_x\mathrm{La}_{1-x})\mathrm{N}_y$ metal gate. This is stable after 900 °C to 1000 °C anneal, and the excellent thermal stability could be related to the enhanced N content in the $(\mathrm{Hf}_x\mathrm{La}_{1-x})\mathrm{N}_y$ films. Fig. 8 compares the work function data from this paper and our previous work [13] for LA-doped refractory metal nitrides on a SiO_2 gate dielectric after a 1000 °C anneal. It can be seen that a wide work function tunability can be obtained by the incorporation of La into refractory metal nitride gates.

In addition to the investigation of work function tunability for $(\mathrm{M}_x\mathrm{LA}_{1-x})\mathrm{N}_y/\mathrm{SiO}_2$ gate stacks, the work function modulation for a $(\mathrm{M}_x\mathrm{LA}_{1-x})\mathrm{N}_y$/Hf-based high-$k$ dielectric by lanthanide incorporation into TaN is also shown in Fig. 9.

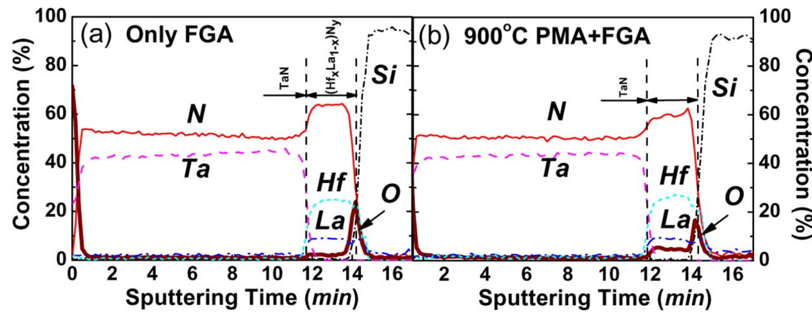

Fig. 1. AES depth profiles of the $TaN/(Hf_{0.70}La_{0.30})N_y/SiO_2$ gate stack. (a) FGA only. (b) 900 °C PMA for 30 s and FGA.

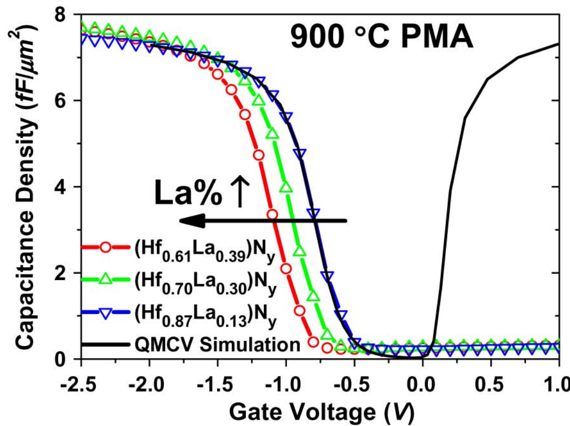

Fig. 2. Typical 100-kHz C–V curves of MOS capacitors with $(Hf_xLa_{1-x})N_y$ grown on SiO_2 after 900 °C PMA annealing. With the increase of La% in $(Hf_xLa_{1-x})N_y$, V_{FB} shifts to a more negative direction.

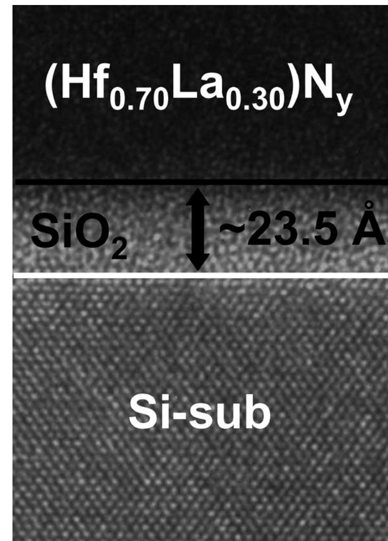

Fig. 4. Cross-sectional TEM for $(Hf_{0.70}La_{0.30})N_y/SiO_2/Si$ gate stack after 900 °C 30-s PMA.

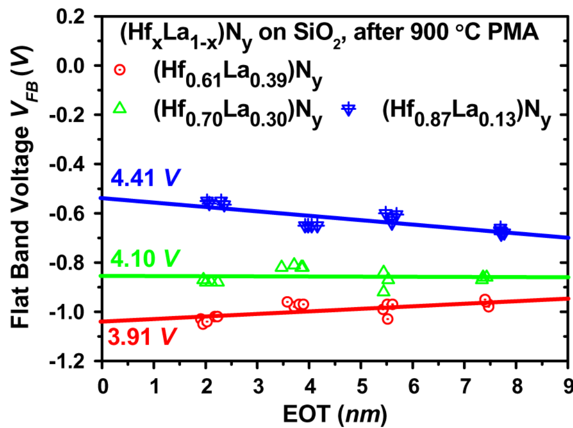

Fig. 3. V_{FB} versus EOT extracted from C–V curves for different La compositions in $(Hf_xLa_{1-x})N_y$ metal gates after 900 °C annealing. The metal work function Φ_M was extracted by extrapolating the line to eliminate the contribution of fixed oxide charges.

About 0.31 V V_{FB} shift can be seen with the 10% Tb incorporation into TaN when using HfAlO as the gate dielectric, which is possibly due to the low bulk work function of Tb (∼3.1 eV). A similar work function tunability was also reported for $(M_xLA_{1-x})N_y$/HfSiON gate stacks [12], which indicates the good compatibility of La-incorporated metal nitrides with high-k dielectrics.

B. Aluminum Doped MN_x, $(M_xAl_{1-x})N_y$, for p-MOS

As previously reported, the doping of aluminum into MN_x could tune the work function to a p-type band edge on SiO_2 dielectric [14], [15], and the key experimental results are summarized in Fig. 10. It is observed that with the increase of Al% in $(M_xAl_{1-x})N_y$, the work function is modulated toward the Si valence band edge and with good thermal stability up to 1000 °C.

The compatibility of $(M_xAl_{1-x})N_y$ work function tunability on a HfO_2 high-k dielectric is further investigated. Fig. 11 shows the typical C–V curves of $(Ta_xAl_{1-x})N_y/HfO_2$ capacitors fitted with the simulated C–V curve. A positive V_{FB} shift of ∼250 mV was seen after 24% Al incorporation, which reflects the approximate effective work function change of the metal gate.

C. Possible Dual Metal Gate Integration Processes for CMOS

The integration of metal gates with two different Si band edge work functions on high-k dielectrics has been a challenging task. Samavedam *et al.* reported the long channel device integration of TiN and TaSiN on HfO_2 [16]. The integration of TaSiN (nMOS) and Ru (pMOS) on HfO_2 by selectively

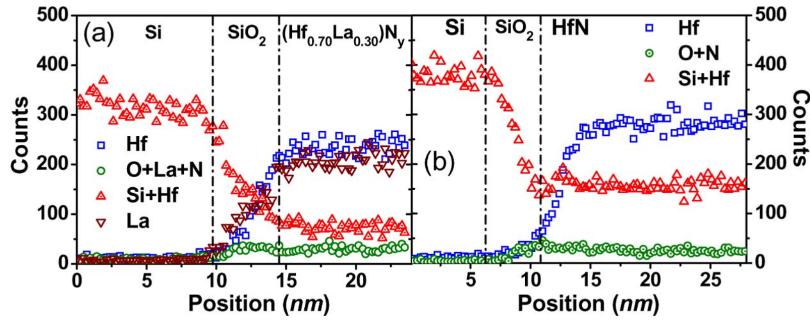

Fig. 5. EDX depth profile for (a) $(Hf_{0.70}La_{0.30})N_y/SiO_2/Si$ gate stack and (b) $HfN/SiO_2/Si$ gate stack. Intermixing of La and Hf with SiO_2 was found in (a), while no Hf diffusion into SiO_2 was detected in (b).

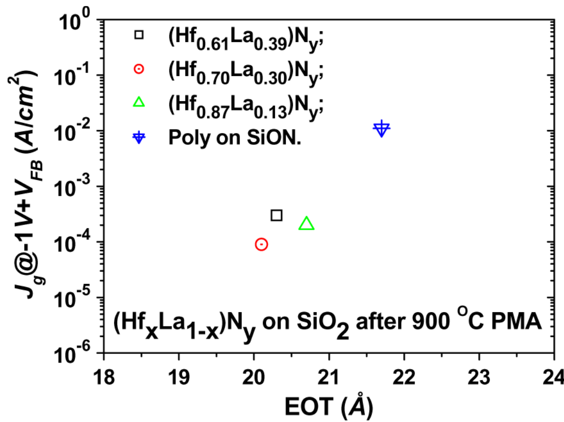

Fig. 6. Gate leakage current comparison of $(Hf_xLa_{1-x})N_y/SiO_2$ gate stacks with poly-Si/SiON gate stack. A two- to three-order lower J_g at the same EOT was obtained for $(Hf_xLa_{1-x})N_y/SiO_2$ gate stacks due to the formation of a high-k layer.

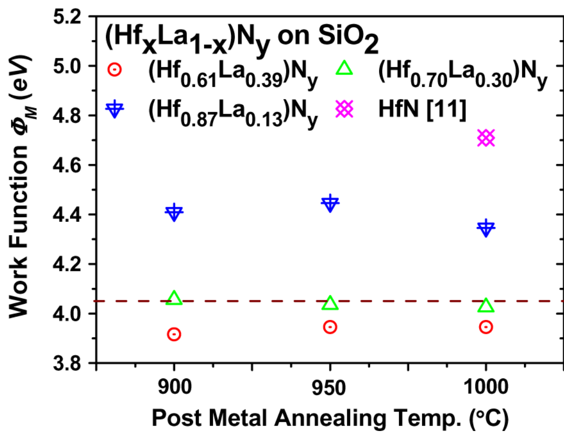

Fig. 7. Summary of the Φ_M values for $(Hf_xLa_{1-x})N_y/SiO_2$ capacitors with varying La composition under different annealing conditions. The Φ_M of HfN can be continuously modulated from 4.6 to 3.9 eV by changing the La composition in $(Hf_xLa_{1-x})N_y$ film.

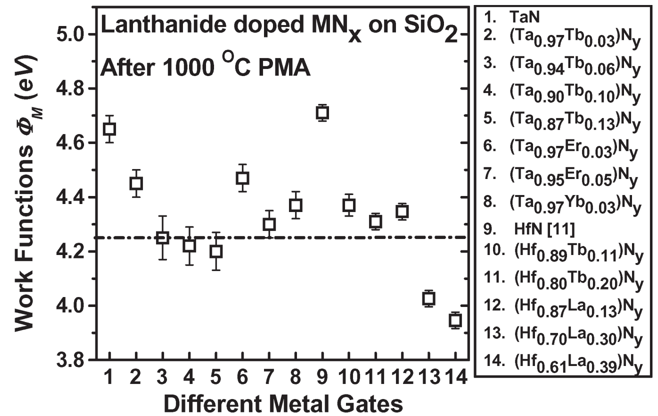

Fig. 8. Summary of Φ_M for LA-doped MN_x on SiO_2 after 1000 °C PMA. The effect of lanthanide on Φ_M tunability is clearly seen.

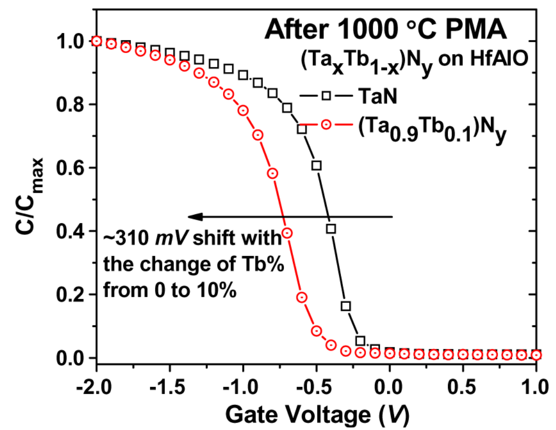

Fig. 9. C–V curves of $(Ta_xTb_{1-x})N_y$/HfAlO/Si MOS capacitors with different Tb composition after 1000 °C PMA. The V_{FB} shift indicates the Φ_M difference of the metal gates.

wet etching TaSiN using a TEOS hard mask was also demonstrated [17]. However, in both schemes, the exposure of the high-k films to a series of wet chemical processes might degrade the integrity of the dielectric. Therefore, recent schemes demonstrate dual high-k and dual metal gate CMOSFETs to avoid the damage of a high-k layer during processes [18]. Here, we propose several alternative integration processes for dual metal gate CMOS technology by incorporating lanthanide and aluminum into the gate stack with MN_x gate electrode. First, since the feasibility of implanting Al and other lanthanide ions has been recently demonstrated for Ni-based FUSI gate electrodes, respectively [19], [20], this would also bring the possibility to implement lanthanide and aluminum incorporation by ion implantation into a single MN_x gate electrode directly or thin MN_x layer involved in the metal-inserted poly-Si stack.

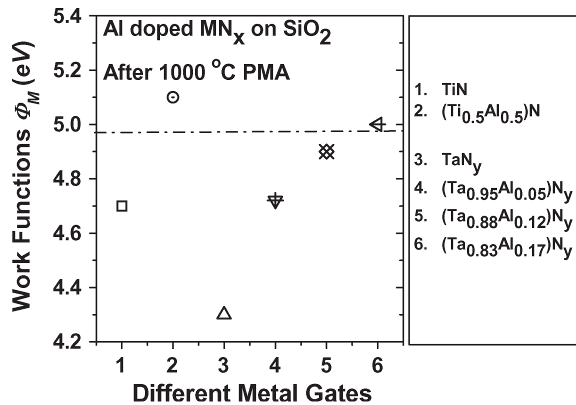

Fig. 10. Φ_M summary for aluminum-doped MN_x on SiO_2 after 1000 °C PMA from previous works. The effect of aluminum on Φ_M tunability is clearly seen.

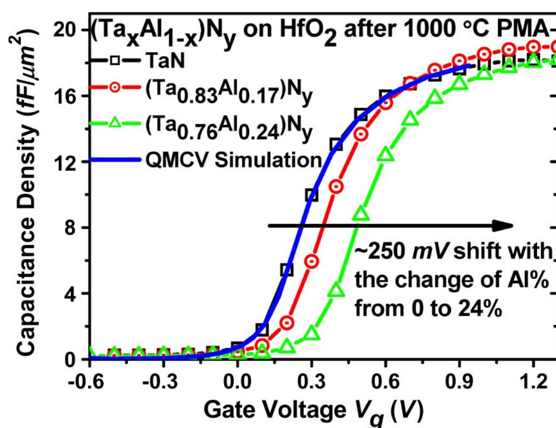

Fig. 11. C–V curves of $(Ta_xAl_{1-x})N_y/HfO_2/Si$ MOS capacitors with different Al compositions after 1000 °C PMA. V_{FB} shifts to a more positive direction with the incorporation of Al into TaN due to the Φ_M difference among these metal gates.

In addition, the ion implantation process could be simplified by depositing the $(M_xLa_{1-x})N_y$ [or $(M_xAl_{1-x})N_y$] electrode on a whole wafer, followed by selectively implanting Al (or La) ions into the p- (or n-) MOS region. Also, the incorporation process can be implemented by previously reported technologies, such as single dielectric and dual metal gate [17] or dual dielectric and dual metal gate [18].

IV. Conclusion

In this paper, we have reported the work function tunability by incorporating lanthanum and aluminum into MN_x on both SiO_2- and HfO_2-based dielectrics with good thermal stability. Based on our results and previous data, we propose several integration processes for dual metal gate CMOS technology.

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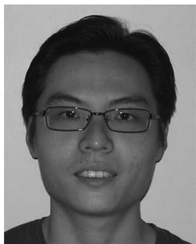

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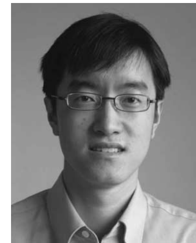

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