行政院國家科學委員會補助專題研究計畫□期中進度報告

■期末報告

低成本矽製程毫米波雙降頻傳收機

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□國際合作研究計畫國外研究報告

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中　華　民　國　101 年　10 月　14 日

I、Abstract

In the first year, we focus on the analysis and the design methodology of the step-impedance phase-inverter rat-race coupler on silicon-based process. The issues of impedance limitation and bandwidth are discussed in detail. Our proposed concept utilizes high silicon dielectric constant, phase-inverter structure, step-impedance technique and Chebyshev response to make the rat-race coupler more compact (~ 64% reduction) and highly balanced over a wide operating bandwidth. Moreover, the inter-digital coplanar stripline (CPS) used in the step-impedance section effectively reduces the characteristic impedance of the transmission line for large size shrinkage and reduction of insertion loss.

In the second year, we propose a concept for the miniaturization of microwave components according to the theory of distortion-less transmission line. A broadband Gilbert down-converter with a phase-inverter rat-race coupler directly on lossy silicon substrate is demonstrated using standard silicon technology. By high silicon dielectric constant, lumped-distributed structure and band-broadening technique, a large shrinkage ratio with wide bandwidth of Chebyshev response can be simultaneously attained in the spiral-shape coplanar-stripline (CPS) phase-inverter rat-race coupler. The area of the demonstrated lumped-distributed phase-inverter rat-race coupler is 0.65x0.65 mm2 and the experimental bandwidth is from 2.5 to 12.5 GHz. As a result, a broadband Gilbert downconverter with the proposed coupler achieves a conversion gain of 11~12 dB, IP1dB of -11 dBm, IIP3 of -1 dBm and noise figure of 16 dB.

Then, a 60-GHz dual-conversion down-converters with Schottky diodes are realized by using 0.18-μm foundry CMOS technology. A new Schottky-diode mixer, down-conversion sub-harmonic mixer with a dual-band lump-distributed phase-inverter rat-race coupler (also directly on lossy silicon substrate), is realized and employed at the high-frequency conversion stage of the dual-conversion architecture to achieve small size and broadband isolation. The silicon-based Schottky diode with a low turn-on voltage offers great advantage in LO pumping power, especially for an anti-parallel diode pair structure. In our Schottky-diode sub-harmonic mixers, the required LO power is only 1 dBm. The dual-conversion down-converter achieves 5-dB conversion gain and 19 dB noise figure under V_{dd}=2.5 V and I_{dd}= 22 mA.

In the third year, a 60-GHz dual-conversion up-converters with Schottky diodes are realized by using 0.18-mm foundry CMOS technology. A $CoSi_2$-Si Schottky diode, fabricated on a lower doped N-well by blocking the threshold voltage adjustment implant, has a lower reverse leakage current and a better ideality factor. Thus, it is ideal for the 60-GHz sub-harmonic mixer design. Two new types of Schottky-diode mixers, a down-conversion sub-harmonic mixer with a dual-band lump-distributed phase-inverter rat-race coupler and an up-conversion sub-harmonic mixer with a trifilar transformer, are realized and employed at the high-frequency conversion stage of the dual-conversion architecture to achieve small size and broadband isolations. The silicon-based Schottky diode with a low turn-on voltage offers great advantage in LO pumping power, especially for an anti-parallel diode pair structure. and the dual-conversion up-converter, with V_{dd}=2.5 V and I_{dd}= 26 mA, attains greater than 40-dB sideband rejection and -1 dB conversion gain over the whole 60-GHz bandwidth.

II、Introduction

1st year

As the speed of CMOS technology increases by device scaling in the past decades, a new silicon microwave and millimeter-wave IC era has finally begun. Because quarter-wave-length based passive components greatly shrink at high frequency, 180° hybrids can be integrated in silicon-based circuits, such as balanced amplifiers [A1], balanced mixers [A2,A3], multipliers, phase shifters [A4, A5], and beam-forming systems [A6]. Among all of the 180° hybrids, Marchand baluns and rat-race couplers are popularly utilized in conventional microwave and

millimeter-wave circuits. Especially, the rat-race couplers can simultaneously provide balanced signals, all-port matching condition and good isolation.

In a conventional rat-race coupler, the total electrical length of the circumference, consisting of one 3λ/4 and three λ/4 sections, is 1.5 λ and keeps balanced outputs only at a certain frequency [A7]. In order to reduce size, 1.25 λ (7/6 λ) rat-race coupler [A8] with 1/8 λ (1/6 λ) sections was utilized to replace the conventional 1.5 λ rat-race coupler at the cost of bandwidth reduction. The formidable larger area makes the inclusion of a rat-race coupler in IC design unrealistic. By using lumped elements, the size of rat-race couplers can be effectively reduced [A9]. However, it is difficult to have high-quality, lumped inductors at high frequencies in silicon IC process. Many efforts have been devoted to design rat-race couplers with smaller size and wider bandwidth at the same time, such as the method of opposing short-circuit end [A10] and twisting-connection [A11]. These methods are proposed to replace the 3λ/4 section, which forms the embryo of a phase inverter. The phase is inherently inverted for all operating frequencies and the bandwidth of a phase-inverter, rat-race coupler is determined by the input return loss. Wang et al [A12] analyzed a phase-inverter rat-race coupler with an arbitrary output power-split ratio and band-broadening design under the lossless condition. A wider bandwidth can be achieved by selecting the impedance of each arm for a Chebyshev response by adjusting the characteristic impedance below [A13].

Because the standard CMOS process has no inherent backside ground for signal guiding, microstrip lines formed by interconnect metals are employed to implement λ/4-based hybrids [A14][A15]. The substrate loss is shielded by the ground plane formed by the metal-1 layer. E-band phase-inverter rat-race couplers are implemented by this technique, and the length of each arm at 77 GHz center frequency is up to 320 μm [A15]. The hybrid size is large because the inter-metal dielectric has a low dielectric constant. Moreover, the microstrip line still suffers from some metal loss because the thin dielectric results in a narrow top metal. On the other hand, thin ground metal also results in poor ground quality. Recently, the phase-inverter rat-race coupler on a lossy silicon substrate was first demonstrated by our group to reduce the size by high effective dielectric constant at the cost of insertion loss [A16]. The phase-inverter, rat-race coupler in our previous work [A16] was only utilized at the LO port of a Gilbert mixer instead of the RF signal path for broadband operation. Because the noise figure in the RF signal path is sensitive to loss, a step-impedance phase-inverter rat race coupler with less insertion loss prevails.

In this work, a low-loss, phase-inverter, rat-race coupler employed at the RF signal path uses step-impedance technique to mitigate its impact on the noise figure of a receiver [A17]. The proposed concept utilizes high dielectric constant of silicon, phase inverter, step-impedance structure and Chebyshev response to achieve compact, wide bandwidth and low loss at the same time for an integrated rat-race coupler. The arm lengths of 10-GHz, step-impedance, phase-inverter, rat-race couplers in this work have large size reduction and only need a nearly half of the equivalent length if compared with a 10-GHz microstrip line using inter-connect metal as ground. We also implement a Gilbert down-converter incorporating the proposed rat-race coupler at the RF input in 0.13-μm standard CMOS process. From the measured results, the size-reduction rat-race coupler with lower loss successfully converts the input signal into Gilbert mixer core without serious noise figure degradation.

THEORY OF A STEP-IMPEDANCE RAT-RACE COUPLER

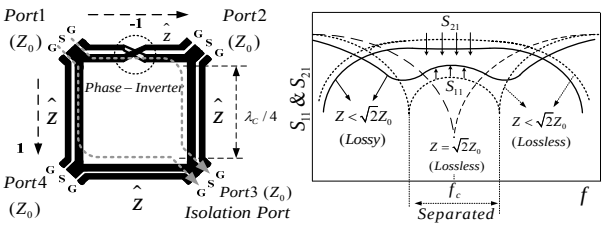


Fig. 1. (a) Operational principle of a phase-inverter rat-race coupler and (b) bandwidth design of a rat-race coupler with phase-inverter directly on the lossy substrate.

Referring to Fig. 1(a), the phase inverter, twisting the signal (S) and ground (G) paths of a coplanar stripline

(CPS), together with a quarter wavelength section not only takes the place of the three-quarter wavelength section for size-reduction, but also provides a differential signal between port-2 and port-4 over all operating frequencies in a rat-race coupler. It is because the signal paths from port 1 (Δ port) to port-2/port-4 are equal geometrically. Thus, the bandwidth is limited by the input matching instead of magnitude/phase imbalance. The bandwidth design (matching types), closely relating to the characteristic impedance and attenuation constant of transmission line (TL), will be discussed in the following sections.

A. Characteristics of Lossy Transmission Line of a Phase-Inverter Rat-Race Coupler

By applying an even- and odd-mode analysis to a phase-inverter, rat-race coupler under lossy condition, the closed-form expressions of the complex S-parameter for return loss, insertion loss and isolation can be obtained from our previous work [A16]. The relation between the characteristic impedance of each arm and the bandwidth of the return-loss can thus be explored under the lossy condition. As derived in Appendix A, the expression is further simplified as follows,

$$\hat{z} = \sqrt{2 + 2\coth^2(\gamma\ell)} = \hat{z}_{re} + j\hat{z}_{im} = \left|\hat{z}\right| \exp\left(j \tan^{-1} \frac{\hat{z}_{im}}{\hat{z}_{re}}\right) \quad (1)$$

where

$$\gamma\ell = (\alpha + j\beta)\ell = \alpha\left(\frac{\lambda_c}{4}\right) + j\frac{2\pi}{\lambda_o}\left(\frac{\lambda_c}{4}\right) = \alpha\left(\frac{\lambda_c}{4}\right) + j\frac{2\pi}{4}\left(\frac{f_o}{f_c}\right)$$

$\hat{z}$ is the normalized characteristic impedance of the CPS TL and consists of the real part $\hat{z}_{re}$ and imaginary part $\hat{z}_{im}$. The termination impedance of each port is as shown in Fig. 1(a). λ_C is the effective wavelength of each arm of the rat-race coupler at the center frequency, f_C. Here, fo is the frequency at matching point, α is the attenuation constant and β is the phase constant, respectively. Based on (1), the normalized amplitude and imaginary part of the characteristic impedance as a function of the normalized frequency and attenuation constant are plotted in Fig. 2(a) and 2(b), respectively. Here, f_C is chosen at 10 GHz, for example. If under a lossless condition, $\alpha = 0$ and thus $\hat{z}$ becomes

$$\hat{z} = \sqrt{2\left[1 + \coth^2(\alpha + j\beta)\ell\right]}\Big|_{\alpha=0} = \sqrt{2(1 - \cot^2\theta)} \quad (2)$$

, which is a well-known formula for the lossless condition [A12]. Here $\theta = \beta\ell$. For a Butterworth-response input matching, there is only one matching point frequency at a given attenuation constant. The required for different attenuation constant is along the axis of *f*o / f_C =1 on the 3-D curve of Fig. 2(a). Under the condition of *f*o=f_C, the minimum of $\hat{z}$ for a lossless condition is $\sqrt{2}$ and the maximum increases to 2 as loss goes toward infinity. The one matching point condition with loss was also described in our previous work [A16]. The matching bandwidth can be extended by designing $|\hat{z}|$ below $\sqrt{2}$ to achieve a Chebyshev-response input matching with two matching-point frequencies [A12]. The input matching bandwidth extension holds true even for a lossy condition as shown in Fig. 2(a). The curve corresponding to (1) in Fig. 2(a) bends downwards and is symmetrically stretched to both sides of *f*o / f_C =1 axis when loss increases; thus, the distance (Δ*f*) of two matching dip points is increased as depicted in Fig. 1(b). For instance, if the normalized characteristic impedance of each arm is chosen as 1.2 (~60 Ω), the bandwidth ratio of fmax / fmin is equal to 1.85 (fmax / f_C =1.3 and fmin / f_C =0.7) under α=0 as indicated in Fig. 2(a). The dip points at Fig. 1(b) can be obtained by intersecting the curve in plane A and the reference plane. When α increases to 1 Np/cm, the curve of equation (1) is projected in plane B. The bandwidth ratio of fmax / fmin, obtained by intersecting the curve in plane B and reference plane, is extended to 2.1. However, the bandwidth extension when loss is concerned is at the cost of higher insertion loss and smaller return loss, as shown in Fig. 1(b).

Under the lossy condition, in general a TL such as each arm of a rat-race coupler has a complex characteristic impedance. A complex characteristic impedance can be represented by a transmission line model with

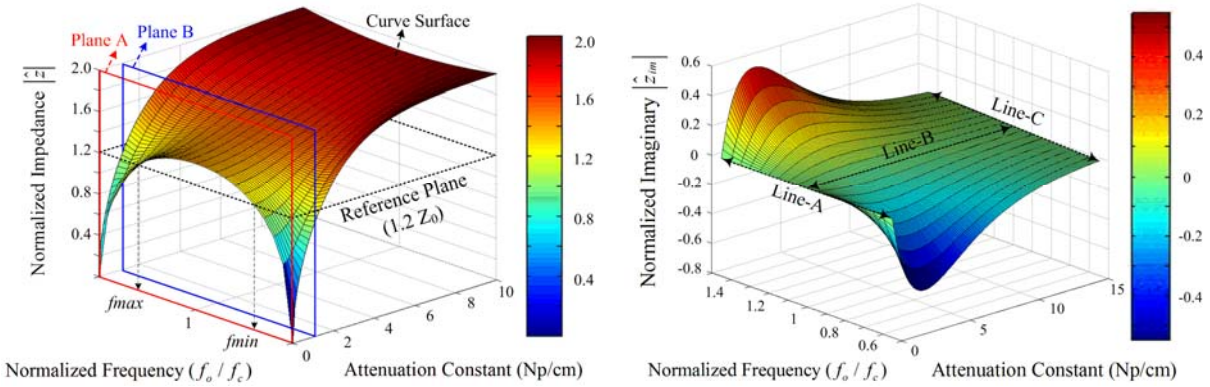


Fig. 2. (a) The normalized amplitude (| |) and (b) imaginary part ( ) of the characteristic impedance designed in the each arm of the phase-inverter rat-race coupler with respect to different loss conditions and normalized frequency (the frequencies of matching dips are normalized to the center frequency).

$$Z = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \qquad (3)$$

Here R, L, G, and C are the unit-length resistance, inductance, conductance and capacitance of the TL. It is interesting to note that the imaginary part becomes zero if the TL is designed under three special cases. As shown in Fig. 2(b), these special cases are indicated by line-A, -B and –C. The conditions for a pure real characteristic impedance in Fig. 2(b) are listed as follows,

1. $R = G = 0$, the lossless condition is along line-A. The characteristic impedance is always a real number unless the degree (θ) of matching point exceeds 45° [A12].

2. $\frac{R}{L} = \frac{G}{C}$, the distortionless TL is along line-B. Under this condition, the attenuation constant is equal for all frequencies and the phase constant is also a linear function of operating frequency. There exists an inherently-perfect matching point in the return-loss response, which is the well-known Butterworth matching condition.

3. $R \to \infty$, $G \to \infty$, the region is located at the line C and behind line C ($\alpha \to \infty$). However, the high metal loss ($R \to \infty$) and substrate loss ($G \to \infty$) make the insertion loss of a rat-race coupler too large to be utilized.

Strictly speaking, Chebyshev response under lossy condition cannot be achieved with a real characteristic impedance. However, there exists a quasi-real characteristic impedance region defined by the ratio of |Zim|/|Z|, as depicted in Fig. 3. A Chebyshev response can be designed inside the shade region because of the small imaginary impedance (|Zim|/|Z|<0.1).

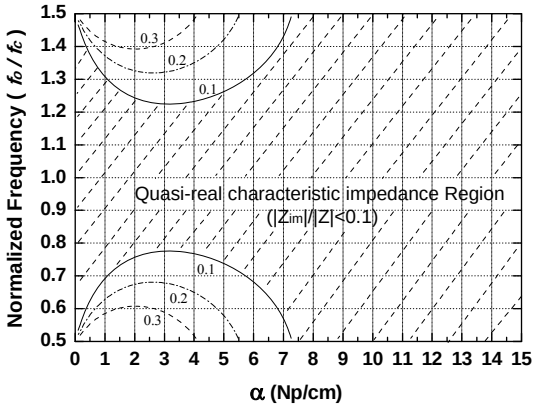
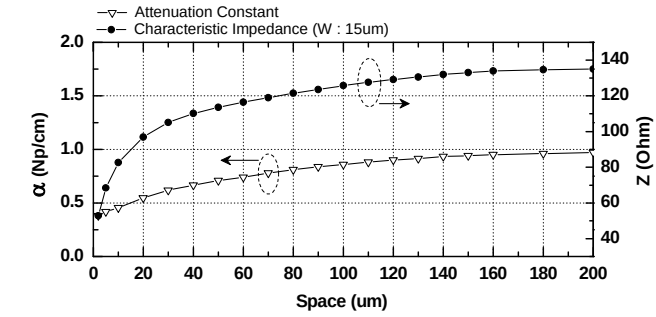


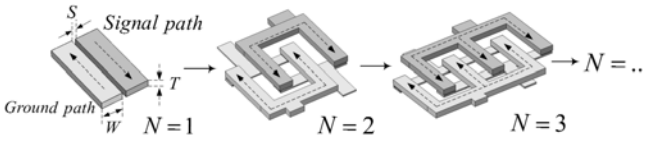
Fig. 3. The quasi-real characteristic impedance region of TL of each arm in the phase-inverter rat-race coupler.

B. Multi-Finger CPS for Large Size Reduction on a Silicon-Based Process

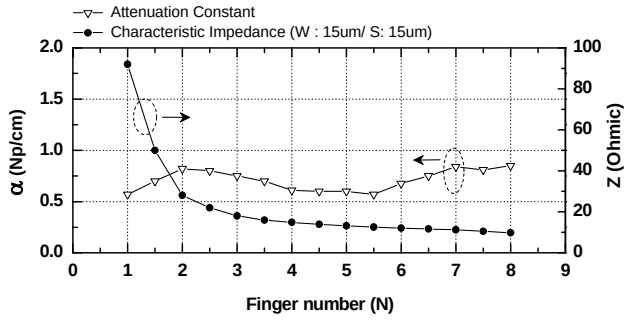
A step-impedance technique is utilized in this paper to reduce the length of a phase-inverter rat-race coupler and loss can be reduced due to shorter transmission line. Here, a high impedance ratio in a step-impedance structure facilitates the size reduction. For 0.13 μm standard CMOS process, the realizable microstrip line impedance formed by interconnect metals ranges from 28 Ω to 77 Ω. The small impedance ratio (~2.75) is a disadvantage for the step-impedance design. In this work, a coplanar stripline directly on silicon substrate is adopted for size reduction because a higher effective dielectric constant results in a shorter effective wavelength. The achievable impedance level is controlled by adjusting the width and spacing of the coplanar stripline because most EM-field is well confined between the adjacent metals. According to 0.13 μm CMOS design rule, the thickness, minimum spacing and maximum width of metal-8 are 3.3 μm, 2



(a)



(b)



(c)

Fig. 4. The EM simulated characteristic impedance and attenuation constant of (a) CPS for various spacing and that of (c) inter-digital CPS for different finger-number. (b) The structure of inter-digital CPS.

μm and 30 μm, respectively. By Sonnet EM simulation [A22], a 15 μm width of CPS with the spacing of 2 μm has a characteristic impedance of 52.8 Ω. If the metal is widened to 30 μm under the same spacing, the minimum characteristic impedance is only reduced to 45 Ω. It is because most of EM-field in the CPS is merely kept at the edge of the metal, and a wider metal does not help to reduce the characteristic impedance. The top layer metal, metal-8, is utilized to reduce the metal loss for the rat-race coupler. The resistivity of silicon substrate is 10 Ω-cm and the thickness of the SiO2 layer is 8 μm. By increasing the slot width, more fields are in the silicon, which increases the loss. As shown in Fig. 4(a), the impedance and attenuation constant both increase as the metal spacing increases. When the metal spacing is larger than 200 μm, the maximum impedance saturates to around 135 Ω. The parameter extraction is according to the reference [A20].

In order to obtain lower characteristic impedance, multi-finger coplanar striplines are positioned side by side to form the inter-digital structure, as shown in Fig. 4(b). The interval and width of each finger are 15 μm. Thick top-layer metal is employed to form the multi-finger structure for lower metal loss, and low-layer metals connect the fingers of the adjacent cells. By using an inter-digital structure, the lowest characteristic impedance shown in Fig. 4(c) is further reduced from 45 Ω to 10 Ω, and the realizable high-to-low impedance ratio is greatly extended from 3 to 13.5. Here, the attenuation constant is nearly constant. In the multi-finger CPS, the effective dielectric constant of a coplanar transmission line is not only determined by the surrounding dielectric, but also by the geometric structure, such as the spacing, width or finger number. The equivalent capacitance between the signal and ground paths increases with finger number, and the effective dielectric constant (ε_{eff}) in the low-impedance section becomes higher to greatly make the TL length shorter.

C. The Relationship between the Step-Impedance Technique and Chebyshev Response Design

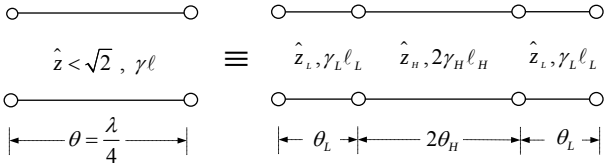


Fig. 5. A low-high-low step-impedance transmission line is equivalent to a lossy quarter-wavelength transmission line. The normalized characteristic impedance is smaller than $\sqrt{2}$ for a Chebyshev response.

Based on the realization of a low impedance section by the multi-finger CPS structure, the step-impedance technique becomes more suitable for large shrinkage in the silicon-based

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cosh(\gamma_L\ell_L) & \hat{z}_L \sinh(\gamma_L\ell_L) \\ \frac{1}{\hat{z}_L}\sinh(\gamma_L\ell_L) & \cosh(\gamma_L\ell_L) \end{bmatrix} \begin{bmatrix} \cosh(2\gamma_H\ell_H) & \hat{z}_H \sinh(2\gamma_H\ell_H) \\ \frac{1}{\hat{z}_H}\sinh(2\gamma_H\ell_H) & \cosh(2\gamma_H\ell_H) \end{bmatrix} \begin{bmatrix} \cosh(\gamma_L\ell_L) & \hat{z}_L \sinh(\gamma_L\ell_L) \\ \frac{1}{\hat{z}_L}\sinh(\gamma_L\ell_L) & \cosh(\gamma_L\ell_L) \end{bmatrix} \quad (4)$$

$$A \text{ or } D=\cosh^2(\gamma_L\ell_L)\cosh(2\gamma_H\ell_H)+\frac{\hat{z}_L}{\hat{z}_H}\sinh(\gamma_L\ell_L)\sinh(2\gamma_H\ell_H)\cosh(\gamma_L\ell_L)+\frac{\hat{z}_H}{\hat{z}_L}\sinh(\gamma_L\ell_L)\sinh(2\gamma_H\ell_H)\cosh(\gamma_L\ell_L)+\sinh^2(\gamma_L\ell_L)\cosh(2\gamma_H\ell_H) \quad (5a)$$

$$B=2\hat{z}_L\sinh(\gamma_L\ell_L)\cosh(\gamma_L\ell_L)\cosh(2\gamma_H\ell_H)+\frac{\hat{z}_L^{\,2}}{\hat{z}_H}\sinh^2(\gamma_L\ell_L)\sinh(2\gamma_H\ell_H)+\hat{z}_H\sinh(2\gamma_H\ell_H)\cosh^2(\gamma_L\ell_L) \quad (5b)$$

$$C=\frac{2}{\hat{z}_L}\sinh(\gamma_L\ell_L)\cosh(\gamma_L\ell_L)\cosh(2\gamma_H\ell_H)+\frac{\hat{z}_H}{\hat{z}_L^{\,2}}\sinh^2(\gamma_L\ell_L)\sinh(2\gamma_H\ell_H)+\frac{1}{\hat{z}_H}\sinh(2\gamma_H\ell_H)\cosh^2(\gamma_L\ell_L) \quad (5c)$$

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}=\begin{bmatrix} \cosh(\gamma\ell) & \hat{z}\sinh(\gamma\ell) \\ \frac{1}{\hat{z}}\sinh(\gamma\ell) & \cosh(\gamma\ell) \end{bmatrix}_{\ell=\lambda/4}$$
$$=\begin{bmatrix} j\sinh\left(\frac{\lambda}{4}\alpha\right) & j\hat{z}\cosh\left(\frac{\lambda}{4}\alpha\right) \\ j\frac{1}{\hat{z}}\cosh\left(\frac{\lambda}{4}\alpha\right) & j\sinh\left(\frac{\lambda}{4}\alpha\right) \end{bmatrix} \quad (6)$$

IC. As shown in Fig. 5, a lossy quarter-wavelength transmission line is replaced by a low-high-low step-impedance structure, and the corresponding ABCD matrix for the lossy condition is expressed as (4). Here, γ_H is the propagation constant and $2\ell_H$ is the length of the high impedance ($\hat{z}_H$) section while γ_L is the propagation constant and ℓ_L is the length of the low impedance ($\hat{z}_L$) section. The equivalent ABCD matrix of the imitated lossy λ/4 transmission line at the center frequency can be simplified as (6). Here, γ is the propagation constant and is the length of the imitated lossy λ/4 transmission line section. Thus, the elements of A or D expressed in (6) are equivalent to $j\sinh(\frac{\lambda}{4}\alpha)$ for the lossy condition. For replacing the quarter-wavelength section by a step impedance section, the ABCD of low-high-low step-impedance section in (5) is equivalent to that of a lossy λ/4 transmission line section in (6). Based on the derivation in Appendix C, θL is a function of θH as described in (C.3). The degrees of $\theta_H+\theta_L$ with respect to θH for different impedance ratios ($R=\hat{z}_H/\hat{z}_L$) are plotted in Fig. 6(a), for the lossless ($\alpha=\alpha_H=\alpha_L=0$) [A19] and lossy ($\alpha=\alpha_H=\alpha_L\neq 0$) conditions. When the impedance ratio of increases, $\theta_H+\theta_L$ becomes smaller. The minimum length for different impedance ratios (R) are along the curve-1 in Fig. 6(a) and always occur under $\theta_H=\theta_L$ [A19]. If compared with the minimum ratio of R=1.5, the degree of $\theta_H+\theta_L$ at R=8 is greatly reduced from 43.8° to 26°, and the total size reduction is about 65 %. However, the shrinkage ratio decreases slightly under lossy conditions. When the loss increases, the total degree of $\theta_H+\theta_L$ becomes larger.

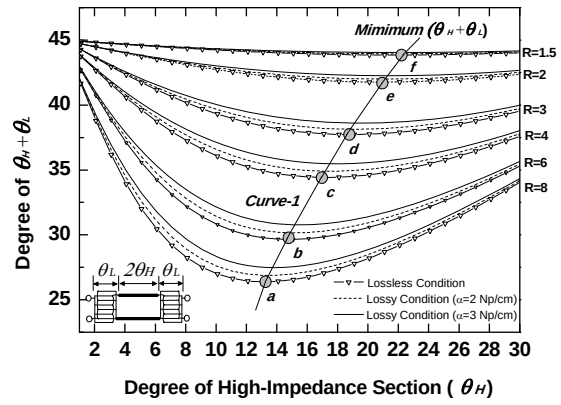
The impedance ratio of R for the step-impedance technique inherently has a maximum value due to the limitation of the realizable impedance ($\hat{z}_{H(MAX)}$ and $\hat{z}_{L(MIN)}$). $\hat{z}_H/\hat{z}$ and $\hat{z}/\hat{z}_L$ as a function of θH can be derived from the elements B and C of ABCD matrix in (5b) and (5c), respectively. $\hat{z}_H/\hat{z}$ and $\hat{z}/\hat{z}_L$ against θH for various impedance ratio of R are plotted in Fig. 6(b) and 6(c) from (7a) and (7b), respectively.

$$\frac{\hat{z}_H}{\hat{z}}=\frac{\hat{z}_H j\cosh(\frac{\lambda}{4}\alpha)}{B} \quad (7a)$$

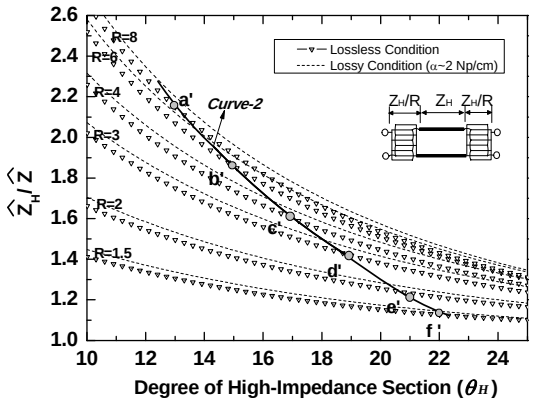
$$\frac{\hat{z}}{\hat{z}_L}=\frac{j\cosh(\frac{\lambda}{4}\alpha)}{\hat{z}_L C} \quad (7b)$$

Equations (7a) and (7b) include the information about the practical impedance selection criterion for $\hat{z}_H$ and $\hat{z}_L$. Because the goal is to shrink the passive circuit size by the step impedance technique, the minimum $\theta_H+\theta_L$ points of a~f in Fig. 6(a) are mapped to these of a'~f and a"~f' along Curve-2 and Curve-3 in Fig. 6(b) and Fig. 6(c), respectively. Thus, the practical required $\hat{z}_H/\hat{z}$ and $\hat{z}/\hat{z}_L$ can be determined. Because the points of a~f in Fig. 6(a) are all located at the minimum points ($\theta_H=\theta_L$), θ_H for the points of a'~f and a"~f" are equal to 13°, 15°, 17°, 19°, 21° and 22° while R= 8, 6, 4, 3, 2, 1.5.

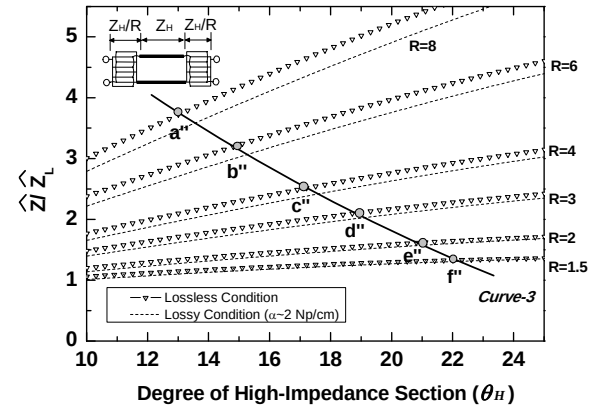
The maximum impedance ratio of R is limited by $\hat{z}$, $\hat{z}_{H(MAX)}$ and $\hat{z}_{L(MIN)}$. The bandwidth of the input return loss is determined by $\hat{z}$ of the imitated λ/4 transmission line while $\hat{z}_{H(MAX)}$ and $\hat{z}_{L(MIN)}$ depend on the process. It will be discussed later that a wider bandwidth is realized by choosing a lower impedance of $\hat{z}$ for each arm of the imitated phase-inverter rat-race coupler as shown in Fig. 7(a). There exists a minimum for $\hat{z}$ in consideration of the magnitude of the return loss at the center frequency of $f/f_C=1$. Thus, $\hat{z}$ is decided first in the design. The impedance ratio



(a)



(b)

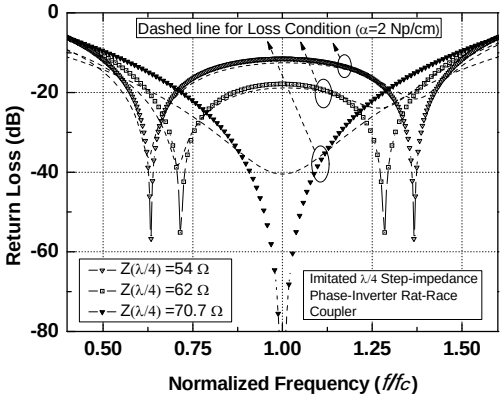


(c)

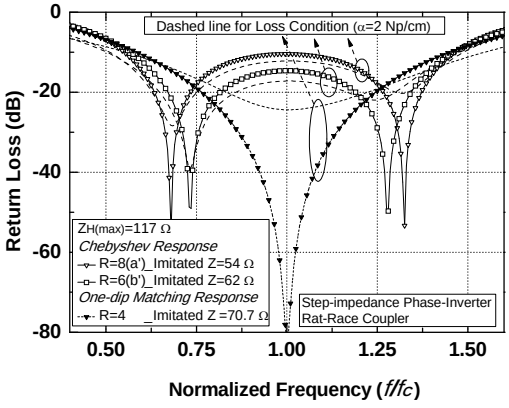
Fig. 6. Solution of the step-impedance technique for different impedance ratio under the lossless and lossy conditions, (a) $\theta_H+\theta_L$ versus the degree of θ_H, (b) $\hat{z}_H/\hat{z}$ versus the degree of θ_H , (c) $\hat{z}/\hat{z}_L$ versus the degree of θH.

of R in curve 2 (curve 3) of Fig. 6(b) (Fig. 6(c)) increases monotonically as $\hat{z}_H/\hat{z}$ ($\hat{z}/\hat{z}_L$) increases. Thus, $\hat{z}_{H(MAX)}/\hat{z}$ sets give an upper limit for the impedance ratio of R from Fig. 6(b) while $\hat{z}/\hat{z}_{L(MIN)}$ sets the other limit from Fig. 6(c). The lower one of the two limits is the maximum achievable impedance ratio of R. Thanks to the low impedance offered by the inter-digital structure, the maximum achievable impedance ratio in this paper is determined by the $\hat{z}_{H(MAX)}/\hat{z}$. A detailed design guideline with practical numbers will be illustrated later.

For the case of a Butterworth response, the normalized characteristic impedance ($\hat{z}$) of a $\lambda/4$ section is equal to $\sqrt{2}$. Here, the reference impedance at each terminal port is 50 Ω. If the realizable highest-impedance section is chosen to be 117 Ω ($\hat{z}_{H(MAX)}=2.3$), the highest $\hat{z}_{H(MAX)}/\hat{z}$ is limited to be 1.6 under $\hat{z}=\sqrt{2}$ (one-point matching response). Only impedance ratios ($\hat{z}_H/\hat{z}$) below 1.6 can be achieved, as marked by the points of c' ~f' in Fig. 6(b). The minimum of $\theta_H+\theta_L$ at the point of c´ is about 34° and each arm is reduced to 76 % of the original λ/4 length. A slight shrinkage of a rat-race coupler can be achieved by the Butterworth design.



(a)



(b)

Fig. 7. (a) The bandwidth of the return-loss for the imitated $\lambda/4$ phase-inverter rat-race couplers (for different $\hat{z}$). (b) The bandwidth of the return loss for the corresponding step-impedance phase-inverter rat-race couplers. Here, each imitated $\lambda/4$ phase-inverter rat-race coupler is replaced by a different step impedance ratio.

For more size reduction, a Chebyshev response is chosen to increase $\hat{z}_{H(MAX)}/\hat{z}$ above 1.6 by adjusting below $\sqrt{2}$ [A12][A13][A21]. By choosing a lower imitated impedance of $\hat{z}$, $\hat{z}_{H(MAX)}/\hat{z}$ is raised to a

higher value; thus, a higher impedance ratio of (R) becomes allowable. For instance, when $\hat{z}$ is reduced from $\sqrt{2}$ (70.7 Ω) to 1.08 (54 Ω), the highest $\hat{z}_{H(MAX)}/\hat{z}$ increases to 2.17 and R=8 (at the point of a´) can be realized. Thus, the minimum $\theta_H + \theta_L$ of 26° becomes possible. Thus, each arm is further reduced to 58 % of the original $\lambda/4$ length. According to Fig. 6(c), $\hat{z}/\hat{z}_L$ is equal to 3.68, which is smaller than the maximum realizable ratio of $\hat{z}/\hat{z}_{L(MIN)}$ (= 54 Ω/ 10 Ω). Because the low-impedance boundary is effectively extended by the inter-digital structure, the impedance constraint in silicon process is limited by $\hat{z}_{H(MAX)}$ instead of by $\hat{z}_{L(MIN)}$. The return loss of the step-impedance technique for the cases of a'~ c' are plotted in Fig. 7(b). It is clearly revealed that demarcation between Butterworth and Chebyshev matching response for the case ($\hat{z}_H = \hat{z}_{H(MAX)} = 2.3$) is located around $\hat{z}_H/\hat{z} = 1.6$. The input return loss at the points of a´~b´ is characterized as a Chebyshev response while the input return loss for c´~f´ corresponds to a one-dip matching at the center frequency. The curves for a lossy condition ($\alpha = 2\ Np/cm$) are also plotted in Fig. 7(a) and 7(b). As marked by the dashed lines, the bandwidth is slightly extended when the return loss dips are gradually smeared out as loss increases especially at the high frequency dip.

It is interesting to notice that a bandwidth extension technique with Chebyshev response also exists for the design of a step-impedance, phase-inverter, rat-race coupler as illustrated by Fig. 7(a) and Fig. 7(b). This property implies that a wide bandwidth, small size and thus less loss step-impedance phase-inverter rat-race coupler can be achieved at the same time in our work. Based on the discussion above, the design flow of a step-impedance phase-inverter rat-race coupler is summarized as follows,

1) Achieve the wanted bandwidth of the input return loss for an imitated, phase-inverter, rat-race coupler by choosing the characteristic impedance of each arm according to Fig. 7(a). For example, 100 % bandwidth ratio with an acceptable (for example, 12 dB) return loss is realized under $Z_{(\lambda/4)} = 54\ \Omega$.

2) The realizable $\hat{z}_{H(MAX)}$ and $\hat{z}_{L(MIN)}$, limited by the silicon process, need to be considered to determine the maximum impedance ratio of R for the step-impedance technique according to constraints in Fig. 6(b)-6(c). In general, $\hat{z}_{H(MAX)}$ sets the limit for the maximum impedance ratio of R because of the extension of the low impedance boundary by the inter-digital structure. Thus, only Fig. 6(b) is used to determine the maximum impedance ratio of R and $\hat{z}_H$ is set to be $\hat{z}_{H(MAX)}$.

3) The length (or degree) of high and low impedance lines can be obtained from curve 1 of Fig. 6(a) to achieve the minimum size.

4) From Section II-B, the design parameters, such as spacing and finger number, for a high-impedance CPS and an inter-digital CPS can be quickly determined.

5) By the electromagnetic simulation, the return-loss bandwidth, amplitude/phase balance, center frequency and size can be accurately verified after several iterations.

TABLE I

PERFORMANCE COMPARISONS OF THE SILICON-BASED PHASE-INVERTER RAT-RACE COUPLER

Ref.	Frequency (GHz)	Topology	Insertion Loss *2 (dB)	Isolation (dB)	Phase-Difference (Degree)	Amplitude-Imbalance (dB)	Size (μm²)
[14]	25~35	Multilayer (with ground plane)	4 (T) 5.1 ~ 7 (C)	< -17	150 ~ 200	~ 3	282 x 314
[15]	48~80	FGCPW *1 (with ground plane)	4 ~ 5 (T) 5.7 ~ 6.5 (C)	< -18.5	182 ~ 186	~ 1.6	334 x 334
	62~90		4.2 ~ 5 (T) 5.6 ~ 6.4 (C)	< -21	184 ~ 187	~ 1.4	320 x 320
[16]	5~23	Spiral-Shaped CPS *3 / Butterworth Response	8 ~ 9.5 (T) 9.1 ~ 11.0 (C)	< -25	172 ~ 178	~ 2	707 x707
This Work	5~15	Step Impedance *3 / Chebyshev Response	6.5 (T) 7.5 (C)	< -30	179 ~ 181	< 1	868 x 868

*1) FGCPW : Finite-ground coplanar waveguide. *2) T : Through / C : Coupled. *3) Implemented directly on the lossy silicon substrate.

10 GHz Step-Impedance Phase-Inverter Rat-Race Coupler

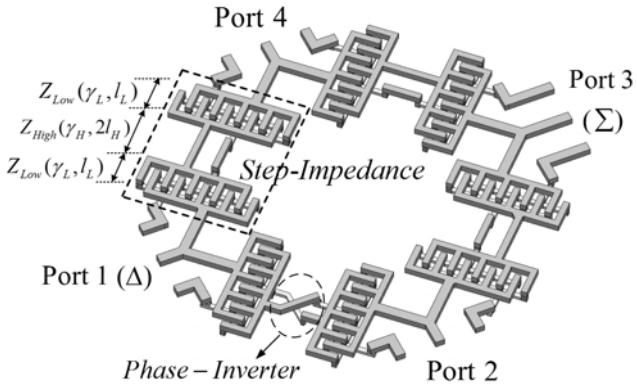
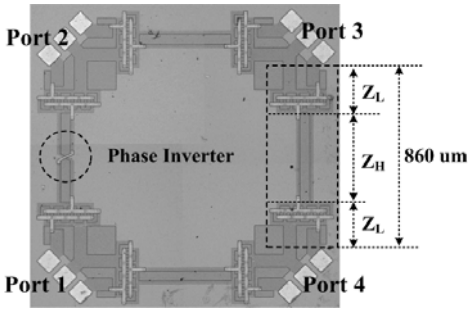
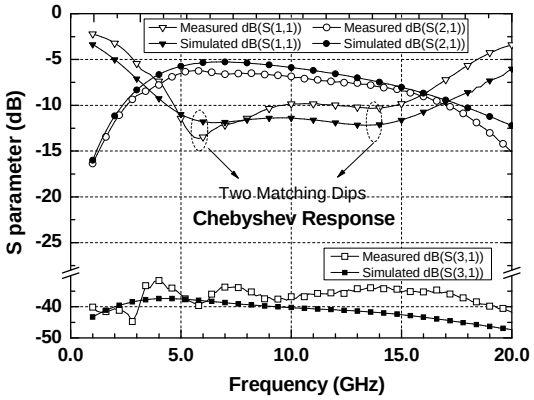


Fig. 8. 3D view of a step-impedance phase-inverter rat-race coupler.

A stand-alone 10 GHz phase-inverter rat-race coupler using the step-impedance technique is demonstrated using a standard 0.35 μm CMOS process with top metal thickness of 0.92 μm in this paper. The 3D layout is shown in Fig. 8. The CPS transmission lines are employed in the four arms of the coupler, while each port is formed by CPW (coplanar-waveguide) type for the GSG probing. The low-impedance section consists of five parallel CPS cells (N=5), as described in Fig. 4(b). The length of each arm in a conventional 10 GHz phase-inverter rat-race coupler directly on silicon substrate is practically up to 1340 μm. After using step-impedance technique, the length is reduced to only 860 μm and a 64% length reduction is achieved. The step-impedance section is equivalent to a quarter-wave length transmission line with a characteristic impedance of 60 Ω while Z_H and Z_L are 121 Ω and 19 Ω, respectively. The percentage of size reduction is consistent with the theoretical minimum of impedance ratio of R around 6. The die photo is shown in Fig. 9(a). The fabricated 10 GHz, rat-race coupler is characterized by a Chebyshev response and the input return bandwidth is from 5 GHz to 15 GHz, as shown in Fig. 9(b). The fractional bandwidth is near 100 % with insertion loss around 6~7 dB. When compared with the previous work [A16], the reduction of insertion loss means that the problem of loss is obviously mitigated. An isolation of better than 30 dB in |S31| is achieved between delta and sum ports as depicted in Fig. 9(b). The differential phase condition (180°) between port-2 and port-4 in Fig. 8 is always held for the whole operating frequency range. The maximum phase and magnitude errors over the operating frequencies of 5~15 GHz are smaller than 4 degrees and 1 dB, respectively. All of the measured results correlate closely with the simulation as shown in Fig. 9(b)-(c). The miniature rat-race coupler with a lower insertion loss reveals that the step-impedance technique can effectively reduce the length of each arm and thus the substrate loss effect. The performance of our work and other state-of-the art phase-inverter rat-race couplers implemented in silicon-based technologies are summarized in Table. I.



(a)



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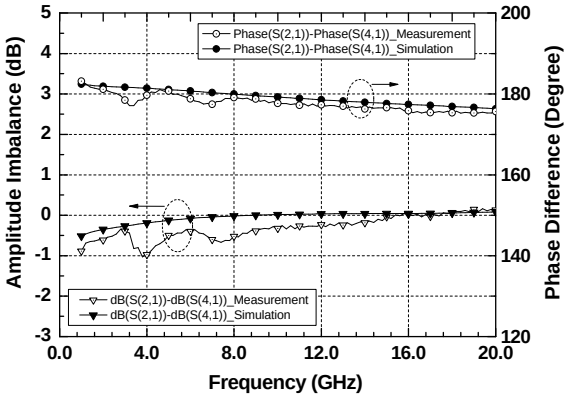


(c)

Fig. 9. (a) The chip micrograph, (b) S-parameter and (c) amplitude imbalance/phase difference of the 10 GHz step-impedance phase-inverter rat-race coupler.

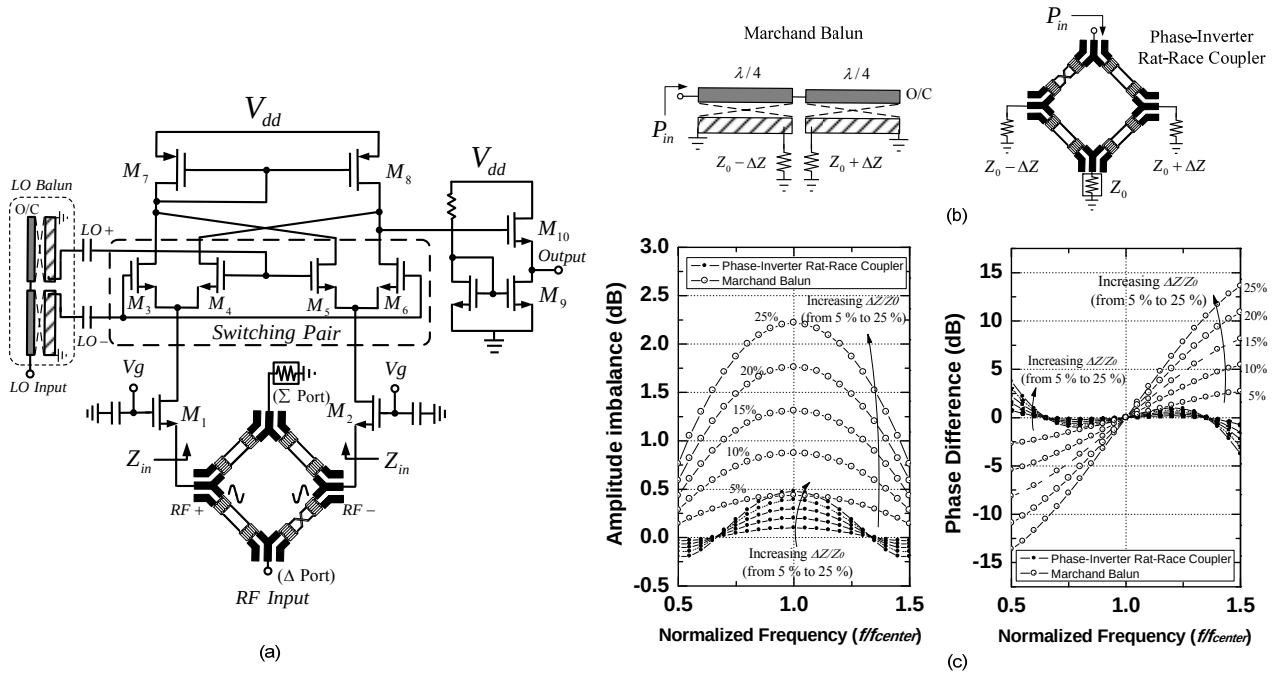


Fig. 10. (a) Simplified circuit diagram of the CMOS Gilbert down-converter using a step-impedance phase-inverter rat-race coupler at RF input stage, (b) the impedance mismatch condition occurred at the output ports of the Marchand Balun (left) and rat-race coupler (right), and (c) simulated amplitude and phase differences with respect to the normalized frequency for variant ratios of ΔZ/Z.

Broadband CMOS Gilbert Down-Converter

Figure 10(a) shows a practical application of the step-impedance phase-inverter rat-race coupler in the broadband Gilbert down-converter using 0.13 μm standard CMOS technology. A 15 GHz miniature rat-race coupler is employed in the RF stage to generate the wideband differential signal, and it is followed by the common-gate-configured transistors, M1~M2, which have superior frequency response and low input impedance to facilitate broad-band impedance matching. The device size of the transistors, M1 and M2, is ten-finger with a unit gate-width of 2.5 μm. The input impedance of the common-gate stage is equal to the reciprocal of the transconductance. By adjusting the DC biasing, a desired input impedance (Zin) can be obtained. The input impedance, Zin, is approximately 50 Ω under the gate voltage of 0.6 V. The Gilbert mixer core (M3~M6), driven by differential LO signal, commutates RF currents for frequency translation. The differential IF current output is combined by the active PMOS current mirror (M7 and M8) to generate a single-ended output. A common collector stage consisting of transistors M9–M10 is employed as the IF output buffer to drive the 50 Ω impedance of the measurement equipment.

When compared with a traditional rat-race coupler [A7], the proposed rat-race coupler can provide dc return paths from port-2/port-4 (RF+/RF-) to ground by the phase-inverter structure. Thus, a wideband differential signal is generated for the double-balanced Gilbert mixer core without voltage headroom and dc power consumption. On the other hand, a rat-race coupler has a better ability to alleviate the unbalanced effect caused by the output impedance mismatch when compared with a Marchand balun. As depicted in Fig. 10(b), ΔZ represents the amount of the impedance mismatch at the output ports of the Marchand balun and

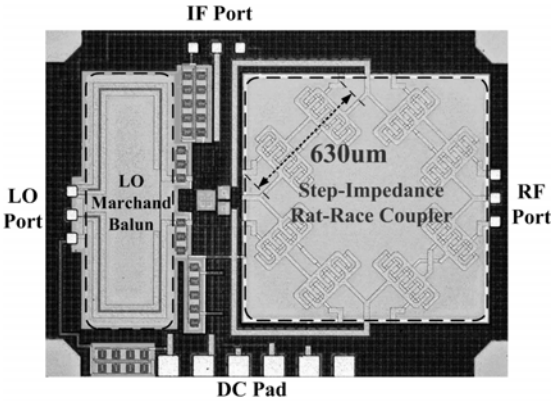


Fig. 11. Chip micrograph of the CMOS Gilbert down converter using a 15 GHz step-impedance phase-inverter rat-race coupler as the RF-port single-to-differential balun. The chip size is 1.4 × 1.8 mm2.

phase-inverter rat-race coupler. For a fair comparison, both components are designed with the same input matching condition and fractional bandwidth ratio of 100% (based on S11<10 dB). As shown in Fig. 10(c), the simulated amplitude and phase differences for various ratios of ΔZ/Z are plotted with respect to the normalized frequency. All the deviations are basically proportional to the mismatch. When the mismatch effect (ΔZ/Z) increases up to 25 %, the amplitude deviation of a Marchand balun is larger than 2 dB; that of a phase-inverter rat-race coupler, however, is only less than 0.5 dB. When it comes to phase condition, a rat-race coupler keeps error within 4°, which is also smaller than that of a Marchand balun. Especially apart from the center frequency, the phase deviation of a Marchand balun increases quickly and exceeds 12.5° at the f / f_{center} of 0.5 and 1.5. It is obvious that a phase-inverter rat-race coupler inherently has smaller amplitude/phase deviations over a wide-band operation than a Marchand balun has when mismatch occurs. In general, the Gilbert active mixer has a flat region for conversion gain versus LO power, where the switching core fully commutes RF input current and has higher tolerance on the mismatch effect caused by an imbalanced LO signal. Thus, a phase-inverter rat-race coupler is used at the RF port to mitigate the critical mismatch problem while a Marchand balun is utilized at the LO port because of the size concern.

In the step-impedance section, the high impedance (Z_{High}) and low impedance (Z_{Low}) are near 113 Ω and 18 Ω, respectively. Thus, the impedance ratio of R is about 6.6 and the impedance of the imitated λ/4 section is equal to 55 Ω. The length of each arm of the 15 GHz rat-race coupler is shrunk to 630 μm. From the simulated results, the insertion loss is 4~5 dB with the amplitude and phase errors of 1 dB and 2°, respectively. When compared with the stand-alone 10 GHz phase-inverter rat-race coupler in Fig. 8, the loss is further reduced due to a smaller size at higher frequency. As shown in Fig. 11, the March Balun is at the left side of the photograph and the miniature rat-race coupler is on the right side. The total size is 1.4 × 1.8 mm2.

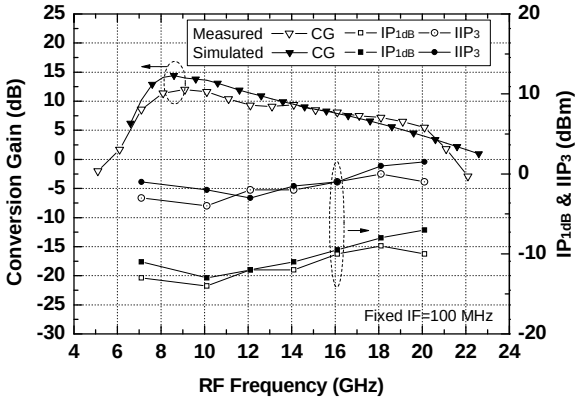


Fig. 12. Measured and simulated conversion gain, IP1dB and IIP3 versus RF Frequency.

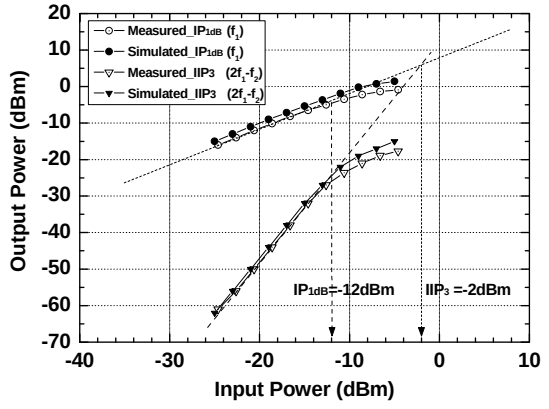


Fig. 13. Measured and simulated power performance of the CMOS Gilbert down converter with a step-impedance phase-inverter rat-race coupler.

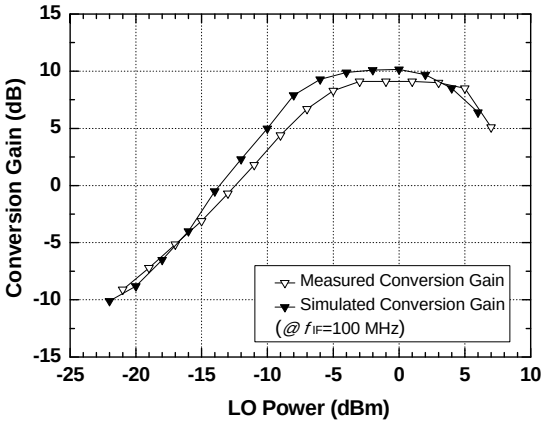


Fig. 14. Measured and simulated conversion gain versus LO Power.

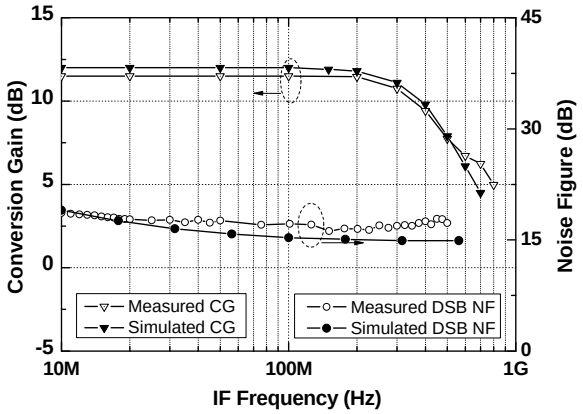


Fig. 15. Measured and simulated conversion gain and noise figure versus IF Frequency.

In the step-impedance section, the high impedance (Z_{High}) and low impedance (Z_{Low}) are near 113 Ω and 18 Ω, respectively. Thus, the impedance ratio of R is about 6.6 and the impedance of the imitated λ/4 section is equal to 55 Ω. The length of each arm of the 15 GHz rat-race coupler is shrunk to 630 μm. From the simulated results, the insertion loss is 4~5 dB with the amplitude and phase errors of 1 dB and 2°, respectively. When compared with the stand-alone 10 GHz phase-inverter rat-race coupler in Fig. 8, the loss is further reduced due to a smaller size at higher frequency. As shown in Fig. 11, the March Balun is at the left side of the photograph and the miniature rat-race coupler is on the right side. The total size is 1.4 × 1.8 mm2.

Figure 12 shows the conversion gain, input 1-dB gain compression point (IP1dB) and input third-order inter-modulation point (IIP3) versus RF frequency under f_{IF}=100 MHz. The conversion gain is above 8 dB from 7 GHz to 18 GHz while the IP1dB and IIP3 within operating bandwidth are better than -12.5 dBm and -2 dBm, respectively. The power performance at the operating frequency of 12 GHz is shown in Figure 13. Because all of the transistors in the Gilbert-cell mixer are implemented in the deep N-well, the signal leakage through substrate is less likely. Most of leakage is caused by the circuit topology; thus, a high symmetry is important for the leakage cancellation between LO and RF ports. LO-to-RF isolation is better than 35 dB and RF-to-IF isolation is around 20 dB over the operating frequency range.

Figure 14 shows the measured conversion gain versus LO power with a RF input power of -30 dBm under f_{RF} of 12 GHz and f_{IF} of 100 MHz. When LO power exceeds -5 dBm, the curve is gradually saturated and enters the flat region of conversion gain versus LO power, where conversion gain and noise figure are insensitive to LO power. In the flat conversion gain region, the Gilbert mixing core has a higher tolerance for the LO signal mismatch. Figure 15 shows the measured conversion gain and double sideband (DSB) noise figure versus IF frequency of 10 MHz ~ 1 GHz under f_{RF}=9.1 GHz. The noise figure of 16 dB indicates that the step-impedance rat-race coupler in the first stage successfully converts the received power to the common-gate input, and suffers less from substrate loss. A better noise figure is expected by further increasing the impedance ratio of R because of the higher size reduction. The mixer core consumes 2.9 mA at the supply voltage of 1.8 V. The simulated results are all shown in Fig. 12~15 for comparisons.

2nd year

A 60 GHz millimeter-wave system with unlicensed 7-GHz bandwidth conspicuously stands out in short-range high-data-rate applications, such as wireless personal area network (WPAN) and high-definition multimedia interface (HDMI). In 2004, the first CMOS 60-GHz amplifier was successfully demonstrated in standard 0.13- m CMOS technology, beginning 60-GHz transmission using the CMOS-based IC [B1]. Subsequently, different architectures for receivers, transmitters and transceivers [B2]-[B13] were proposed and came into fruition by using standard advanced 130-nm CMOS, 90-nm CMOS and SiGe HBT processes. The reported noise figure (NF) of a 130-nm CMOS receiver [B3] is up to 12.5 dB while 90-nm CMOS receivers [B5]-[B13] achieve a better NF of 5.5~8 dB. Recently, 65-nm [B14][B15] or 45-nm [B16] CMOS technologies have also been devoted in the 60-GHz transmission. To date, the noise figures of the 65-nm and 45-nm CMOS receivers are 5.5~7 dB and 6~8 dB, respectively. Even with more advanced CMOS technologies, NF improvement is limited. Additionally, a power amplifier (PA) is also a key component at such high 60-GHz path loss because the output power of PAs determines the maximum transmission distance. The low breakdown voltage in the advanced CMOS process makes high-power designs difficult. Compared with III-V compound technologies, standard CMOS PAs have lower power added efficiency (PAE) [B4],[B5],B[10],[B12],[B13], thus requiring larger DC power consumption for the same output power. The DC power consumption becomes more severe at 60-GHz system because many PAs are required for multiple paths in the transmitter, especially for beam-forming

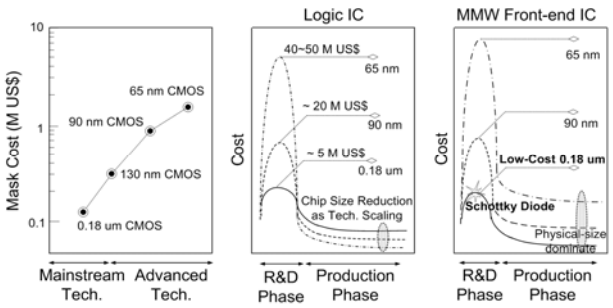


Fig. 1. (a) Mask costs and the costs for (b) logic ICs and (c) millimeter-wave front-end ICs as a function of R&D and manufacturing phases for different CMOS generations.

phased-array architectures.

In addition to an improvement in the speed of the circuit by advanced technologies, the scaling rule has caused both chip size shrinkage and steady reductions in IC manufacturing costs. In the past, research and development (R&D) costs were never a concern and could easily be accounted for in the manufacturing stage. However, R&D costs recently have become an issue as the transistor size of the CMOS process approaches the photolithography limit [B17]. Figure 1(a) shows the photo mask cost for different CMOS generations. The mask cost increases dramatically as technology scales down because of expensive photolithography techniques. For the 90-nm CMOS generation, the mask already costs more than one-million US dollars; thus, the R&D costs for a 60-GHz system using advanced CMOS technology is an issue for product development. In millimeter-wave IC design, many iterations are unavoidable due to inaccurate device modeling and high process variation, greatly aggravating R&D costs. Moreover, the passive components, used in millimeter-wave transceiver, occupy a large percentage of the chip. These components cannot be scaled down using advanced CMOS technology B[6]. The costs of the logic ICs and millimeter-wave front-end ICs as a function of the R&D and manufacturing phases are described in Figs. 1(b) and 1(c), respectively [B17]. Here, the high R&D expense forms a barrier to product development. In Fig. 1(b), the high R&D costs of an advanced CMOS technology may still be covered for the logic IC product because of lower manufacturing cost by the device scaling rule. However, that is not the case for the millimeter-wave IC product because the scaling rule does not considerably decrease the manufacturing cost, as shown in Fig. 1(c). The Schottky diode, like a catalyst, significantly reduces the R&D cost barriers shown in Fig. 1(c) and makes a 60-GHz transceiver with low-cost CMOS technology possible. However, no millimeter-wave transceiver based on the Schottky diodes has been reported to date.

In the millimeter-wave regime, HEMT-based LNAs [B18] and PAs [B19][B20] have superior noise figure at low DC power and larger output power with higher power added efficiency, respectively. The unmatched performances offered by HEMT-based LNA and PA at 60 GHz are still very attractive for millimeter-wave applications. While most other research follows the CMOS scaling rule and employs advanced CMOS technology for the 60-GHz application, an alternative approach is proposed in this work due to the occurrence of Schottky diodes in the foundry CMOS process. Here, LNA and PA are realized using GaAs-based technology while the other circuits of a 60-GHz millimeter-wave front-end are fully implemented in a low-cost 0.18- m CMOS single chip. In this work, the first 60-GHz Schottky-diode-based receiver, excluding the GaAs-based LNA, is demonstrated in a 0.18- m foundry CMOS process.

The Methods and Experimental Results

(A) Theory of a distortionless transmission line

When a lossy transmission line is designed as a distortionless transmission line based on the ratio of R/L=G/C, the propagation constant and the characteristic impedance according to reference [B21] are expressed as follows,

$$\gamma = \alpha + j\beta = \frac{R}{\sqrt{\frac{L}{C}}} + j\frac{\omega}{v_P} \quad \text{(B.1)}$$

$$Z = \sqrt{\frac{L}{C}} \quad \text{(B.2)}$$

$$v_P = \frac{1}{\sqrt{LC}} \quad \text{(B.3)}$$

It is obvious that the attenuation constant is a

constant, the phase constant is a linear function of frequency and the characteristic impedance is independent of frequency. Thus, for the case of a distortionless transmission line, the size shrinkage concept by the effective dielectric constant is preserved by observing (B.2) and (B.3) while the attenuation constant coexists. In other words, the design methodology of the size shrinkage for the lossless condition is still applicable as if the loss does not exist. There is no constraint on the loss for the distortionless transmission line and one distinct concept for the distortionless transmission line is the coexistence of size shrinkage and loss. A quality factor for the distortionless transmission line can be defined as follows [22] to discuss the loss effect.

$$Q = \frac{1}{\frac{R}{\omega L} + \frac{G}{\omega C}} = \frac{\beta}{2\alpha} \qquad \text{(B.4)}$$

It turns out that the quality factor is only 2.1 for the distortionless transmission line example in reference [B21] when the center frequency is 15 GHz.

Here, a simple parallel plate transmission line is employed as a heuristic example to establish the distortionless condition (R/L=G/C). As shown in Fig. 2, parallel plates with metal width W and thickness t are separated by a distance of d. Finite metal thickness t accounts for the metal loss and silicon with finite dielectric loss is inserted between two parallel plates.

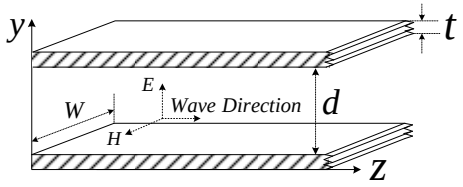


Fig. 2. Parallel plate distortionless transmission line.

Here, R, L, G and C in the parallel plate transmission line can be expressed as follows,

$$R = \frac{2}{\sigma_C}\frac{1}{t \times W}, \quad L = \mu\frac{d}{W}, \quad G = \frac{1}{\rho}\frac{W}{d}, \quad C = \varepsilon\frac{W}{d} \qquad \text{(B.5)}$$

$$\frac{G}{C} = \frac{1}{\rho\varepsilon}, \qquad \frac{R}{L} = \frac{2}{\mu\sigma_C}\frac{1}{t \times d} \qquad \text{(B.6)}$$

$$Z = \sqrt{\frac{L}{C}} = \sqrt{\frac{\mu}{\varepsilon}}\frac{d}{W} \qquad \text{(B.7)}$$

Here, ε, μ, σ_c and are the dielectric constant, permeability and resistivity of silicon and the conductivity of the metal plate, respectively. The factor of two in (B.6) accounts for the metal loss from both top and bottom plates. The distortionless condition (R/L=G/C) can be fulfilled by the following equation.

$$\frac{1}{\rho\varepsilon} = \frac{2}{\mu\sigma_C}\frac{1}{t \times d} \qquad \text{(B.8)}$$

By plugging in the silicon relative dielectric constant of 11.8 and metal conductivity of 2.0x107 S/m into (B.8), a heuristic design formula is established as follows,

$$t \times d = 0.81 \quad \mu\text{m}^2 \qquad \text{(B.9)}$$

The derivation above assumes that the current conducts uniformly in the finite thickness t. This assumption holds true if the metal thickness t is less than the skin depth. Otherwise, the metal thickness is replaced by the skin depth for a very thick metal and the skin effect complicates the distortionless condition because the metal resistance R is a function of frequency. Then, a distortionless condition can only be designed at the center frequency and the dispersive transmission line puts an additional constraint on the bandwidth of a rat race coupler. The metal thickness in IC fabrication is about the same order of magnitude of the skin depth. The skin depth at 10 GHz is 0.65 m. Thus, a metal thickness of 0.5 m has a uniform current approximately and d is 1.62 m from (B.9). The resulting separation distance d is a reasonable number for passive coupler design in the IC fabrication process. In summary, the distortionless condition is established by introducing a finite thickness t for the metal. The design methodology for the characteristic impedance is only affected by the width W and distance d parameters as the case of a lossless transmission line. Thus, a distortionless condition and matching condition for a phase-inverter rat-race coupler can be achieved simultaneously. In our work, a coplanar stripline is employed and more involved analysis is needed for the distortionless condition. This is beyond the scope of our work.

(B) A Gilbert Down-converter with lumped-distributed phase-inverter rat-race coupler based on Chebyshev band-broadening technique

In the past decades, many quarter-wavelength-based passive components, such as phase-inverter rat-race couplers, can be fully-integrated into the silicon-based ICs at microwave and millimeter

frequency regimes. Recently, directly implementing quarter-wavelength-based passive components on silicon substrate is the most effective way for size reduction because of the higher dielectric constant despite of higher loss. To shrink the size and minimize the loss, miniaturization methods such as spiral-winding structure [B21], step-impedance structure [B23] were proposed for the phase-inverter rat-race coupler. The spiral-shaped phase-inverter rat-race coupler (2.5 GHz to 13 GHz) with a Butterworth response has an area of 1.4x1.4 mm2 and is demonstrated with a mixer for UWB applications [B21]. The step-impedance technique also effectively reduces the size because of the large high impedance ratio between the high-impedance and low-impedance inter-digital sections. On the other hand, the bandwidth reduction caused by the step-impedance structure can be alleviated by designing the equivalent characteristic impedance of each arm of a phase-inverter rat-race coupler for a Chebyshev response [B23]. Thus, a step-impedance rat-race coupler (7 GHz to 18 GHz) with a Chebyshev response has an area of 0.63x0.63 mm2 has been realized with a mixer [B23]. The inter-digital low-impedance section of a step-impedance section behaves as a capacitor and is hard to meander due to its wide shape. Thus, for lower operating frequencies, incorporating spiral-winding [B21] and lump-distributed [B24] techniques with a Chebyshev response is the effective way for size reduction and bandwidth extension. In this letter, a spiral-shaped lumped-distributed phase-inverter rat-race coupler (2.5 GHz to 12.5 GHz) with a Chebyshev response has been implemented with a mixer for UWB applications. The resulting coupler only occupies an area of 0.65x0.65 mm2. As a result, the demonstrated rat-race coupler has about 80% area reduction when compared with our previous spiral-shaped Butterworth-response design [B21] and maintains a broad bandwidth for UWB Gilbert Mixer applications.

Figure 3 shows the lumped-distributed phase-inverter rat-race coupler by shunting capacitors at the two terminations of each arm with the Gilbert micromixer. Each arm of the lumped-distributed coupler is equivalent to an imitated quarter-wavelength TL, as shown in Fig. 4. When loss is negligible, the equation to establish the equivalence at the center frequency between the imitated quarter-wavelength TL and the lumped-distributed TL is expressed in (1).

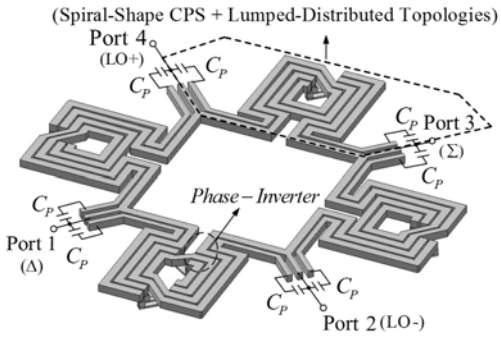


Fig. 3. Schematic of the lumped-distributed spiral-shape CPS phase-inverter rat-race coupler.

$$\begin{bmatrix} 0 & jZ_{imitated} \\ jY_{imitated} & 0 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ j\omega C & 1 \end{bmatrix} \begin{bmatrix} \cos\theta & jZ\sin\theta \\ jY\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} 1 & 0 \\ j\omega C & 1 \end{bmatrix}$$

$$\rightarrow \begin{cases} \dfrac{Z_{imitated}}{Z} = \sin\theta & 1\,(a) \\ \omega CZ = \cot\theta & 1\,(b) \end{cases}$$

The impedance ratio of Zimitated/Z is reduced as the length of θ is shrunk. Due to the physical layout, the characteristic impedance (Z) of spiral-shape CPS is limited at 80 Ω. Here, Zimitated is chosen as 50 Ω (below 70.7 Ω) for Chebyshev response and the input return loss has two splitting matching dips [B25,B26]. When the spacing of the two dips increases by reducing Zimitated, the bandwidth can be extended. In this work, the length (θ) is shrunk below 40°, representing that small θ accompanies Chebyshev response instead of Butterworth response. Thus, the targets for small size and broad bandwidth are achieved in the lumped-distributed design. From 1(b), the shunt capacitance can be obtained. The proposed rat-race coupler directly on the silicon substrate uses the top thick metal with 3-μm thickness to reduce metal loss, and the spacing and width of the CPS are 4 μm and 15 μm in the spiral shape, respectively. Since the RF trans-conductance stage of the 0.35-μm SiGe BiCMOS Gilbert micromixer has excellent frequency response, the operating bandwidth of the Gilbert micromixer is

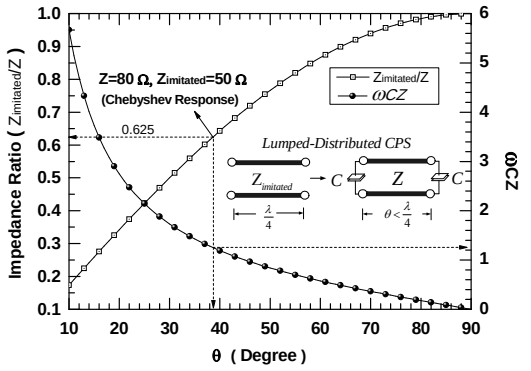


Fig. 4. The impedance ratio of Zimitated/Z and required shunt capacitance versus the length (θ) for the lumped-distributed technique.

finally determined by the lumped-distributed phase-inverter rat-race coupler (used in LO port).

The proposed rat-race coupler is employed at the LO port of the UWB Gilbert micro-mixer and the area excluding pads is 0.9x0.8 mm2 as shown in Fig. 5. The current consumption of the mixer core is 4.1 mA at 5-V supply voltage. Figure 6 shows the measured conversion gain (CG), P1dB, IIP3 and noise figure with respect to the RF frequency. The CG keeps 11~ 12 dB within 1-dB variation and the noise figure is 15~17 dB from 3 to 11 GHz. IP1dB and IIP3 keep around -12~-10 dBm and -1 dBm for each UWB band group, and the measured IF 3-dB bandwidth is up to 1.0 GHz. The measured LO-to-RF/ LO-to-IF/RF-to-IF isolation is better than 40 dB/35 dB/20 dB.

(C) The demonstrated 60-GHz dual-conversion down-converter in 0.18 μm foundry CMOS technology

The 60 GHz dual-conversion down-converter demonstrated in this research is composed of an SHM driven by the LO1 signal (first LO), the first intermediate-frequency (IF1) amplifier, a resistive mixer driven by the LO2 signal (second LO), a wideband amplifier (IF2), and a quadrature generator (LO2) as shown in Fig. 7 (a). The frequency planning of the dual-conversion is illustrated in Fig. 7(b). It is easy to fix the LO2 frequency at the most accurate point of the IQ generator to obtain a precise baseband IQ output while the designated RF channel is selected by tuning the LO1 frequency. Here, the 2fLO1 signal is tuned between 47~56 GHz and the LO2 signal is fixed

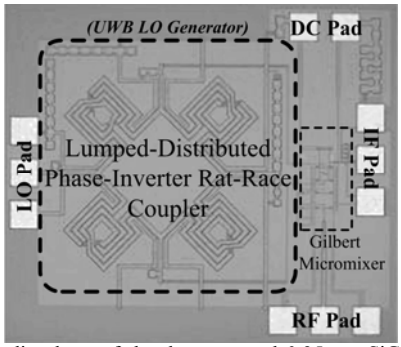


Fig. 5. The die photo of the demonstrated 0.35-μm SiGe BiCMOS UWB Gilbert downconverter using the proposed lumped-distributed phase-inverter rat-race coupler.

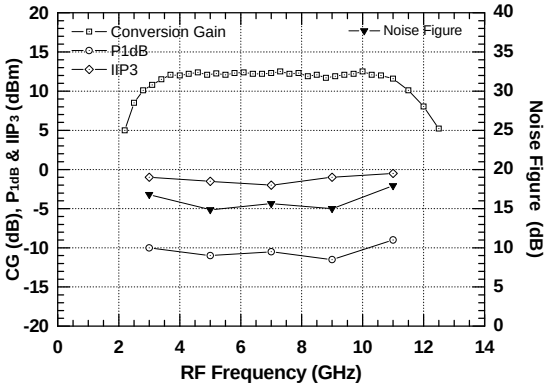


Fig. 6. The measured conversion gain, P1dB, IIP3, noise figure of the demonstrated 0.35-μm SiGe BiCMOS UWB Gilbert down-converter.

at 10 GHz. In the high-frequency conversion, the silicon Schottky-diode SHM with low turn-on voltage facilitates the LO1 buffer amplifier design.

The first stage in the dual conversion is a 60-GHz SHM, which includes a dual-band phase-inverter rat-race coupler and two Schottky-diode mixer cells in APDP configuration, as shown in Fig. 8. The coupler merges an RF divider and an LO1 balun into one passive component to reduce the area necessary for SHM. An in-phase/out-of-phase signal is generated from the RF/LO port while the two APDPs are series-connected between the remaining two ports as shown in Fig. 7(a). The in-phase/out-of-phase signal is always maintained for all frequencies because the physical paths from the RF/LO ports to the other two outputs are equal in geometry for the phase-inverter rat-race coupler. The output IF signal is taken from the virtual ground of the LO1 signals, formed at the middle point of two series connected APDPs, to achieve a good broadband LO-to-IF isolation. There are good broadband isolations between the RF and LO ports due to the intrinsic isolation property of the wideband four-port coupler. The APDP structure inherently

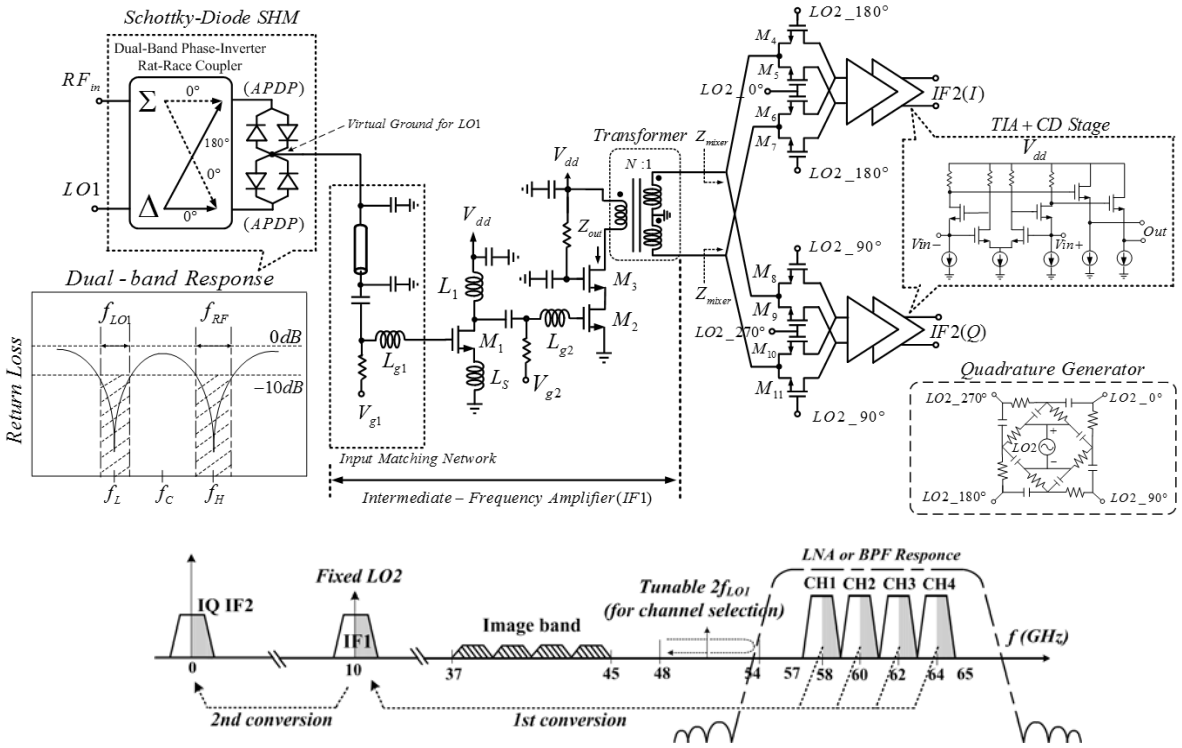


Fig. 7. (a) Schematic and (b) frequency planning of the 60-GHz dual-conversion down-converter by using Schottky diodes in 0.18-μm CMOS technology.

possesses an even-harmonic rejection, enabling it to achieve good broadband 2LO1-to-RF and 2LO1-to-IF isolations. Here, the rat-race coupler must handle RF and LO signals at two widely separate frequencies for the SHM. The RF signal ranges from 57-66 GHz, while the LO1 signal covers 23.5-28 GHz. The bandwidth of a phase-inverter rat-race coupler is determined by the input matching instead of the magnitude/phase imbalance. Thus, we design the return-loss as a dual-band, and two matching dips can be arranged by adjusting the transmission-line impedance of each arm of the phase-inverter rat-race coupler. Based on the equation (1) of [B25],

$$\hat{z} = \sqrt{2(1-\cot^2\theta)} = \sqrt{2(1-\cot^2\beta\ell)} = \sqrt{2\left(1-\cot^2(\frac{\pi}{2}\frac{f_0}{f_c})\right)} \qquad (1)$$

$\hat{z}$ is the normalized characteristic impedance of a coplanar strip-line transmission line of the phase-inverter rat-race coupler and $\theta = \beta\ell$. $f0$ and f_C represent the frequencies of the matching dips and the center frequency of the phase-inverter rat-race coupler, respectively. There are two matching dips when the characteristic impedance of each arm is below 70.7Ω, and the spacing of the two split matching dips is extended for a lower characteristic impedance. The ratios of the two matching points to the center frequency of f_H / f_C and f_L / f_C are designed to be 1.4 and 0.6. f_H=61.5 GHz and f_L=25.75 GHz are the center frequencies for the RF and LO1 bands, respectively. The corresponding characteristic impedance of the coplanar strip-line transmission line is designed as 55 Ω by setting the spacing and width of metal-6 to 1.5 μm and 16 μm, respectively. Using a small spacing, higher coupling between adjacent metals can be achieved. This effectively reduces the amount of electric field penetrating into silicon substrate, thus alleviating the loss caused by a lossy silicon substrate.

The phase-inverter rat-race coupler shown in Fig. 8 is directly implemented on the silicon substrate. Compared with the transmission line formed by interconnect metals and interlayer dielectrics, a coplanar strip-line directly on the silicon substrate has a shorter effective wavelength due to its higher silicon dielectric constant ($\varepsilon_r = 11.8$), while the inter-metal dielectric has a smaller dielectric constant of 3.8~4. A lump-distributed technique, shunting capacitors at each port, is also used for size reduction. The length of each arm in the phase-inverter rat-race coupler at fcenter= 40 GHz is shrunk from 900 μm to 510 μm. Because the

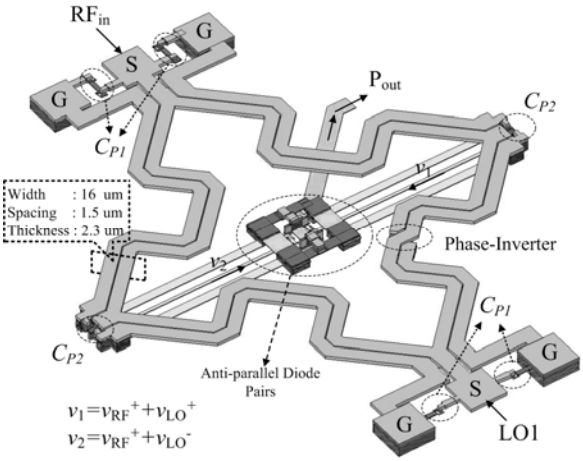


Fig. 8. The 3D view of the 60 GHz sub-harmonically pumped mixer using a dual-band lumped-distributed phase-inverter rat-race coupler in 0.18-μm CMOS technology.

junction capacitance from the APDP, contributing to the size reduction, is not negligible, the shunting capacitance (CP1) at both RF and LO ports needs to be larger than that (CP2) of the other two ports. Finally, the phase-inverter rat-race coupler can be further compacted to a square with sides of 400 μm in length by winding the arms, and the practical size of a stand-alone SHM is only 0.16 mm2 as shown in Fig. 9.

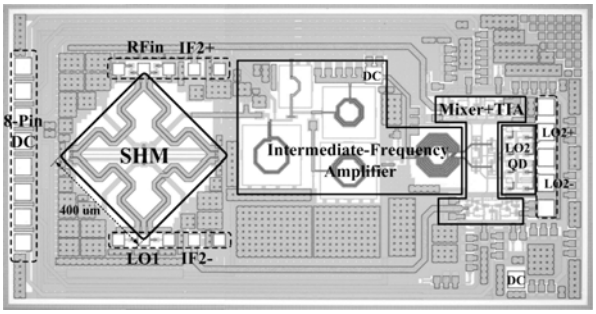


Fig. 9. Die photograph of the 60 GHz dual-conversion down-converter using 0.18-μm CMOS technology.

After the first conversion, the noise figure caused by the second conversion must be low enough to achieve an acceptable noise figure for the 60 GHz dual-conversion down-converter. Our goal is to have the overall noise figure of dual conversion below 20 dB based on the gain and noise figure of GaAs-based LNAs at 60 GHz. The first stage Schottky-diode SHM has a conversion loss of 15 dB. It means that the noise figure of the subsequent stage, including the intermediate-frequency (IF1) amplifier, the second stage resistive mixer and the wideband output buffer, must be lower than 5 dB at fIF1=10 GHz. A topology with low noise figure and high gain, as shown in Fig. 7(a), is chosen for the IF1 amplifier. The IF1 amplifier consists of a common source stage with the source degeneration inductor of LS for simultaneous noise and gain match and a subsequent cascode stage for gain boosting. Here, the gain of the IF1amplifier is designed to be around18~20 dB to suppress the noise caused by the resistive mixer. The bandpass response of the input matching network of the IF1 amplifier suppresses the fLO1 leakage signal. A 25-dB reduction in the LO1 leakage signal is obtained in simulation. At the output load of the IF1 amplifier, a single-to-differential transformer is employed for ac coupling, dc blocking, balanced-signal generation, and impedance transformation. The primary-coil inductance combined with the parasitic capacitance of the cascode device, M3, forms an LC tank at fIF1, and the secondary-coil inductance resonates out the parasitic capacitance at the source of the resistive mixer. The transformer is designed with a turn ratio of two (N=2) to transfer the high output impedance (Zout) of the cascode stage to the low input impedance (Zmixer) of the double-balanced resistive mixer. The transformer has a coupling factor of 0.7 while the primary and secondary inductances are 1.62 nH and 0.62 nH, respectively. The peak of quality factor is designed as closely as possible to fIF1. The maximum quality factor of the primary coil is 7.8 at fQmax of 8.5 GHz while the quality factor at 10 GHz is 7.5. The maximum quality factor of the secondary coil is 6.9 at fQmax of 10.3 GHz. For generating IQ baseband signals at low-frequency conversion stage, a two-stage polyphase shifter is employed at the LO2 ports of the 10-GHz double-balanced resistive mixers.

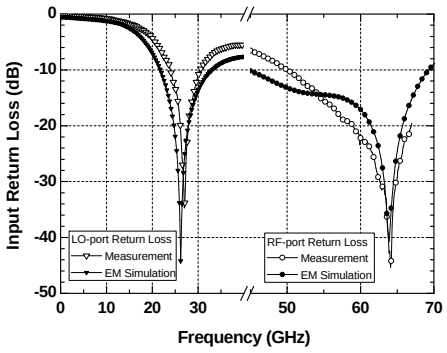


Fig. 10. Measured and simulated RF/LO return loss of the miniature dual-band rat-race coupler of the 60-GHz dual-conversion down converter using 0.18-μm CMOS technology.

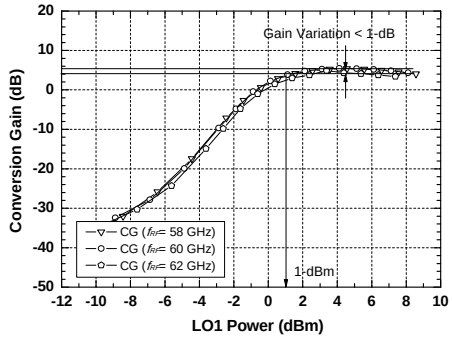


Fig. 11. Measured conversion gain of the 60-GHz dual-conversion down-converter versus LO1 power for different RF frequencies.

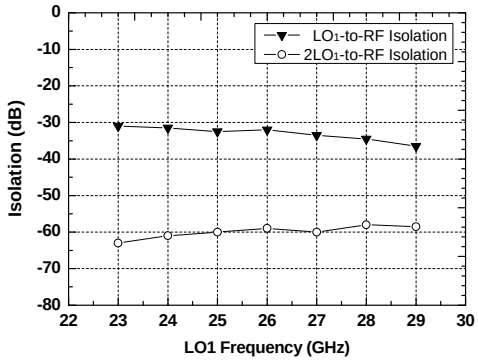


Fig. 12. Measured 2LO1-to-RF and LO1-to-RF isolations of the 60-GHz dual-conversion down-converter using 0.18-µm CMOS technology.

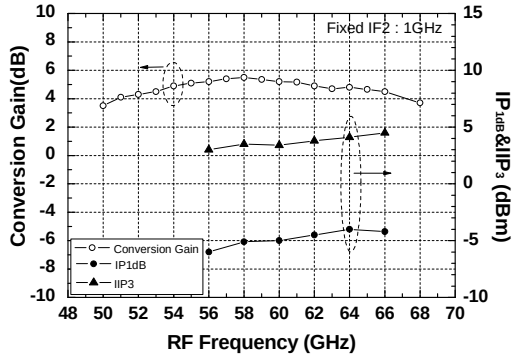


Fig. 13. Measured conversion gain and power performance of the 60-GHz dual-conversion down-converter using 0.18-µm CMOS technology.

Figure 9 shows the die photograph of the demonstrated 60-GHz dual-conversion down-converter using 0.18-µm CMOS technology. The chip size is 1.9x1 mm2 while the circuit area excluding the pads is 1.5x0.73 mm2. An 8-pin DC pad is on the left side of the chip and the GSGSG pad for differential LO2 signal is on the right side of the chip. Two differential pads on the top and bottom sides are used for RF/LO1 and IF2+/IF2-, respectively. The total current consumption is 22 mA under 2.5-V supply voltage. Figure 10 shows the simulated and measured input return loss of the RF and LO1 ports. The RF bandwidth, defined by the 10-dB return loss, is from 50 GHz to 70 GHz and fully covers our interest band of 57~66 GHz. The other matching bandwidth at lower frequency is located at the desired LO1 band of 23~30 GHz. The measured conversion gain versus LO1 power begins to flatten once the LO power exceeds 1 dBm as shown in Fig. 11. The required LO1 pumping power is small for the SHM due to the good-matching design at fLO1 and the low turn-on voltage of the Schottky diodes. According to the literatures [B27][B28], a 20~30 GHz CMOS driving amplifier with 0-dBm output power is easily implemented using 0.18-µm CMOS technology because the maximum available gain at 25 GHz of common-source / cascode configuration is higher than 8 dB / 15 dB. The measured 2LO-to-RF and LO-to-RF isolations as shown in Fig. 12 are in the range of -60 dB and -30 dB, respectively. For comparison, a stand-alone SHM, which is identical to the high-frequency SHM of the dual-conversion converter, is fabricated. The measured conversion loss of the stand-alone SHM from RF 57 GHz to 66 GHz is around 15 dB. The results of the stand-alone SHM together with other state-of-the-art millimeter-wave sub-harmonically pumped diode mixers are summarized in Table I. Our silicon Schottky-diode SHM requires the lowest LO power when compared with GaAs Schottky-diode SHMs.

The measured conversion gain and power performance of the 60-GHz dual-conversion down-converter are depicted in Fig. 13. At $f_{IF}2$=1 GHz, the conversion gain remains around 5 dB from 57 GHz to 66 GHz. The corresponding IP1dB and IIP3 are -6~-4 dBm and 3~5 dBm, respectively. The measured 3-dB IF2 bandwidth, shown in Fig. 14, is up to 2.1 GHz and the gain variation is less than 1 dB for IF2 frequency of up to 1.8 GHz. The measured noise figure at f_{RF}=60 GHz keeps around 19 dB for IF2 frequencies from 100 MHz to 2.2 GHz. For a 60-GHz gigabit transmission, the IF2 bandwidth must be higher than 1 GHz for a 2-GHz RF channel. Here, the demonstrated dual-conversion down-converter has enough RF and IF bandwidths. Finally, the measured output IQ waveform under fIF2=1 GHz is shown in Fig. 15. The phase and amplitude errors are 0.3° and 0.8 %, respectively.

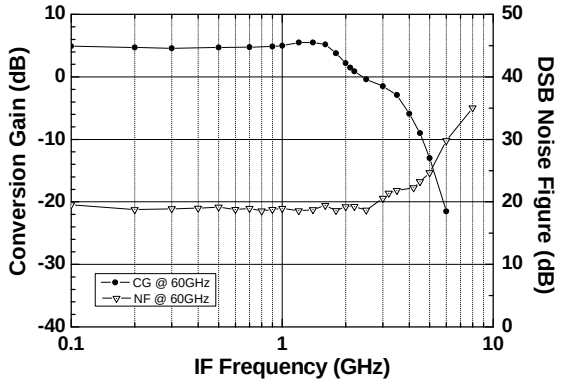


Fig. 14. Measured conversion gain and noise figure of the 60-GHz dual-conversion down-converter using 0.18-μm CMOS technology.

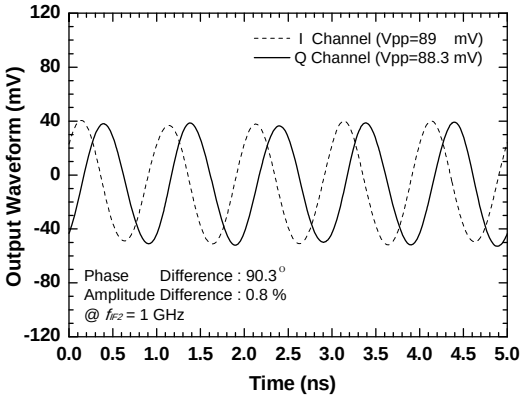


Fig. 15. Measured I/Q output waveform of the 60-GHz dual-conversion down-converter using 0.18-μm CMOS technology.

Table I.

COMPARISON OF MICROWAVE/MILLIMETER-WAVE SUB-HARMONICALLY PUMPED DIODE MIXERS

	Tech.	f_{RF} (GHz)	CL (dB)	P_{LO} (dBm)	2LO-to-RF Isolation (dB)	Size (mm^2)
[35]	GaAs	40	10	6	75	1.7x2.2
[36]	GaAs	58.5~60.5	11.3	7	N.A.	2.3x3
[37]	GaAs PHEMT (0.15 μm)	23~27	10~12	13	50~65	0.85x0.85
[38]	GaAs PHEMT	33-42	10~13	2*a	>37	0.81x1.34
[20]	Si-based diode	24	15.2	1.5*b	N.A.	Hybrid
[23]	0.13 μm SiGe BiCMOS	100~120	6~7	16	N.A.	0.78x0.43
[39]	0.18 μm CMOS	10~40	15.6~17.6	8*c	51~59	1.1x0.67
This work*d	0.18 μm CMOS	50~70	~15	1*b	60~65	0.4x0.4

*a Including a LO driving amplifier in the chip
*b Using Schottky Diode
*c Using a gate-drain connected NMOS Diode
*d Used at the high-frequency conversion of the 60 GHz dual-conversion down-converter.

3rd year

As the speed of CMOS technologies improves by the scaling rule, an SOC solution with RF front-end and baseband circuits becomes feasible for the low frequency band. Recently, commercial 5-GHz WLAN transceivers excluding power amplifiers have been realized by advanced CMOS and SiGe BiCMOS technologies. Highly-integrated CMOS transceivers with digital ICs are easily attained, but it is difficult to merge high-power PAs with good linearity into RF transceivers due to the low breakdown voltage and high silicon-substrate coupling. To date, a stand-alone high-power PA has a unique market in 2.4 GHz or 5-GHz WLAN applications. Although CMOS PAs and SiGe PAs have been demonstrated for 2.4 GHz WLAN applications, III-V compound technology is still a good candidate for high power design with excellent linearity and efficiency.

Up to millimeter-wave regime, is a fully CMOS-based design the best solution for 60-GHz transceivers?

In the millimeter-wave regime, HEMT-based LNAs and PAs have superior noise figure at low DC power and larger output power with higher power added efficiency, respectively. The unmatched performances offered by HEMT-based LNA and PA at 60 GHz are still very attractive for millimeter-wave applications. Before introducing the architecture of our work, the performances of 60-GHz LNAs and PAs implemented in different technologies are studied. Figure 1 shows the comparison of stand-alone 60-GHz LNAs using 130-nm, 90-nm, 65-nm CMOS and III-V compound technologies. The noise figure of 60-GHz CMOS-based LNAs slightly improves as the scaling rule, but the III-V compound LNAs with the smaller than 3-dB noise figure obviously prevail. This is because III-V

GaAs-based technologies inherently have superior noise figure under low DC power consumption. The best III-V compound LNA [C1] provides 2-dB NF and 23-dB gain at a drain voltage of 0.8 V and a drain current of 8 mA, due to the minimum NF (NFmin) of 0.6 dB (at 60-GHz) provided by 0.1-μm InP heterojunction FETs. The III-V compound technologies are still very attractive for the 60-GHz LNA design.

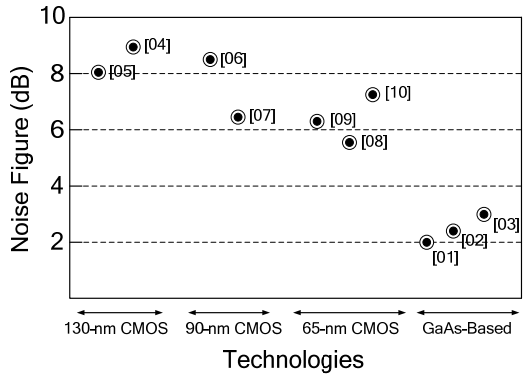
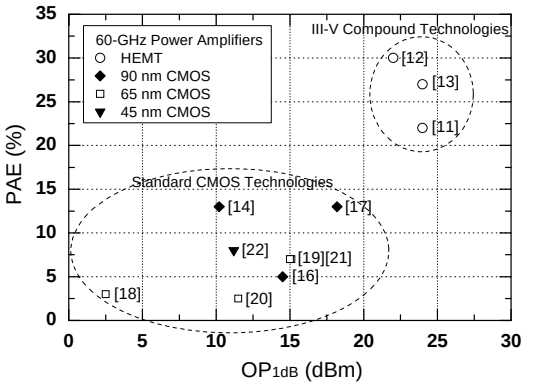


Fig. 1 Comparison of 60-GHz low noise amplifiers using standard CMOS and III-V compound technologies.

Additionally, a power amplifier (PA) is a decisive component in resisting high 60-GHz path loss because its output power determines the maximum transmission distance. A survey of the state-of-the-art 60-GHz PA using advanced CMOS and III-V compound technologies is shown in Fig. 2. Compared with III-V compound technologies, standard CMOS PAs have lower P_{sat} or OP_{1dB}, thus requiring larger DC power consumption for the same required output power. The low breakdown voltage in advanced CMOS processes makes high-power designs difficult. Even through P_{sat} or OP_{1dB} of CMOS PAs can be increased by the current-combing technique, the total DC power consumption is consequently raised and low power added efficiency (PAE) is still an issue for portable applications. In 60-GHz beam-forming phased-array architectures, the DC power consumption becomes more severe due to the greater number of PAs required for the multiple paths of a transmitter.

Complex modulation techniques such as OFDM are used in 60-GHz transmission. Thus, PAE at OP_{1dB} is a proper criterion for verifying the ability of the PA under high-data transmission. Fig. 2(a) shows that PAE and OP_{1dB} decrease as the CMOS device is scaled down. **As a result, there is a trade-off between noise figure and output power in advanced CMOS technologies, and the 60-GHz link budget is still very tight.**

While most other research follows the CMOS scaling rule and employs advanced CMOS technology for the 60-GHz application, an alternative approach illustrated in Fig. 3 is proposed in this project due to the occurrence of Schottky diodes in the foundry CMOS process. Here, LNA and PA are realized using GaAs-based technology while the other circuits of a 60-GHz millimeter-wave front-end are fully implemented in a low-cost 0.18-μm CMOS single chip. In this project, the first 60-GHz Schottky diode based transceiver, excluding the GaAs-based LNA and PA, are demonstrated in a 0.18-μm foundry CMOS process. Two enabling technologies for realizing 0.18-μm CMOS 60-GHz dual-conversion transceivers are the **Schottky Diode** and **Distortionless Microwave Passive Component.** The former has been realized in the first year while the concept of the latter has been proposed and discussed in the second year.



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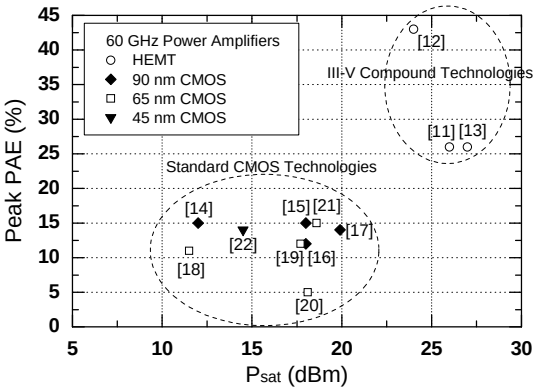


(b)

Fig. 2. Comparison of the 60-GHz power amplifiers using standard CMOS and III-V compound technologies.

Here, we briefly review the history of the Schottky diode realized in the foundry CMOS process. The Schottky diode, a majority-carrier device, has no minority storage effect and thus possesses very high-speed response for mixing and rectification. Among the GaAs-based technologies, Schottky-diode mixers have matured [C23]. However, little attention has been paid to the silicon processes because of the absence of Schottky diodes in a standard CMOS process. A 12-GHz down-converter using silicon Schottky diodes was demonstrated using bipolar technology with an extra processing step for Schottky diodes [C24]. In 1996, the first experimental work to form Schottky diodes without an extra processing step in a foundry CMOS process was demonstrated by arranging the layout layers appropriately [C25]. However, the initial rectifying effect of the Schottky diodes was limited to 600 MHz, possibly due to the long wire bonding used in the measurement set-up. Until 2005, Schottky diodes with a cut-off frequency beyond

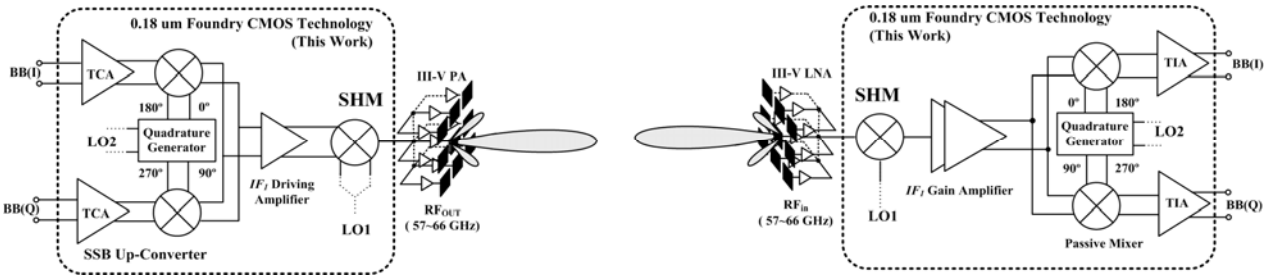
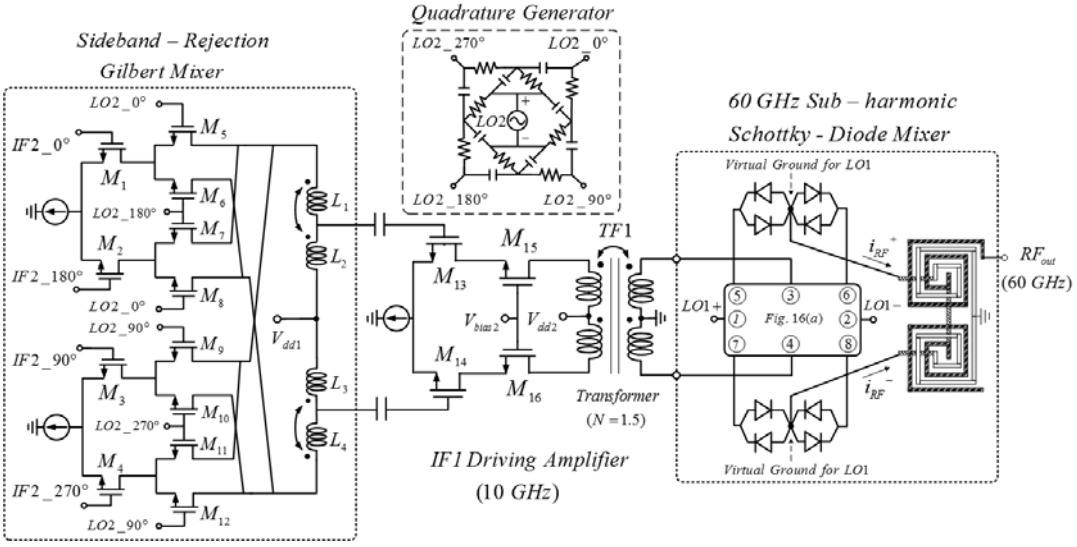


Fig. 3. Block diagram of the demonstrated dual-conversion up-/down- converters using Schottky diodes in 0.18-μm standard CMOS technology for a 60 GHz transmission system.

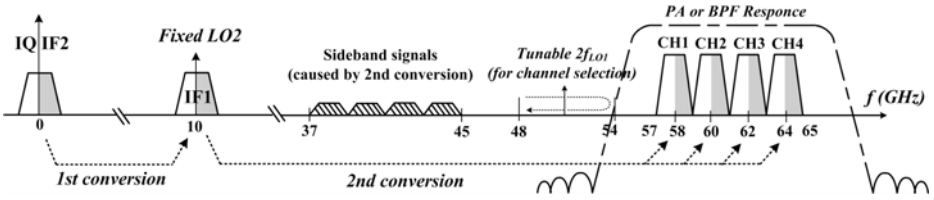
several hundred GHz were developed in standard CMOS [C26]. The Schottky diodes based on the standard silicon process offer superior frequency conversion and thus key components such as signal detectors [C27][C30], frequency doublers [C29], and mixers [C28] have been implemented in the millimeter-wave regime. These results [C27][C29][C30] shed light on the suitability of Schottky diodes in millimeter-wave applications using foundry CMOS process. The Schottky diode, like a catalyst, significantly reduces the R&D cost barriers and makes a 60-GHz transceiver with low-cost CMOS technology possible. However, no millimeter-wave transceiver based on the Schottky diodes has been reported to date.

A direct conversion requires accurate quadrature *LO* signal generation directly at the same frequency of RF signals. Fully integrated transceivers, based on the direct conversion architecture, have been successfully demonstrated below 5 GHz because IQ signal generation is less sensitive to the parasitic effects of the practical layout. When the channel bandwidth approaches several GHz at the millimeter-wave frequency, it becomes difficult to generate a precise, wideband IQ signal at 60 GHz. Thus, as discussed later in this report, a dual-conversion architecture is employed to accomplish the band selection and quadrature generation in two separate steps. As shown in Fig. 3, the block diagrams for the 60-GHz dual-conversion up-/down-converters are depicted inside the dashed-square area. A precise IQ signal is generated by a fixed quadrature LO_2 at low-frequency conversion while channel selection is achieved by sweeping LO_1 at high-frequency conversion. Here, the dual conversion consists of a high-frequency conversion using the microwave/millimeter-wave design approach and a low-frequency conversion using the analog design approach. For the higher-frequency conversion, a dual-band lump-distributed phase-inverter rat-race coupler and a compact trifilar transformer together with anti-parallel diode pairs (APDPs) are proposed for Schottky-diode sub-harmonic down-conversion and up-conversion mixers (SHMs), respectively. The SHMs reduce the *LO* frequency to one-half of a fundamental mixer, and thus alleviate the difficulty of millimeter-wave *LO* generation with 0.18-μm CMOS technology. The proposed SHM topologies provide inherent cancellation among all ports of SHMs to achieve broadband

isolations. For lower-frequency conversion, analog mixers such as resistive and Gilbert mixers are employed due to the size concern. A high-gain *IF1* amplifier is inserted between the high-frequency and low-frequency mixers as shown in Fig. 3. There is however a trade-off in designing the *IF1* frequency. In consideration of the problems of image/sideband signal at the high-frequency conversion, *IF1* designed at higher frequency to facilitate the image/sideband signal suppression is preferred. However, the gain requirement sets an upper limit for the *IF1* frequency. In this work, *IF1* frequency is set at 10 GHz for 0.18-μm CMOS technology. The image/sideband signal is 20 GHz away from the desired RF band of 57 ~ 66 GHz and can be easily filtered out by not only the bandpass response of the 60-GHz LNA/PA but also the preceding RF bandpass filter.



(a)



(b)

Fig. 4. (a) Schematic and (b) frequency planning of the 60-GHz dual-conversion up-converter by using Schottky diodes in the 0.18-μm CMOS technology.

The Methods and Experimental Results of The Demonstrated 60-GHz Dual-Conversion Up-Converter in 0.18 μm Foundry CMOS Technology

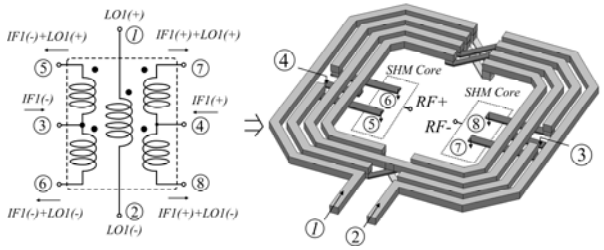
The 60 GHz dual-conversion up-converter and its frequency planning are shown in Figs. 4(a) and 4(b), respectively. The frequency planning is similar to that of the dual-conversion down-converter (realized in second year) for the compatibility with the frequency arrangement of *LO* generator in the 60 GHz dual-conversion down-converter. The IF_1 signal is at 10 GHz when the LO_2 frequency is also fixed at 10 GHz; thus, the sideband signal caused by the high-frequency conversion is 20 GHz away from the 60 GHz channel and easily filtered out by the subsequent bandpass circuits.

However, $2LO_1$ leakage signal, located at 48~54 GHz, is very close to the 60-GHz signal. It is difficult to suppress the $2LO_1$ leakage signal by the subsequent bandpass circuits, meaning that $2LO_1$ leakage signals could be emitted together with the desired 60-GHz signal. A good *2LO-to-RF* isolation is very important in the transmitter design. Thus, an SHM using trifilar transformer is proposed to solve the problem of port-to-port isolations. In addition, the 60 GHz up-converter consists of a single sideband (SSB)

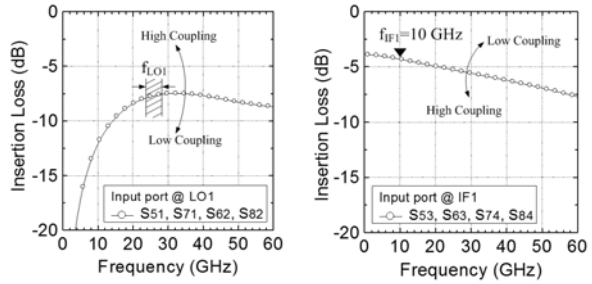
up-conversion mixer pumped by LO_2 signal at low-frequency conversion and an IF_1 differential driving amplifier inserted between the two-step up-conversion stages. Details of the schematics are presented below.

(A) 60 GHz Sub-Harmonic Schottky-Diode Mixer Using Trifilar Transformer

The 60 GHz SHM includes a trifilar transformer for differential IF_1 and LO_1 inputs, series-connected Schottky-diode APDPs in double-balanced configuration for sub-harmonic mixing, and a Marchand Balun for 60-GHz differential RF signal extraction. A trifilar transformer with



(a)



(b) (c)

Fig. 5. (a) The schematic and (b)(c) the simulated insertion loss (for LO_1 and IF_1 signals) of the trifilar transformer used in the sub-harmonically pumped mixer of the 60-GHz dual-conversion up-converter.

2:1:1 turn ratios to implement an SHM in millimeter-wave frequency. The schematic and physical layout are illustrated in Fig. 5(a). The IF_1 signal is fed via the center-taps of two secondary coils while the LO_1 signal is coupled by the magnetic flux from the primary coil to two secondary coils. Due to the port arrangements, the mutual isolations between the LO and IF ports are achieved by the trifilar. As show in Fig. 4(a), two series-connected APDPs are placed at the remaining ports of a trifilar transformer such that the middle point of each series-connected APDPs is a virtual ground for the differential LO_1 signal. Thus, an inherently good *LO_1-to-RF* isolation can be attained because differential RF signals are taken from the virtual-ground points. At the same time, *$2LO_1$-to-RF* isolations are achieved due to the APDP configuration. In order to drive the external single-ended amplifier, a March balun is used for the differential-to-single conversion. The Marchand balun adopts slotted shielding to block the lossy silicon substrate for loss reduction and to reduce the speed of the propagating wave for size reduction. Because there is a wide separation in frequency between IF and RF signals, the IF-to-RF isolation can be achieved by the bandpass response of the Marchand balun.

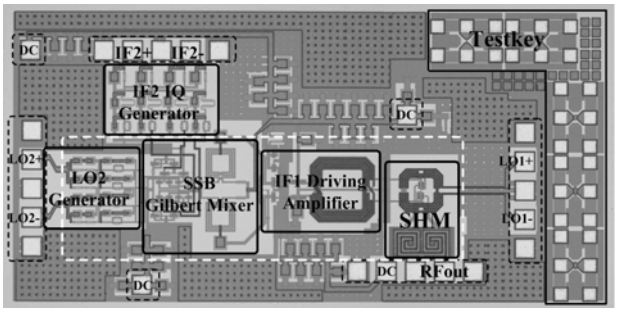


Fig. 6. Die photograph of the 60-GHz dual-conversion up-converter using 0.18-μm CMOS technology.

There is a trade-off in the coupling design for the IF_1 and LO_1 inputs to the ports connected to the APDPs because the trifilar transformer deals with two signals with different frequencies at the same time. All the terminals are labeled as shown in Fig. 5(a). If the coupling between the LO_1 ports (terminals of 1 and 2) to the ports connected to the APDP (terminals of 5, 6, 7 and 8) is too high, the signal transmitted between LO_1 ports to the ports connected to the APDP increases; thus, the required LO_1 power is lowered at the cost of low transmission between IF (terminals of 3 and 4) to the port connected by the APDP (terminals of 5, 6, 7 and 8). Figures 5 (b) and 5 (c) show the *LO_1-to-RF* and *IF_1-to-RF* insertion loss versus operating frequency by EM-simulations. A trade-off between the LO_1 pumping

power and the up-conversion loss exists in designing the coupling strength of a trifilar. In this work, the IF_1-*to-RF* insertion loss at 10 GHz is about 4.5 dB while the LO_1-*to-RF* insertion loss at 23.5~28 GHz is around 7 dB.

(B) 10 GHz Single Sideband Gilbert Mixer and IF1 Differential Driving Amplifier

The 10-GHz SSB mixer consists of two Gilbert multipliers, a quadrature generator and two center-tapped inductors. Each multiplier is composed of a double-balanced Gilbert cell (M_5~M_8 or M_9~M_{12}), IF_2 input trans-conductance stage (M_1~M_2 or M_3~M_4), and one current source. It is difficult to generate a millimeter-wave transmitting signal with good sideband rejection by a direct up-conversion because the parasitic effects degrade the amplitude and phase accuracy of IQ signals. A dual conversion remedies the problem. The SSB mixer is used to up-convert the spectrum of the desired based-band IQ signal to the IF_1 frequency with good sideband rejection at low-frequency conversion. The signal at IF_1 frequency is then up-converted to 60 GHz by an SHM. Because the high-frequency mixer does not have sideband rejection, the IF_1 frequency is set at 10 GHz to enable the undesired sideband signal generated by the high-frequency conversion to be easily filtered out by the subsequent external bandpass filter and power amplifier. Thus, generating a millimeter-wave signal with good sideband rejection is achieved by a two-step conversion. In order to overcome headroom limitation, the T-coil inductors (L_1~L_2 and L_3~L_4) are used as the output load for gain enhancement at f_{IF1}=10 GHz.

The differential driving amplifier, employed between the SHM and the sideband-rejection mixer, raises the IF_1 output power before the IF_1 signal enters the 60-GHz SHM. Because the frequency response of a cascode configuration is better than that of a common-source configuration, a higher maximum available gain (MAG) at 10 GHz can be obtained by the former under the same DC current. Here, the size of each transistor (M_{13}~M_{16}) is 0.18x4x30 μm^2. The fully-differential architecture with symmetrical layout has less sensitivity to the parasitic effects at the ac-ground point. A differential transformer (TF_1) is used at the output load to increase the dynamic range, and also to achieve conjugate impedance match to the SHM's input via a turn ratio of 1.5.

(C) Experimental Results

The die photo of the 60 GHz dual-conversion up-converter is shown in Fig. 6. The circuit area, excluding pads and test-key, is 1.4x0.87 mm^2, and the compact 60-GHz SHM with the compact trifilar transformer occupies a mere 0.23x0.33 mm^2. The differential baseband IQ signals are generated by applying the differential signals to a two-stage polyphase shifter to facilitate the measurement. The IF_2 is designed at 1 GHz for a 2-GHz channel. If the IF_2 IQ generator is also deducted, the area of the SHM, IF_1 amplifier, SSB mixer, and LO_2 generator, is 1.4x0.44 mm^2 (as marked by the white dashed line). The total power consumption of the main circuit is 26 mA at a supply voltage of 2.5 V. Here, the driving IF_1 amplifier consumes most of the DC power.

Figure 7 shows the measured and simulated S-parameter of RF output return loss. The measured RF output return below -10 dB is from 50 to 66 GHz. Figure 8 shows the measured power performance. The OP_{1dB} for each channel is close to -17~-18 dBm and the maximum saturated power is -16 dBm at f_{RF}=58 GHz. Each 60-GHz channel has an almost identical power performance. Moreover, the measured 51~66 GHz conversion gain, shown in Fig. 9, is around -2 dB and the RF bandwidth is basically limited by the output return loss of the RF marchand balun. Within the 3-dB bandwidth, the measured OIP_3 remains around -6 dBm in most cases.

Figure 10 shows the measured SSB output power spectrum at $f_{RF(out)}$=60 GHz and f_{IF2} =1 GHz, and the sideband rejection (SBR) reaches 41.43 dB. The SBR is better than 40 dB over 50~66 GHz and remains nearly

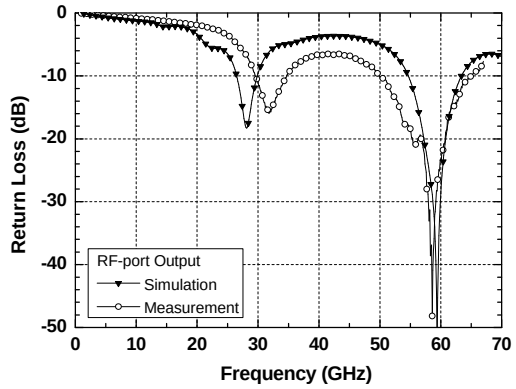


Fig. 7. Measured and simulated *RF* output return loss of the 60-GHz dual-conversion up-converter using 0.18-μm CMOS technology.

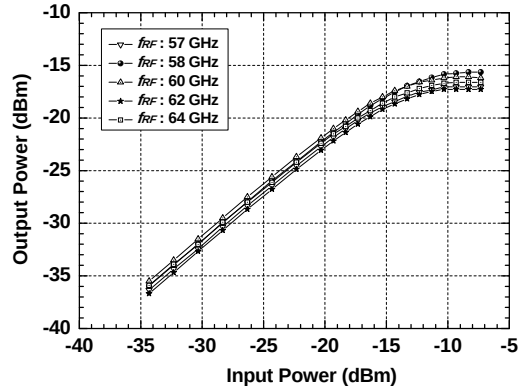


Fig. 8. 60-GHz RF output power verses baseband *IF2* input power for the different RF frequencies.

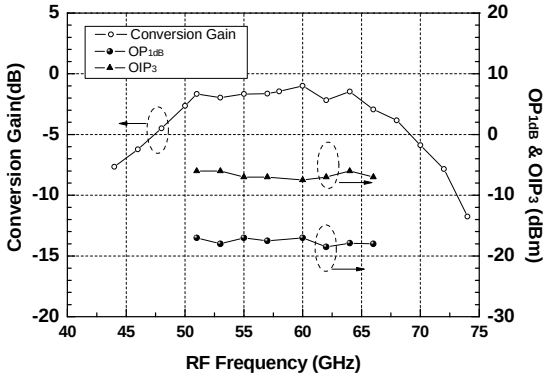


Fig. 9. Measured conversion gain of the 60-GHz dual-conversion up-converter using standard 0.18-μm CMOS technology.

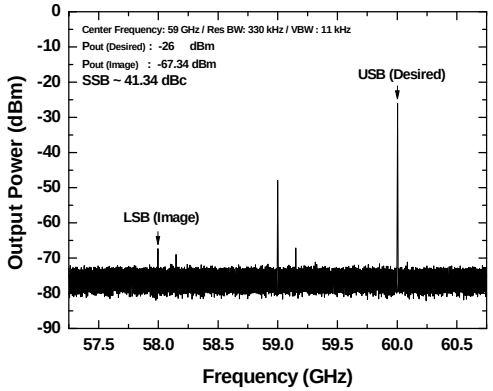


Fig. 10. Sideband rejection ratio (SBR) of the 0.18-μm CMOS 60-GHz dual-conversion up-converter at f_{RF}= 60 GHz.

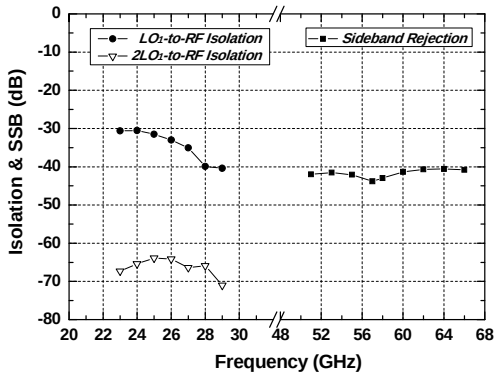


Fig. 11. Measured isolations and sideband rejection of the 60-GHz dual-conversion up-converter verses operating frequency.

constant. The best performance is nearly 44 dB rejection at $f_{RF(out)}$=57 GHz, meaning that the LO_2 quadrature signal keeps the amplitude and phase errors smaller that 0.2 dB and 1 ° , respectively. Moreover, the $2f_{LO1}+f_{LO2}$ (10-GHz LO_2 signal leaked to the *RF* interest band) suppression, referring to desired output power, is about 22~23 dBc. The measured suppression and isolations across the entire 60 GHz bandwidth are shown in Fig. 11. Here, LO_1*-to-RF* isolation is about 30~40 dB, and 2LO_1*-to-RF* isolation is better than 65 dB thanks to the fully-symmetrical design of the double-balanced SHM by using the trifilar transformer and the APDPs structure.

The performances of the 60-GHz up-converter and other state-of-the art up-converters at millimeter-wave frequency are summarized in Table II. Our proposed dual-conversion up-converter has the highest SBR over the 60 GHz bandwidth of any circuit on the list.

TABLE II.
COMPARISON OF SINGLE-SIDEBAND REJECTION OF MICROWAVE/MILLIMETER-WAVE UP-CONVERTERS

	Technology	f_{RF} (GHz)	*CL* (dB)	In-Band *LO2* Rejection (dBc)	SBR (dBc)	Size (mm^2)
[34]	0.3 μm GaAs MESFET	22~26	13	> 20	24	2.8x1.28
[35]	0.13 μm CMOS	20~40	13	20~30	> 20 #a	0.68x0.58
[36]	0.13 μm CMOS	35~65	6	> 24 #b	> 20	0.98x0.8
[37]	GaAs	44.5	11	10~20 #b	20~30	1.7x1.7
[38]	GaAs HBT	50~110	< 20	15~23	22	2.0x2.0
[39]	GaAs	76.5	12~15	< 10	24	2.0x1.6
[40]	Hybrid	60	14.2	N.A.	> 20	5.15x1.35
[41]	90-nm CMOS #d	60	N.A.	N.A.	20 #c	0.49x0.42
This work	0.18 μm CMOS #d	57~65	1	22 ~ 23 #e	**> 40 #f**	1.5x0.87

#a SSB>40 dBc only from 27 GHz to 30 GHz
#b 2*LO Suppression (SHM)
#c SSB is achieved by using polyphase filter at 60 GHz
#d Dual-conversion up-converter
#e $2*f_{LO1}+f_{LO2}$ suppression (DUC)
#f This performance **almost remains the same** over whole interesting 60 GHz bandwidth

IV. Conclusions

1st year

In the first year we analyzes the step-impedance technique on the silicon process for miniature, wide-band and low-loss phase-inverter rat-race coupler design. A design guideline for the step-impedance phase-inverter rat-race coupler on lossy silicon substrate is developed. Large shrinkage must be in consideration of required return-loss bandwidth and realizable impedance limitation at the same time. Thus, the inter-digital coplanar stripline structure and Chebyshev design are adopted to extend the low impedance boundary for large size shrinkage and bandwidth increase, respectively. A demonstrated 10-GHz step-impedance rat-race coupler with impedance ratio of 6 has insertion loss about 6~7 dB from 5 GHz to 15 GHz. When compared with our previous work, the insertion loss is obviously reduced. Thus, a 0.13-μm CMOS broadband Gilbert down-converter with the proposed step-impedance phase-inverter rat-race coupler at the RF stage has conversion gain above 8 dB from 7 to 18 GHz and noise figure of 16 dB which means that the miniaturized rat-race coupler suffers less from the substrate loss.

2nd year

An effective way for size reduction (distortionless transmission line theory and lumped-distributed technique) and bandwidth extension (Chebyshev response design) is proposed to greatly shrink a phase-inverter rat-race coupler, and a 0.35-μm SiGe BiCMOS Gilbert down-converter with the lump-distributed phase-inverter rat-race coupler is successfully demonstrated for UWB applications.

The introduction of Schottky diodes with a cut-off frequency of several hundred GHz in standard CMOS process has changed the scenario of the scaling rule. The demonstrated 60-GHz dual-conversion down-converter, operating from 57~66 GHz, has conversion gain of 5 dB, IP1dB of -5 dBm and IIP3 of 5 dBm. The corresponding Schottky-diode SHM requires only the small LO power of 1 dBm.

3rd year

The introduction of Schottky diodes with a cut-off frequency of several hundred GHz in standard CMOS process has changed the scenario of the scaling rule. This enabling technology makes possible the implementation of 60-GHz dual-conversion up-/down-converters using 0.18- m foundry CMOS process even though MOS transistors have only fT/fmax of 50-GHz/60-GHz. Additionally, both microwave/millimeter-wave and analog design approaches are used to accomplish the low-cost 60-GHz transceiver. In the dual-conversion architecture, 60 GHz Schottky-diode SHMs are employed in the high-frequency conversion while analog mixers with accurate IQ signal generation are chosen for low-frequency conversion. Because the silicon-based Schottky diode possesses a low turn-on voltage and the

advanced passive circuits, such as the proposed phase-inverter rat-race coupler and trifilar transformer, are available, the Schottky-diode millimeter-wave mixers using low-cost foundry CMOS process becomes practical. The demonstrated 60-GHz dual-conversion down-converter (in the second year), operating from 57~66 GHz, has conversion gain of 5 dB, IP1dB of -5 dBm and IIP3 of 5 dBm. The corresponding Schottky-diode SHM requires only the small LO power of 1 dBm. For the 60-GHz dual-conversion up-converter (in the third year), conversion gain of -2 dB, OP1dB of -17 dBm, and broadband sideband rejection better than 40-dB are achieved. Based on the results of this work, incorporating the demonstrated 0.18- m CMOS dual-conversion up-/down-converters with high-performance HEMT-based LNA and PA gives an alternative attractive solution for 60-GHz transmission.

V. Reference

1st year

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