行政院國家科學委員會專題研究計畫 期中進度報告

金屬閘極/高介電係數材料互補式金氧半場效電晶體在45到22奈米世代之應用(2/3)

期中進度報告(精簡版)

計 畫 類 別 ：整合型
計 畫 編 號 ：NSC 98-2120-M-009-005-
執 行 期 間 ：98年08月01日至99年07月31日
執 行 單 位 ：國立交通大學電子工程學系及電子研究所

計 畫 主 持 人：荊鳳德
共 同 主 持 人：管傑雄、張廖貴術、王水進、巫勇賢

報 告 附 件 ：出席國際會議研究心得報告及發表論文

處 理 方 式 ：本計畫可公開查詢

中 華 民 國 99年05月17日

行政院國家科學委員會補助專題研究計畫 □ 成果報告 ■期中進度報告

金屬閘極/高介電係數材料互補式金氧半場效電晶體在45 到22 奈米世代之應用(2/3)

計畫類別：□ 個別型計畫　　■ 整合型計畫

計畫編號：NSC 98-2120-M-009-005

執行期間：　2009　年　8　月　1　日至　2010 年　7　月　31　日

計畫主持人：荊鳳德教授(國立交通大學電子工程學系及電子研究所)

共同主持人：管傑雄教授(國立臺灣大學電子工程學研究所)

張廖貴術教授(國立臺灣大學工程與系)

巫勇賢助理教授(國立臺灣大學工程與系統科學系)

王水進教授(國立成功大學微電子工程研究所)

計畫參與人員：陳維邦、周坤億、蔡竣揚、劉思麟

成果報告類型(依經費核定清單規定繳交)：■精簡報告　□完整報告

本成果報告包括以下應繳交之附件：

□赴國外出差或研習心得報告一份

□赴大陸地區出差或研習心得報告一份

□出席國際學術會議心得報告及發表之論文各一份

□國際合作研究計畫國外研究報告書一份

處理方式：除產學合作研究計畫、提升產業技術及人才培育研究計畫、列管計畫及下列情形者外，得立即公開查詢

□涉及專利或其他智慧財產權，□一年□二年後可公開查詢

執行單位：國立交通大學電子工程學系及電子研究所

中　華　民　國　99　年　5　月　12　日

金屬閘極/高介電係數材料互補式金氧半場效電晶體在45到22奈米世代之應用(2/3)

"Metal-gate/ high-κ CMOSFETs for 45 to 22 nm technology nodes"

計畫編號：NSC 98-2120-M-009-005

執行期間：98 年 08 月 01 日至 99 年 07 月 31 日

主持人：荊鳳德 交通大學電子工程系教授

一、中文摘要

高的「臨界電壓」(V_t)是「金屬閘極/高介電係數」互補式「金氧半場效電晶體」的主要挑戰，我們發現了較高的「臨界電壓」主要是由於在小的「等效氧化層厚度」(EOT)下「平帶電壓」(V_{fb})下降所導致。而「平帶電壓」的下降，其物理機制為帶電的氧缺陷在界面上反應所產生。我們利用先進的低溫製程來降低界面反應的問題。利用此方法，在「自我對準」和「閘極優先」的互補式「金氧半場效電晶體」上，可以在「等效氧化層厚度」0.6~0.7 奈米時達到低的 0.12 and -0.17 V「臨界電壓」。

二、英文摘要

The toughest challenge for metal-gate/high-κ CMOS is to lower the undesired high threshold voltage (V_t) at smaller equivalent-oxide thickness (EOT) [1]-[9], which is opposite to scaling trend of low power ICs. The high V_t issue is especially hard for *p*-MOS, since only Ir and Pt in the Periodic Table have the needed high work-function larger than the target 5.2 eV. Unfortunately, both Ir and Pt are not thermally stable on thin high-κ dielectric [1]. Further, the flat band (V_{fb}) roll-off at smaller EOT even worsens the required low V_t challenge [6]-[7]. The tough challenge is evident from the slower EOT scaling: 1.0 nm EOT of Intel 1st-generation high-κ + metal-gate CMOS for 45 nm node (*IEDM 2007*) to only 0.95 nm EOT of 2nd-generation technology for 32 nm node (*IEDM 2009*). To address these issues, in this paper we present possible mechanism for the high V_t issue from our experiment data, which is due to flat-band voltage (V_{fb}) roll-off at smaller EOT. A mechanism of charged oxygen vacancies formed by interface reaction was proposed to explain the V_{fb} roll-off effect. Based on this mechanism, a novel process method has been used that leads to the low V_t metal-gate/high-κ CMOSFETs at 0.6~0.7 nm EOT with several orders of magnitude lower gate leakage. Such small EOT is significantly smaller than the 0.95 nm EOT used in Intel's 2nd-generation high-κ + metal-gate CMOS at 32 nm node.

二、計畫的緣由與目的

A fundamental challenge for metal-gate/high-κ *C*-MOSFETs is the undesirable high threshold voltage (V_t) that is opposite to low voltage scaling trend. This is especially difficult for high work-function *p*-MOS, since only Ir and Pt in the Periodic Table have the required high work-function greater than the target 5.2 eV. However, both Ir and Pt fail for *p*-MOS devices, due to metal diffusion through the high-κ dielectric during the 1000°C RTA necessary for ion-implanted source-drain activation [1]. Although thermal stability up to 1000°C can be achieved by using an Ir_3Si gate [4]-[5] on HfLaON developed by us, this yields a V_t of only -0.1 V, at 1.6 nm equivalent-oxide-thickness (EOT). Unfortunately this value increases at a thinner EOT of 1.2 nm due to the roll-off of the flat-band voltage (V_{fb}) [6], as a result of reactions and inter-diffusion at the high-κ/Si interface. Although the interfacial reaction can be decreased by inserting a thin SiO_2 layer, this may not work when the EOT is scaled down to ~0.7 nm. This is evident from the limited EOT scaling of 1.0 to 0.95 nm with down-scaling the technology from 45 to 32 nm nodes. Such negligible EOT scaling is much slower than the EOT proposed by *International Technology Roadmap for Semiconductor*s (*ITRS*). Since the inevitable interfacial reactions follow an Arrhenius temperature dependence, low-temperature processing is essential. This has been verified by the low V_t in metal-gate/high-κ *p*-MOSFETs in our previous works when a < 900°C solid-phase diffusion (SPD) was used to form the ultra-shallow junctions [6] and laser-annealing of the laser-reflective-gated CMOS with an EOT in the range 1.05~1.2 nm [7].

To address these issues, in this paper we present a possible mechanism of V_{fb} roll-off effect at smaller EOT – the charged oxygen vacancies generated by interface reaction. Based on the proposed mechanism, we have developed a low temperature process for metal-gate/high-κ CMOS silicide-induced doping for source-drain shallow junction. The fabricated metal-gate/high-κ CMOSFETs using this method have good control of V_{fb} roll-off with low V_t values of 0.12 and -0.17 V at small 0.6~0.7 nm EOT, with several orders of magnitude lower gate leakage

than poly-Si/SiO_2 stack at the same EOT. Such good transistor performance further supports our proposed mechanism of V_{fb} roll-off effect.

三、研究方法及成果

A. *Experimental procedure:*

Standard Si wafers with ~10 ohm-cm resistivity were used in this study. To increase the κ value, we added higher κ TiO_2 dielectric into our pioneered La_2O_3 [8]-[9]. The TiO concentration is ~25% as controlled by the calibrated thickness rate during LaTiO deposition. After depositing the high-κ gate dielectrics on Si substrate using physical vapor deposition (PVD), a post-deposition anneal (PDA) under O_2 is applied to decrease the defects in gate dielectric. Then different low and high work-function TaN and Ir metal-gates were deposited on high-κ dielectric using PVD and subsequent gate patterning for *n*- and *p*-MOSFETs, respectively.

After gate patterning, self-aligned 20 nm or Sb 5 nm Ga and thin Ni were deposited for respective *n*- and *p*-MOSFET, followed by silicide-induced doping at 600~650°C RTA and removing the non-reacted metals [6]. The Ni-induced SPD is similar to dopant segregation technique, where both cases use the silicidation to drive in the impurities. However, the impurities in dopant segregation technique were delivered by ion-implantation, while in Ni-induced SPD used the PVD deposited Ga and drive in [8]-[9]. The fabricated MOSFETs were characterized by capacitance-voltage (*C-V*) and current-density-voltage (*J-V*) measurements.

B. *Interface reaction and V_{fb} roll-off at thinner EOT*:

Figure 1 shows the *C-V* characteristics of HfLaON CMOS. The adding La_2O_3 into HfO_2 with nitridation can achieve wanted negative V_{fb} in TaN/HfLaON n-MOS at 1.6 nm EOT, while needed positive V_{fb} is also reachable using high work-function Ir_3Si gate on HfLaON, even after 1000°C RTA. These results indicate the good V_{fb} control for n- and p-MOS in top metal-gate/high-κ interface. The nitridation is important for HfLaON to preserve an amorphous structure at 1000°C RTA, where the HfLaO starts to crystallize at RTA temperature above 900°C RTA.

However, as the EOT of HfLaON gate dielectric scaled down to 1.2 nm, severe V_{fb} roll-off was found using the same Ir_3Si metal-gate on HfLaON gate dielectric. Although negative V_{fb} was still obtained for n-MOS using lower work-function $HfSi_{2-x}$ gate on HfLaON gate dielectric, no proper work-function metal-gate can be used for p-MOS under the requirement of 1000°C RTA for process integration.

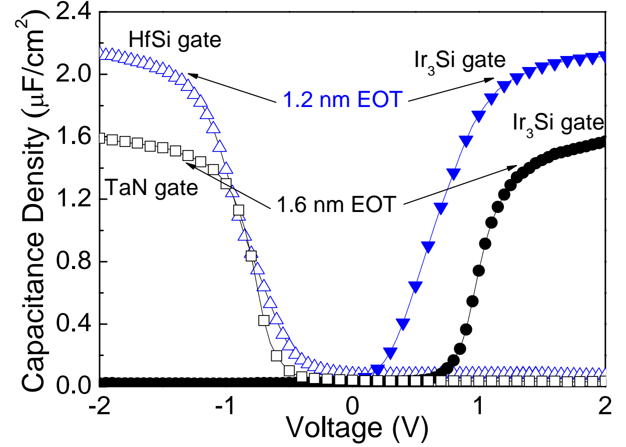


Fig. 1. *C-V* characteristics of mixed high-κ HfLaON n- and p-MOS capacitors with various metal-gates after 1000°C RTA. The V_{fb} roll-off is found at smaller EOT.

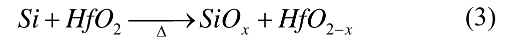
To analyze the V_{fb} roll-off effect from 1.6 nm to 1.2 nm EOT, we have examined the V_{fb} dependence. The V_{fb} is related to the fixed oxide charges (Q_f), distributed oxide charges $\rho_{ox}(x)$), work-function difference between metal-gate and Si ($\Phi_{MS} = \Phi_M - \Phi_S$), and V_t:

$$V_{fb} = \Phi_{MS} - \frac{Q_f}{C_{ox}} - \frac{1}{C_{ox}} \int_0^{t_{ox}} \frac{x}{x_{ox}} \rho_{ox}(x) dx \quad (1)$$

$$V_t = V_{fb} + 2\varphi_F + Q_{dep}/C_{ox} \quad (2)$$

Here C_{ox} is the gate capacitance, Q_{dep} is the depletion charge and $2\varphi_F$ is the surface potential bending at onset of charge inversion. Since the same Ir_3Si/HfLaON gate stack and 1000°C thermal cycle were used, the V_{fb} roll-off at thinner EOT is unlikely from the top metal/high-κ interface or Φ_M difference. The φ_F, Φ_S and Q_{dep} depend strongly on the doping concentration of Si, which is also kept the same when scaling down the EOT. Therefore, the V_{fb} roll-off at thinner EOT is due to oxide charges and/or dipoles from the above equation.

Here we propose that the oxide charges at thinner EOT are generated from interface reaction at high temperature:



$$Si + HfO_2 \xrightarrow[\Delta]{} SiO_x + HfO_{2-x} \quad (3)$$

Such interface reaction, generating oxygen vacancy charges of non-stoichiometric SiO_x and HfO_{2-x} (x<2), is inevitable at 1000°C RTA due to the close bond enthalpy of SiO_2 (800 kJ/mol) and HfO_2 (802 kJ/mol) [1]. Here the bond enthalpy is defined as the standard molar enthalpy change of bond dissociation. From the interface reaction and V_{fb} roll-off effect at thinner EOT, the bottom high-κ/Si interface is also the key factor for low V_t CMOS.

C. *Solution - silicide-induced doping for source-drain shallow junction:*

To further investigate our proposed V_{fb} roll-off effect by interface reaction, we have measured RTA temperature dependence on *C-V* characteristics of higher κ TaN/LaTiO p-MOS capacitors under different 600~900°C temperature. As shown in Fig. 2, the V_{fb} roll-off increases with increasing RTA temperature from 600 to 900°C. In addition, a degraded EOT is also found with increasing RTA temperature.

We have used cross-sectional TEM to analyze the EOT degradation with increasing RTA temperature. As shown in Fig. 3, the degraded EOT is due to the forming thicker interfacial oxide layer as observed by cross-sectional TEM. These results were predicted by the V_{fb} roll-off mechanism proposed in *eq*(1)- *eq*(3), which is also srelated to the interface reaction trongly. Besides, the V_{fb} roll-off effect can also be decreased by decreasing process temperature.

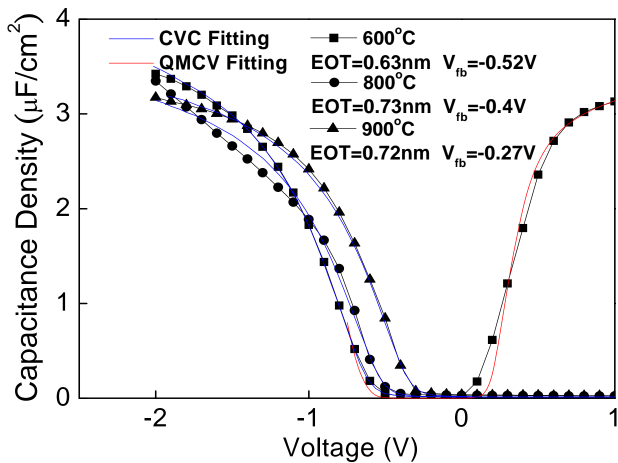


Fig. 2. The PDA temperature dependence on *C–V* characteristics of TaN/LaTiO/p-Si n-MOS devices. The 600°C *C–V* data were measured in a MOSFET from accumulation to inversion, while the 800°C and 900°C *C–V* data were measured in MOS capacitors from accumulation to depletion.

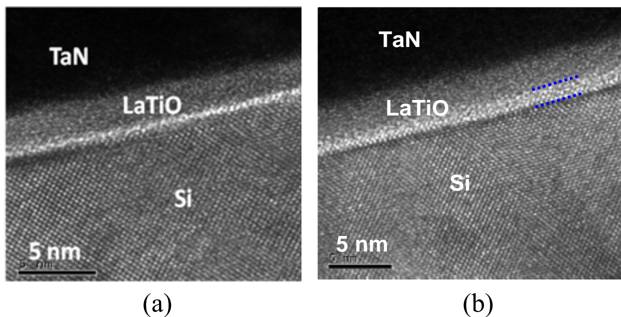


Fig. 3. The cross-sectional TEM pictures of TaN/LaTiO/p-Si n-MOS devices after 600°C and 900°C RTA.

Using the low temperature process of 600~650°C and high work-function Ir gate metals, we have also fabricated the Ir/LaTiO *p*-MOS capacitors, in additional to the TaN/LaTiO *n*-MOS capacitors in Fig. 2. As shown in the *C-V* characteristics of Fig. 4, proper positive V_{fb} value with small hysteresis is still obtained even at small EOT of 0.66 nm for *p*-MOS capacitors.

It is important to notice that the different EOT value between *n*- and *p*-MOS devices is due to the process variation and the different electron and hole effective mass and wave-function distribution, from quantum-mechanical *C-V* calculation.

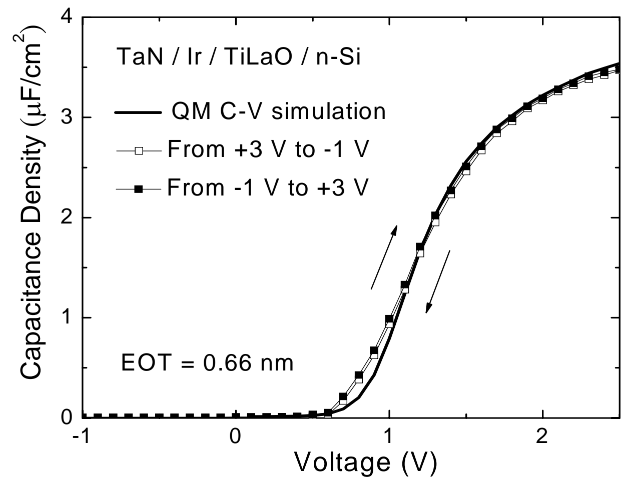


Fig. 4. [TaN-TaN/Ir]/LaTiO *p*-MOS capacitors.

However, the challenge is how to fabricate the MOSFET at low temperature. Conventionally, a high temperature RTA of 1000°C is required to activate ion-implanted dopants in the source-drain of a MOSFET. The other methods to dope the source-drain at low temperature are the solid-phase diffusion [6] and silicide-induced doping [8]-[9]. Here we used silicide-induced doping to fabricate the CMOS devices since it has even lower process temperature than using solid-phase diffusion.

Figures 5(a) and 5(b) show the transistor I_d-V_g characteristics of self-aligned and gate-first TaN/LaTiO *n*-MOSFETs and Ir/LaTiO *p*-MOSFETs, respectively. Low V_t of -0.17 and 0.12 V were reached at these small EOT of 0.63 and 0.66 nm for *n*- and *p*-MOSFETs, respectively. These excellent results are due to the using higher κ LaTiO gate dielectric and low temperature (600~650°C) NiSi-induced doping in source-drain. Such small EOT is significantly smaller than the 0.95 nm EOT used in Intel's 2nd-generation high-κ + metal-gate CMOS at 32 nm node (*IEDM 2009*). These results further support our proposed interface reaction mechanism with its Arrhenius temperature dependence.

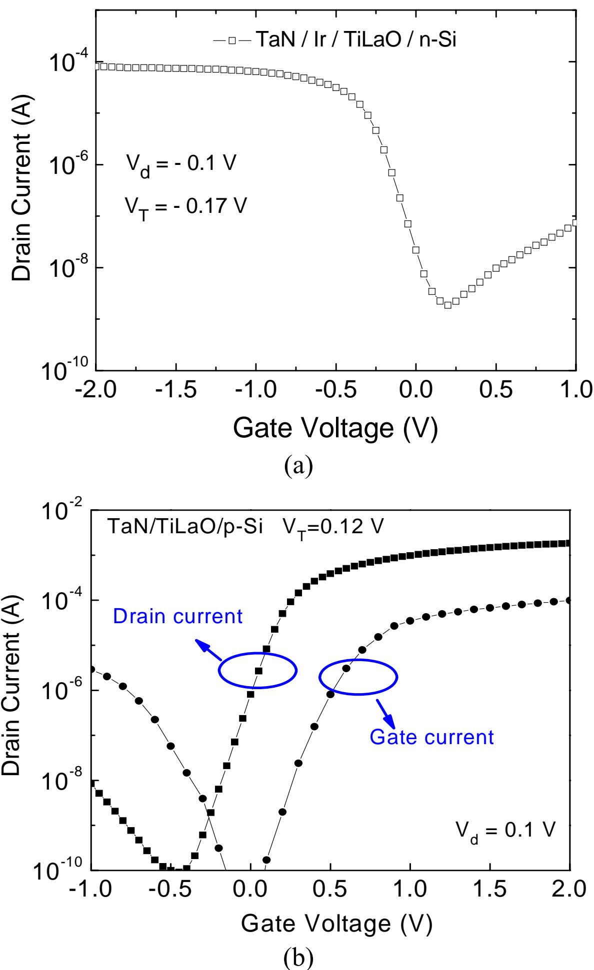


Fig.5 I_d-V_g characteristics of self-aligned and gate-first (a) TaN/LaTiO *n*- MOSFETs and (b) Ir/LaTiO *p*-MOSFETs.

四、結論與討論

We have analyzed the V_{fb} roll-off effect at smaller EOT and proposed a mechanism of charged oxygen vacancies by interface reaction for the explanation. The interface reaction can also be decreased by using novel low temperature process from its Arrhenius temperature dependence. Using a simple process, we have fabricated metal-gate/high-κ TaN/LaTiO *n*-MOSFET with a low V_t of 0.12 V at 0.63 nm EOT and Ir/LaTiO *p*-MOSFET with a low V_t of -0.17 V at 0.66 nm EOT. Besides, this device has the advantages of simple self-aligned and gate-first process compatible with current VLSI.

五、Reference

[1]. D. S. Yu, Albert Chin, C. H. Wu, M.-F. Li, C. Zhu, S. J. Wang, W. J. Yoo, B. F. Hung and S. P. McAlister, “Lanthanide and Ir-based dual metal-gate/HfAlON CMOS with large work-function difference,” in *IEDM Tech. Dig.*, 2005, pp. 649-652.

[2]. C. H. Wu, D. S. Yu, Albert Chin, S. J. Wang, M.-F. Li, C. Zhu, B. F. Hung, and S. P. McAlister, “High work function Ir_xSi gates on HfAlON p-MOSFETs,” *IEEE Electron Device Lett.* 27, no. 2, pp. 90-92, 2006.

[3]. X. P. Wang, C. Shen, M.-F. Li, H. Y. Yu, Y. Sun, Y. P. Feng, A. Lim, H. W. Sik, A. Chin, Y. C. Yeo, P. Lo, and D. L. Kwong, “Dual metal gates with band-edge work functions on novel HfLaO high-κ gate dielectric,” in *Symp. VLSI Tech. Dig.*, 2006, pp. 12-13.

[4]. C. H. Wu, B. F. Hung, Albert Chin, S. J. Wang, X. P. Wang, M.-F. Li, C. Zhu, Y. Jin, H. J. Tao, S. C. Chen, and M. S. Liang “High temperature stable [Ir_3Si-TaN]/HfLaON CMOS with large work-function difference,” in *IEDM Tech. Dig.*, 2006, pp. 617-620.

[5]. B. F. Hung, C. H. Wu, Albert Chin, S. J. Wang, F. Y. Yen, Y. T. Hou, Y. Jin, H. J. Tao, S. C. Chen, and M. S. Liang, “High Temperature Stable Ir_xSi Gates with High Work Function on HfSiON p-MOSFETs,” *IEEE Trans. Electron Device*, vol. 54, no. 2, pp. 257-261, 2007.

[6]. C. F. Cheng, C. H. Wu, N. C. Su, S. J. Wang, S. P. McAlister and Albert Chin, “Very low V_t [Ir-Hf]/HfLaO CMOS using novel self-aligned low temperature shallow junctions,” in *IEDM Tech. Dig.*, 2007, pp. 333-336.

[7]. C. C. Liao, Albert Chin, N. C. Su, M.-F. Li, and S. J. Wang, “Low V_t gate-first Al/TaN/[Ir_3Si-$HfSi_{2-x}$]/HfLaON CMOS using simple process,” in *Symp. on VLSI Tech. Dig.*, 2008, pp. 190-191.

[8]. S. H. Lin, C. H. Cheng, W. B. Chen, F. S. Yeh, and Albert Chin, “Low Threshold Voltage TaN/Ir/LaTiO *p*-MOSFETs Incorporating Low-Temperature-Formed Shallow Junctions,” *IEEE Electron Device Lett.*, vol. 30, pp. 681-683, June 2009.

[9]. S. H. Lin, C. H. Cheng, W. B. Chen, F. S. Yeh, and Albert Chin, “Low Threshold Voltage TaN/LaTiO n-MOSFETs with Small EOT,” *IEEE Electron Device Lett.*, vol. 30, pp. 999-1001, Sept. 2009.

六、Invited Papers (List from Aug. 2009~May 2010)

[1] **Albert Chin**, M. F. Chang, S. H. Lin, W. B. Chen, P. T. Lee, F. S. Yeh, C. C. Liao, M.-F. L, N. C. Su and S. J. Wang “Flat Band Voltage Control on Low V_t Metal-Gate/High-k CMOSFETs with small EOT,” 16th Bi-Annual Conference on Insulating Films on Semiconductors (INFOS), pp. 1728–1732, Cambridge University, UK, June 29~July 1, 2009. **(Invited)**

[2] **Albert Chin**, S. H. Lin, K. C. Chiang, and F. S. Yeh, “Improved Device Characteristics in Charge-Trapping-Engineered Flash Memory Using High-k Dielectrics,” 7th Intl. Symp. on High Dielectric Constant Materials and Gate Stacks, *216th Electro Chemical Society (ECS) Meeting*, Vienna, Austria, Oct. 2009. **(Invited & Session Chair)**

[3] **Albert Chin,** “Charge-trapping memories: materials and devices,” *Materials Research Society* (*MRS*), San Francisco, USA, April 2010. **(Tutorial & Section Chair)**

[4] **Albert Chin,** “Novel Ultra-Low Energy High-Speed Non-Volatile Memory with Good Retention and Endurance,” CMOS Emerging Technologies, Whistler, BC, Canada, May 2010. **(Invitation only)**

Travel Reports

I. Nano Technology 2010, Tokyo, Japan

本次因國科會“奈米國家計畫辦公室”之邀請，至日本東京參加「國際奈米展」(Nano Technology 2010, //www.nanotechexpo.jp/)，其展出的時間從 2 月 17 日(星期三)至 2 月 19 日(星期五)，展出的地點在東京灣展場(Big Sight)，為了使參展成功，本實驗室除了我以外更有博士後鄭存護研究員，及兩位博士班的同學蔡竣揚(博二)及周坤億(博二)。我於 2 月 16 日(星期二)一大早 7:40 分搭乘華航飛機至東京，到達旅館時已下午三點。於放下行李後，我們及出發至 Big Sight 展場，加以佈置及整理。

次日星期三為展場開幕第一天，我們於大多的時間都在自己展出的位置，向參訪者介紹。由於此次奈米展為國際性質，其他歐美的研究單位及公司亦有參加，因此參與之人員十分眾多。此外，欲參觀“國際奈米展”之民眾均需要填寫資料及換牌，因此主辦單位可正確的統計人數。首日參加”國際奈米展”之人數，則高達一萬五千多人，將展場擠得水洩不通盛況空前。

第二天(星期四)之展出，狀態和第一天差不多，除了人數再多一、二千人。由於第一天的參展經驗，我們比較有時間分配人手於我們參展之位置，因此我可以找到時間去參觀其他展出之產品。花了大半天的時間參觀，其中重要的發明首推日本東京大學所推出之“塑膠電子”。此發明將電子元件技術及積體電路製作於塑膠基板上。此外，此塑膠基板可製作成可伸縮的產品，對於未來的“人工皮膚”及「感應器」(Sensor)有重大的貢獻。此「人工皮膚」亦可應用於日本發展之重點“機器人”，因為其手部的“感應器”為機器人的重要技術。此可“伸展性塑膠電子”之重要性，可由大會特別安排日本東京

大學 Someya 教授之演講得知，其演講時間半小時，座無虛席，我亦在聽一次他的演講，(前一次於去年 12 月初於 IEEE International Electron Devices Meeting, IEDM)此次，再加深了印象，其"伸展性塑膠電子"真的是人類的重大發現。此外，於第二天參展晚上，有邀請各國人員出席之 receiption，我們亦出席並和其他國家展出者互相交換資訊，及進行國名外交。

第三天最後一日之參展，其狀況和和前兩日相同，我再藉此機會和各國參展單位進行學術交流，其中主要和日本「National Institute of Advanced Industrial Science & Technology」(AIST，日本先進工業科學&技術國家研究室)進行討論，因為我們今年初已正式和 AIST 簽訂技術合作協定，並進行台灣國科會 NSC 和日本 Japan Science & Technology (JST)之合作計畫。

此次我們展出了所研發之 high-k MOSFET，新世代的快閃記憶體及高頻 RF Power 元件。此次參展收穫良多，有日本更司有興趣和我們進一步說合作事宜。我於星期五晚上回到台灣，此次參展，雖然在農曆年初三尚在放假時，然而得到日本奈米科技研發第一手資訊，收穫良多。

II. IEDM Executive Committee Planning Meeting & IEEE Electron Device Society Distinguished Lecture

此次美國之行乃代表臺灣學術界至美國佛羅里達州出席 IEEE International Devices Meeting (IEDM) 之 Executive Committee Planning Meeting (執行委員會議) 及 IEEE Electron Device Society (電子元件學會) 之 Distinguished Lecture (傑出演講)，我於 3 月 6 日搭乘華航由台北至洛杉磯，再於當日晚上轉機至佛羅里達州 Orlando (奧蘭多)，已是次日早上了。到達奧蘭多後，再租車開至 Tampa 會議地點，住進旅館時，已近中午。此行程雖然十分辛苦，在飛機上過夜，然卻可替國家省下一晚的旅館費，省下一次至 Tampa 之來回機票。

次日 IEDM (國際電子元件會議) 由早上 7:30 分級開始，主要的任務包含決定重要之 plenary talks、決定 emerging technology 之主要主題及可能講員、short course 之主題、invited talk 之講員及各 sub-committee (次委員會) 成員，包含 CMOS Device & Technology (CDT), Characterization, Reliability & Yield (CRY), Displays, Sensors & MEMS (DSM), Memory Technology (MIT), Modeling & Simulation (MS), Process Technology (PT), Quantum, Power & Compound Semiconductor Devices (QPC), 及 Solid State & Nano-electronic Devices (SSN) Committee。而組成各次委員會之成員，除主席外，共 12 名。一般而言，此 12 名委員會成員，需平均分配於美、歐、及亞洲。然而目前積體電路之製造業，包含邏輯電路、記憶體及通訊電路，已大幅移到亞洲，因此歐洲的次委員會成員，尤其在 PT 及 MT 等領域，只好大幅減少。然而在尖端科技之研發，歐美仍較亞洲為先進，因此在 invited talk (邀請演講) 上，仍較亞洲為多，這也是亞洲各國及工業界需努力的地方。此外，本次會議亦探討了過去幾年亞洲方面論文接受率，雖然亞洲各大

學校及工業界寄出了較歐美更多的論文，然而被接受的比率卻較歐美低得多，這也表示亞洲地區的研發品質有進步的空間，而我身為 Asian Arrangement Chair (亞洲區安排主席)，更有如何提昇論文接受率的任務，我將未來於各國參加國際會議之際，和他國之「國際電子元件學會」的委員共同討論改進之道。再經過一天的討論後，其中一些議題仍尚未解決，因此我們於晚餐時繼續討論至九點多，於晚餐後，我再開車至奧蘭多住進旅館時已是凌晨了。

第二天中午應 University Central Florida 州立大學之邀，進行「國際電子元件學會」之傑出演講，由於此次演講正逢大學 Spring Break (春假期間)，我本來預期參與人員應十分少，然而演講時參與之學生卻高達 50 位左右，令我對 University Central Florida 之研究生及研究環境十分敬佩。而在演講結束後，研究生的問題及水準亦十分令人敬佩。這也是為何 University of Central Florida 於短短二十年之內，成長至美國第三大的大學之部分原因。於演講結束後，我亦參訪了其研究室及拜訪了一些教授，而於次日搭機返國，回到國內已是星期四晚上了。

III. Progress in Electromagnetic Research Symposium and Institute of Microelectronics, Chinese Academy of Science

此次至國外出差主要為參加於大陸西安所舉行的 Progress in Electromagnetic Research Symposium 「電磁研究進展研討會」。由於我的演講排在星期二，3/23，且北京中國科學院微電子所亦於前些日子邀請我於星期一，3/22 參加 The Prospective Studies of New Microelectronic Devices & Their Integration in Package Workshop 「微電子元件及積體化封裝演進研討會」，因此我順便安排了此二緊湊的演講行程。我於 3/21 星期日下午搭機前往北京，到達時已晚上 7 點。再搭車至旅館時，已經是晚上 8 時了。次日早上 8 點，「北京中科院微電子所」之秘書來旅館接我，並於 8:40 到達演講會場。研討會於 8:50 由葉所長致詞後開始，而我為第一位講者，並為與會人員報告了我們於 Low Power Electronic Devices「低功率電子元件」的研究。早上另外兩場演講分別為 Director Subramanian S. Iyer 及 Director Stuart P. Parkin, 分別為 IBM Systems & Technology Group 及 IBM Almaden Research Center 的處長。Director Iyer 報告了 IBM 的 Embedded Trench DRAM 於 Logic IC 的技術，而其技術較全球各半導體公司於此產品更為先進。Director Parkin 則報導了 IBM 之先進 Spin-Torque Magnetic RAM, 期望於未來能夠取代目前之快閃記憶體。Director Parkin 亦為 Stanford University 之合聘教授，目前亦指導 Stanford University 之研究生。上午三場演講結束時已 12 點，由於時間緊迫，中午用餐時「北京中科院微電子所」幾位研究人員向我們介紹，其所內有近三十位研究人員，許多均為美國 IBM, Intel, 歐洲 IMEC, 日本大公司返大陸之博士。而其中以 IBM 的研究員居多，這也是為何有 2 位 IBM 處長於研討會發表演說之故。本次研討會於下午五時結束，而我由於下午應邀至北京清華大學訪問，故於午餐後先行離開。至北京清華微電子所後，和其所長相互交換了意見，目前清華主要半導體的發展為「微機電元件」，他們自己有一 5 吋廠，為近十年前由 IBM 所贈送。然目前 5 吋晶圓之取得不易，因大多公司均為 4 吋、6 吋、8 吋、12 吋，這也造成了其發展的限制。北京清華雖亦為大陸微電子研究前 8 強之一，然而較有大量世界一流人才及經費的「北京中科院微電子所」而言，仍有待加強。我於晚餐後至西安，到達旅館時已經凌晨一點了。

次日即參加「電磁研究進展研討會」，我的演講安排於下午，而台灣參與此研討會的

同仁尚有台大林唯芳，清大周卓輝教授等。此研討會每半年於全世界輪流舉行，而值得一提的是其所出版之 PIERS 期刊， Impact factor 高達 4 以上，較 Applied Physics letters 及絕大多數 IEEE 期刊均為高。我於會議期間亦和 PIERS 總編相談，其 Impact factor 如此之高的原因，乃有許多理論電磁物理學者發表研究報告於此期刊，而總編為知名之前 University of Illinois 之教授，目前兼任「香港大學」院長。於研討會期間，我抽出半天時間拜訪了西安電子大學並發表演講，而西安電子大學亦為大陸前 8 大微電子重點大學。重要之電子發展乃於 GaN 及 SiC Power Devices & ICs 為世界著名。我於星期四下午搭機返台，結束此研討會行程。

IV. Materials Research Society

此次受邀至 Materials Research Society「材料學會」擔任 Session Chair 及 Tutorial 的任務，為國內極少受邀者。此期提升台灣的國際知名度。此次材料學會於美國加州 San Francisco (舊金山)舉行，由 4 月 5 日(星期一)至 4 月 9 日(星期五)為期一周，而我擔任 Session Chair 為星期一，且 Tutorial 為星期五，因此必須全程參與，然此行卻使我得到許多意外的收穫。此次赴美行程，我於 4 月 4 日(星期日)搭乘長榮航空的飛機赴美，到達美國時為下午 4 點，再乘捷運 BART 至舊金山市區的旅館，會場 Moscone West 及旅館離地鐵站較近，到旅館時不需提行李走很長的路，到達旅館時已下午 5 點多了。

次日早上即至「材料學會」報到，雖然我是首次參加此會議，然而仍是對所參與近千人的規模留下深刻的印象。此外，由於「材料學會」有許多研究是美國軍方所贊助，因此參與的廠商十分眾多，我於星期一早上先聽了熱門的 Solar Cells 太陽電池，然其中德國的廠商報告了近 20%的「能量轉換率」及保證 19%「能量轉換率」，令與會大眾十分震驚。因為如此高的「能量轉換率」已接近半導體太陽電池的理論極限 25%。其主要之重大改善，為使用 amorphous-Si 來覆蓋表面，以減少表面的能量損失，雖然過去此技術為 Sanyo 所發明並使用至量產，此乃其他設備廠商少數能達到如此高的「能量轉換率」，並保證量產成功至 19%以上。星期一下午即為我主持之 Non-volatile Memory Device Session，其中大會邀請了 Tower Semiconductor 之 Director 來演講過去十多年來，他們如何將[poly-Si]-Oxide-Nitride-Oxide-Si (SONOS) Charge-Trapping Flash (CTF) Memory，由構想至今奈米尺寸的量產。值得一提的是，當初的創始者為以色列的軍官，於以阿戰爭時受俘至阿拉伯國家的監獄中，閒來無事因此看起半導體元件方面的書，在獄中發現此 SONOS CTF 的重要，在三年後離開監獄後，開始於 National Semiconductor 研發此快閃記憶體，而後公司經變革改為 Tower Semiconductor，而公司於 2008 年與 Jazz Semiconductor、一家由 Aerospace & Defense industry 的 Rockwell Semiconductor 及 Conexant spun-off 的 fabless 公司、再度合併為 Tower Jazz 其發展過程只能用傳奇來表示。

而後第二、三、四天我聽了 Advanced CMOS Technology，目前 Ge MOSFET 主要為日本東京大學 Akira Toriumi 及 S. Takagi 所主導，其並有最高「電子遷移率」(mobility)

的紀錄。本次大會重點熱門的研發領域，除太陽電池外，尚有熱電(thermal electric)、非揮發性記憶體、生物工程等方面，而此能源、電子、生物領域，亦為美國政府、軍方、及民間大企業、美國 National Science Foundation 贊助的領域，因此均有派人參與演說，他們要求並鼓勵直接提計畫，而最熱門的領域，只在能源方面，而此目標型導向研發，值得國內借鏡。

我於星期五演說了過去所研發之 SONOS Charge-Trapping Flash 快閃記憶體，參與我的 tutorial 之人員對此研究十分有興趣，問了近 20 個問題，因此甚至於在休息時尚在討論，反應十分熱烈。與會同仁亦提及未來與歐盟合作的可能，而其中法國 CEA LETI 之 Deputy Director 即將於 4 月底來台並討論合作事宜，如果飛機可以飛不受火山灰的影響的話。於星期五下午結束後，我於星期六凌晨搭長榮航空返國，此次材料學會參與成果豐盛，未來有機會還會再次參加。