行政院國家科學委員會補助專題研究計畫 □ 成 果 報 告
■期中進度報告

三維積體電路(3D IC)關鍵技術之研究

計畫類別：■ 個別型計畫　　□ 整合型計畫
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計畫主持人：陳冠能
共同主持人：無
計畫參與人員：陳冠能及其指導之博碩士班學生

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中英文摘要：

隨著電晶體的縮小，摩爾定律的遵循已經到了極限點。3D IC 被視為最佳且最有潛力的解決方案，本計畫針對3D IC 鎖定其三種最關鍵的技術加以研究，包括銅晶圓接合(Cu wafer bonding)、TSV(Through-silicon via)的製程研究、薄化晶圓的關鍵技術。本年度成功的在接合技術上有所突破，除了讓晶圓表面有更好的粒子汙染容忍度外，讓矽完美且直接接合提供更高的via的密度和更好的對準，更發現混合接合可以為3DIC的可行方法。在via方面，將其應用在未被直接加熱的相變化開關，我們得到了絕佳的電子特性，而且也得到充分的證據via可以被重新可配置的邏輯應用所使用。此外在晶圓等級的蝕刻上，我們發現負光阻加上e-beam顯影的方式，會對蝕刻具有很強的抵抗力，這些研究及發現都被已發表成論文。

As integrated circuits (IC) is scaling down, Moore's Law gets its limitation. Three-dimensional integrated circuits (3D IC) are viewed as not only the best but the most potential approach. This research project proposal focuses on the research of key technologies of 3D IC, including Cu wafer bonding, TSV (through-silicon via) research, and wafer thinning. In this year, we conquer some difficulties in bonding technology. We make the success in better particle contamination tolerance on wafer surface and let silicon direct bonding provide high via density and better alignment. And we also find out that hybrid bonding can be the useful option for bonding. At the point of via, we can apply a programmable via in an indirectly heated phase-change switch. In addition, we obtain excellent electrical characterization and glean enough clues to demonstrate that via can apply for reconfigurable logic. Besides, we find that negative PR by e-beam development will have the large resistance in wafer level etching. These researches and findings had polished as international papers.

前言：

自1960 年代以來，經過數十年的發展，藉由縮小電晶體本身的體積與增加運算能力，晶片功能得以不斷的提升，這個晶片的進步基本上依循摩爾定律的預測。在不久的未來，由於微影技術及物理極限，縮小電晶體的發展將會遇到瓶頸。

除了半導體電晶體本身發展的極限外，另一方面，由於單一晶片上電晶體數目的持續增加及晶片複雜化所造成的總導線增加，決定晶片表現的關鍵已經由單一電晶體轉為總導線電阻電容延遲。雖然元件的某些區域可以透過電路設計與區塊的重組，來減少某些重要區域的傳遞距離，但是總導線的距離還是保持不變。因此，若要晶片的效能可以持續進步，有效的減低導線的總傳遞距離將是不可或缺的要求。

再者，隨著對晶片功能需求的不斷提升，往往需要特殊製程或是特殊材料的元件的加入，因此，異質元件的整合需求也越來越大，此類元件整合包括使用不同異質基板材料與在不同製程溫度製造元件。異質基板材料的整合，很明顯必須要靠新的方式才能將兩種元件整合；而對於不同製程溫度的元件，則後面製程的元件其製程溫度必須低於已製程完畢元件的熱允許溫度，此將限制許多元件的應用，如矽波導元件與傳統CMOS 的整合。

為了解決上述的挑戰與需求，遂有3D 整合(3D Integration)與三維積體電路(3D IC)概念的出現。3D IC 技術的概念基本上是改變傳統將元件放置在二維XY 平面晶片上的方式，增加第三維也就是直立堆疊的空間(Z 軸)。也因為如此，使用3D 技術可以避免傳統二維電子晶片或元件繼續發展下去所擁有的問題，譬如：總導線過長或晶片面積太大而無法達到輕薄短小的需求。

3D IC 技術是指利用晶圓接合(wafer bonding)或是晶片堆疊(chip stacking)，利用through-silicon via (TSV)連接已薄化的晶圓或是晶片，因此可將傳統的二維積體電路晶片轉變成三維積體電路晶片。也由於3D IC 能有效地利用空間及縮短電流信號所傳輸的距離，故可減低電阻電容延遲及總電阻值。再者，由於利用晶圓接合或是晶片堆疊的特殊概念，因此異質基板材料的元件可以分別製作再行堆疊，而如前所述有製程溫度或其他環境限制的不同元件，也可藉堆疊的方式加以解決。因此3D IC 技術能在輕薄短小與價格的要求下提供多功能異質整合、高效能(high performance)與低功耗(low power dissipation)等許多優點。

由於未來邏輯晶片、記憶體產品與其他電子產品均朝向高密度、高速與高頻寬的方向發展、另外通訊與光電產業將以維型模組為發展目標、加上微機電產業與藍芽科技的市場、最後生技產業對生醫晶片的需求，由此可知異質晶片的整合方式將是未來發展趨勢，更可說明3D IC 技術之前景與重要性。

而3D IC 的特殊概念，此科技將會顛覆傳統的二維積體電路，也因此牽涉的領域包括設計、製程技術與設備、封裝測試方式及終端產品應用及表現，這些領域均缺一不可，也同時息息相關，並將決定3D IC 的成熟度與最終產品。換句話說，3D IC 事實上乃為一個整合上中下游領域的一個全新科技。而在這些領域中，尤其以關鍵的3DIC 製程技術為最重要的決定因素。

研究目的：

本研究計畫之目的為建立台灣學術界的3D IC 關鍵技術(bonding technology、TSV、晶圓薄化)的研究實力與科學知識，以國外學術界（如MIT 與RPI）發展3D IC 的關鍵技術大約近十年，雖然經驗較豐富。但缺乏工業界的奧援、故只能發展單一技術。而國外產業研究（如IBM 與IMEC），發展3D IC 的關鍵技術均是以產品需求為優先考量，而且缺乏基礎科學的，加上無法與其他公司合作，故資訊封閉且常常需重頭開始探索。目前台灣對3D IC 仍屬起步階段，除了少數半導體廠如台積電與日月光有初步的研究外，其他研究單位或是學術機構皆屬剛起步階段，以學術單位而言均是以3DIC 設計與EDA為研究主題，並無關鍵技術的研究。

然而3D IC 當前最重要的就是要關鍵技術的成熟，藉此提供3D IC 製程與模式的選項，才能帶動3D IC 設計，並達成3D IC 的產品製作。當前最重要的，就是需要有專業3D IC經驗的人在台灣從事研究，同時透過學術交流與機構合作方式的機會，慢慢的將3D IC 的種子灑出並與台灣產業界合作，藉此厚植台灣3D IC 的實力。

此外，以個人在3DIC近十年的努力及耕耘，再加上對 3DIC先進製程技術的深刻了解，從3DIC基本但卻最重要的技術開始著手，也就是銅晶圓接合，銅是現在半導體產業中的熱門金屬，也是3DIC領域中大家所熱切希望使用的接合材料，期望研究出最佳可靠度與最佳強度(包括與其他材料的異質整合)的元件結構，銅晶圓接合也是個人在IBM時主攻的項目，期待能將所學及所長發揮，讓銅晶圓接合技術能和美國居於領先的研究中心並駕齊驅，甚至拿下這項技術的領先位置，

而TSV及晶圓薄化(wafer thinning)在整個3DIC發展中相對處於發展較晚的階段，但其製程的技術卻是極為關鍵的，而本計畫想利用這個機會將整個TSV及薄化晶圓的藍圖、模型、參數等等基礎建立起來，讓這些製程條件及技術成為3DIC的標準範本。最後利用薄化晶圓的發展將銅晶圓接合與TSV 整合，以達到對3D IC 關鍵技術的充分研究與製程能力，以期在這次半導體革命中能再度佔有領先地位，這也是本研究計畫之主要目的。

研究方法：

銅晶圓接合：

本年度計畫主要內容為銅晶圓接合之物理特性與材料分析研究，預計需時兩年時間，目前雖然已有銅晶圓接合之基本研究，但是，科學界對於其詳細的物理特性如晶粒生成及材料分析仍有許多不明瞭之處，將以現有的晶圓接合參數進行晶圓接合，然後進行物理特性與材料分析的研究，重點在於建立銅晶圓接合的參數地圖，並測試最佳的參數。

此外，目前雖然已有銅晶圓接合之基本研究，但是大部分的結果都是銅膜接合，科學界對於如何製作最佳pattern的銅以供接合所知仍有限，將採用的方法各種不同的方法包括CMP(化學機械研磨法)進行研究，以製作出不同形狀的銅pattern 已進行接合，然後利用切割的方式測試接合強度，本年度主要的重點在於建立銅pattern 製程的參數地圖，並測試最佳的參數。

由於科學界對於銅晶圓接合仍缺乏系統性的研究，對於與元件的整合更是缺少，本年度將以進行一連串的銅晶圓接合整合，從設計、製程到測試與分析都將包括在內，本年度主要的重點在於建立銅晶圓接合之製程整合。

TSV：

本年度的重點在於TSV之蝕刻製程研究，將使用DRIE的機台，配合參數的調整進行物理性質的研究，已達到了解並掌握TSV 蝕刻的目的，並建立TSV蝕刻製程的參數地圖，測試最佳的參數。

此外，還要研究TSV之材料填充與應力所產生的結果，研究方法將以取得TSV 蝕刻試片後，然後使用不同材料加以填充，並發展出最佳填充與最低應力的材料，本年度主要的重點在於建立不同材料的TSV 填充能力，並且確定填充的均勻性。

目前雖然已有TSV(Through-silicon Via)之基本研究，但是，科學界對於TSV 仍缺乏系統性的研究，對於與元件的整合更是缺少，本研究採用的方法將以進行一連串的TSV 製程整合，從設計、製程到測試與分析都將包括在內，本年度主要的重點在於建立TSV 之製程整合。

薄化晶圓：

目前國際上薄化晶圓研究大部分均屬產業應用，學術研究還屬稀少，本年度主要內容為薄化晶圓之研究與特性分析，研究方法將以使用各種薄化晶圓方式來進行晶圓本身研究與特性分析，第一年主要的重點在於建立晶圓薄化的製程與可靠度能力。

結果與討論：

在接合技術上的突破：在晶圓表面有更好的粒子汙染容忍度。然而，這種技術在設備和製造工具上，還是有潛在污染問題。金屬擴散和共晶接合提供直接的連結，但是有空氣間隙的未接合區域會導致可靠度問題。矽直接接合提供更高的 via 的密度和更好的對準，但是乾淨的表面和接合環境的要求是非常重要的。 混合接合，結合金屬和附著劑或者氧化物接合，在封裝的電路上，同時能達到穩定且增強的黏著性。高產出量和可靠性優勢，混合接合成為了 3DIC 的一種可行方法。

在Via方面，可以應用在未被直接加熱的相開關，除了絕佳的電子特性外，元件的操作可以被應用在標準的CMOS的製程科技上，並且元件可以包含多種的操作模式。所以，這個結構可以被重新可配置的邏輯應用所使用。最終好的實驗数据會與模擬結果，證明此設備應用的可行性。

在筒形的結構上:晶圓等級上，用負光阻加上 e-beam 顯影的方式，對蝕刻具有很強的抵抗力。處理的順序和筒形的結構形成可能機制在附件中被詳細的論述。此外，在半導體的先進製程中，此筒形的結構將有極大的機會被應用及提倡
。

計畫成果自評：

經過實驗團隊一年來的合作與努力，各項研究已有相當進展，成果如下：

(1) 銅晶圓接合

a. 解決包括如何精確觀察銅晶圓接合時兩銅膜之介面的晶粒成長與生成。

b. 解決如何控制不同的晶圓接合參數以供觀察與分析。

c. 解決如何精確控制在銅製程參數下，可以得到最佳高度的銅 pattern。

d. 解決如何精確控制在銅製程參數下，可以得到最佳形狀的銅 pattern。此計畫成果發表於以下列出之國際會議論文[3]

e. 解決完整考慮不同銅接合參數與製程整合的關係。

f. 將在低溫下銅晶圓接合及混和接合(銅與介電質材料)製程技術應用於三維積體電路，此計畫成果發表於以下列出之國際會議論文[9] 。

(2) TSV

a. 在機台內控制參數及達到 TSV 在不同晶圓與不同位置的均勻性。

b. 了解如何觀察 TSV 的實際蝕刻深度。

c. 了解如何觀察 TSV 的實際填充深度。

d. 了解如何將具相變化的材料填充應用在可控之程序化 TSV 製程，並將其與 CMOS 元件做相當程度的整合，此計畫成果發表於以下列出之國際期刊論文[3] 。

(3) 薄化晶圓

a. 了解如何控制晶圓薄化後的最後厚度。

b. 了解在薄化晶圓的過程中因太過薄化而造成晶圓呈彎曲弓狀所帶來的變化及晶圓接合技術上的影響，此計畫成果發表於以下列出之國際會議論文[4] 。

在致力於建立銅晶圓接合、TSV 及薄化晶圓製程整合的過程中，仍有部分成果未達完善，如: 薄化晶圓的可靠度能力、研究 TSV 之材料填充與應力所產生的結果，對於發展出最佳填充性及最低應力的材料並達成填充得均勻性皆尚在實驗階段，然而目前已能掌握 TSV 的蝕刻及填充深度且使用具相變化的材料填充以達到與 CMOS 元件的整合。而混和接合中使用高分子材料與銅金屬的方式更是能進階得提高晶圓級接合技術的發展及可靠度能力(發表之國際會議論文[1])，另外對於架構出奈米級銅接合 pad 的技術能提升在元件內訊號傳輸的速率(發表之國際會議論文[6]) ，此成果能達到輕薄短小及高效能的應用要求，總括上述成果對於 3D IC 關鍵技術的發展有階段性的提升並為台灣的半導體業跨出重要的一步。

已發表論文:

本計畫實驗成果豐碩，目前已有三篇國際期刊論文已發表或即將刊出，四篇論文審查中，另外有 12 篇的國際會議論文已發表或被接受。此外，由於研究成果傑出，這些論文中包括一篇邀請論文及三篇邀請演講。

發表論文總表:

已發表或接受之國際期刊論文

1. **Kuan-Neng Chen,** and John C. Arnold, "Wafer-level Self-aligned Nano Tubular Structures and Templates for Device Applications", *Journal of Nanoscience and Nanotechnology,* 10, pp. 1-6, 2010.
2. ***[Invited]*** Cheng-Ta Ko and **Kuan-Neng Chen**, "Wafer Level Bonding/Stacking Technology for 3D Integration", *Microelectronics Reliability*, 50 (4), pp. 481-488, 2010.
3. **Kuan-Neng Chen,** and Lia Krusin-Elbaum, "The fabrication of a programmable via using phase-change material in CMOS-compatible technology", *Nanotechnology*, 21 (13), 134001, 2010.

審查中之國際期刊論文

4. **K.N. Chen,** Y. Zhu, W.W. Wu, and R. Reif, "Investigation and Effects of Wafer Bow in 3D Integration Bonding Schemes", submit to *Journal of Electronic Materials*.
5. Cheng-Ta Ko, **Kuan-Neng Chen,** Zhi-Cheng, Hsiao, Huan-Chun Fu, and Wei-Chung Lo, "Polymers Investigation for 3D IC Bonding Technology", submit to *Journal of Electronic Materials*.
6. **Kuan-Neng Chen,** Chung Seng Tan, "Integration Schemes and Enabling Technologies for Three-Dimensional Integrated Circuits (3D IC)", submit to *IET Computers and Digital Techniques.*
7. **K. N. Chen,** C. K. Tsang, W. W. Wu, S. H. Lee, and J. Q. Lu, "Fabrication of Nano-Scale Cu Bond Pads with Seal Design in 3D Integration Applications", submit to *Journal of Nanoscience and Nanotechnology*.

已發表或被接受之國際會議論文

1. Cheng-Ta Ko, Zhi-Cheng Hsiao, Huan-Chun Fu, **Kuan-Neng Chen,** Wei-Chung Lo, and Yu-Hua Chen, "Wafer-to-Wafer Hybrid Bonding Technology for 3D IC", ESTC, Berlin, Germany, Sep. 13-16, 2010.

2. **Kuan-Neng Chen,** Ming-Fang Lai, and Hung-Ming Chen, "Wafer-Level Three-Dimensional Integrated Circuits (3D IC): Schemes and Key Technologies", IUMRS-ICEM, Seoul, Korea, Aug. 22-27, 2010.

3. **K. N. Chen,** C. Cabral, Jr., S. H. Lee, P. S. Andry, and J. Q. Lu, "Investigations of Cu Bond Structures and Demonstration of a Wafer-Level 3D Integration Scheme with W TSVs", International Symposium on VLSI Technology, Systems and Applications (2010 VLSI-TSA), Hsinchu, Taiwan, Apr. 26-28, 2010.

4. **K. N. Chen,** Y. Zhu, W.W. Wu, and R. Reif, "Investigation and Effects of Wafer Bow in Different 3D Stacking Schemes", 2010 TMS Conference, Seattle, WA, Feb 14-18, 2010.
5. Cheng-Ta Ko, Wei-Chung Lo, **Kuan-Neng Chen,** Huan-Chun Fu, Zhi-Cheng, Hsiao, and Yu-Hua Chen "Polymers Investigation for 3D IC Stacking Technology", 2010 TMS Conference, Seattle, WA, Feb 14-18, 2010.
6. **K. N. Chen*,*** Y. Zhu, W. W. Wu, C. K. Tsang, S. H. Lee, and J. Q. Lu, "Fabrication of Nano-Scale Cu Bond Pads with Seal Design in 3D Integration Applications", IEEE International NanoElectronics Conference (INEC) 2010, Hong Kong, Jan 3-8, 2010.
7. **K.N. Chen,** Y. Zhu, W.W. Wu, and R. Reif, "Copper Thin Film Research and Development for Wafer Bonding", TACT 2009 International Thin Films Conference, Taipei Taiwan, Dec 14-16, 2009.
8. ***[Invited]*** **Kuan-Neng Chen**, "Wafer-Level Alignment Technology for 3D Integration", The 4th IMPACT 2009 Conference and International 3D IC Conference, Taipei, Taiwan, Oct. 21-23, 2009.
9. ***[Invited]*** Chuan Seng Tan and **Kuan-Neng Chen**, "Low Temperature Cu-Cu Bonding and Hybrid Cu/Dielectric Bonding: An Enabling Technology for 3-D ICs Application", The 4th IMPACT 2009 Conference and International 3D IC Conference, Taipei, Taiwan, Oct. 21-23, 2009.
10. ***[Invited]*** **Kuan-Neng Chen**, "Wafer-Level Copper Bonding Technology in 3D ICs", 216th ECS Meeting, Oct. 4-9, 2009.
11. **K.N. Chen** and L. Krusin-Elbaum, "CMOS-Technology Compatible Programmable Via using Phase-Change Materials", 2009 Nano and Giga Challenges in Electronics, Photonics and Renewable Energy, Hamilton, Ontario, Canada, Aug 10-14, 2009.
12. **K.N. Chen,** E.A. Joseph, J.C. Arnold, and N. Ruiz, "Fabrication of robust self-aligned nano-scale tubular structures and templates for device applications", 2009 Nano and Giga Challenges in Electronics, Photonics and Renewable Energy, Hamilton, Ontario, Canada, Aug 10-14, 2009.

出席國際學術會議心得報告

計畫編號	NSC 98-2218-E-009 -013 -MY2
計畫名稱	三維積體電路(3D IC)關鍵技術之研究
出國人員姓名 服務機關及職稱	陳冠能 國立交通大學電子工程學系副教授
會議時間地點	10-14 Aug 2009, Hamilton, ON, Canada (Toronto area)
會議名稱	Nano and Giga Challenges in Electronics, Photonics and Renewable Energy
發表論文題目	1. CMOS-Technology Compatible Programmable Via using Phase-Change Materials 2. Fabrication of robust self-aligned nano-scale tubular structures and templates for device applications

一、　參加會議經過

(1) 為拓展國際視野，及將研究成果發表於世界，個人此次參加此項於加拿大多倫多近郊所舉辦的國際學術會議。

(2) 此次大會邀請到數十位 Invited Speakers，他們均為國際知名科學家及研究學者，尤其是個人所聆聽的 Phaedon Avouris，更是國際間的知名人士，講題為"Carbon Based Electronics and Optoelectronics"。

(3) 本人此次會議共計兩項論文，均為 poster session，除了於會議期間時展示，並在八月十三日下午六點至九點為討論時間，接受參加會議的人員發表問題及討論。

二、　與會心得

(1) 本次的會議同時與加拿大 2009 半導體會議一起舉辦，因此參加的人數眾多，同時有許多知名的國際學者應邀演講。

(2) 以個人所聆聽的 Phaedon Avouris，他除了是許多重量級機構的院士外，在碳奈米管(Carbon Nanotubes)的研究領域，更是世界級的知名人士，所做的研究均是最前瞻的領域，也因此他的演講吸引了許多人士的參與及發問。

(3) 個人本次的兩個研究主題，一為相變化材料在邏輯元件上的研究，另一為可自行對準的奈米及管狀物組織及元件應用，經大會審核後在本次會議上發表，發表的形式為海報展覽，這兩項研究均是個人與美國 IBM 華生研究中心執行國際合作之共同成果，此項國際合作計畫為有關三維積體電路之研究。

(4) 因為這兩項研究成果均為原創性質，同時也因為與知名的國際級研究單位合作，研究成果展出期間，受到為數不少的與會人士注目，同時就研究成果與個人進行廣泛的討論。並有單位希望將來與個人進一步進行共同合作。

(5) 本次會議成果豐碩，除了兩項研究成果的順利發表，聆聽不少最新的研究成果，同時亦帶回會議論文集與 CD，並與國際間相同領域的人士進行學術交流，可謂不虛此行。

出席國際學術會議心得報告

計畫編號	NSC 98-2218-E-009 -013 -MY2
計畫名稱	三維積體電路(3D IC)關鍵技術之研究
出國人員姓名 服務機關及職稱	陳冠能 國立交通大學電子工程學系副教授
會議時間地點	4-9 Oct 2009, Vienna, Austria
會議名稱	216th ECS Meeting
發表論文題目	Wafer-Level Copper Bonding Technology in 3D ICs

一、　參加會議經過

(1) 為拓展國際視野，及將研究成果發表於世界，個人此次參加此項於奧地利維也納所舉辦的國際學術會議。於十月四日搭乘長榮客機經曼谷轉機於五日早上抵達維也納國際機場。

(2) ECS Meeting 在微電子與材料方面是一個相當重要的國際會議，同時也是電化學領域最重要的國際會議。

(3) 參加其間亦有許多台灣學界人士參加，個人在會場交談的即包括交通大學荊鳳德教授、呂志鵬教授與吳文偉教授，清華大學歐陽浩教授，及來自台灣大學與中興大學的教授們。

(4) ECS 大會這次著眼於三維積體電路在半導體領域的積極發展，特地籌畫” Processing, Materials, and Integration of Damascene and 3D Interconnects” ，在三維積體電路的部分，十三篇口頭報告中就有七篇是受邀報告，本人有幸名列其中。

二、　與會心得

(1) 本次的會議同時與 EuroCVD 17 與 SOFC XI-11th International Symposium on Solid Oxide Fuel Cells 一起舉辦，因此參加的人數眾多，同時有許多知名的國際學者應邀演講。

(2) 個人本次所參加的研討會，是有關三維積體電路方面的研究。受邀或最後接受的論文皆是在三維積體電路界素有名聲的專家及機構，如 IMEC、Fraunhofer IZM 與 Semitool。以受邀單位為例，共有七篇受邀論文，其中有四篇為歐美學術研究單位、一篇為公司、兩篇為大學，個人的論文就是這兩篇大學論文中的其中一篇。

(3) 因為個人在此三維積體電路的方面已經研究快十年，故大會在籌辦此次會議時，在數個月前就積極邀請個人參加演講。個人基於與國際方面多交流的原則，同時也希望增加台灣與交通大學在三維積體電路界的知名度，遂同意此項邀請，並以台灣國立交通大學的名義在大會發表專題演講。

(4) 個人本次發表論文的題目為: Wafer-Level Copper Bonding Technology in 3D ICs，乃是有關於晶圓級銅接合技術在三維積體電路上的應用，因為這研究成果相當重要，為三維積體電路發展所需要必備技術，同時也因為與知名的國際級研究單位合作，研究成果發表期間與之後，受到為數不少的與會人士注目，同時就研究成果與個人

進行廣泛的討論。並有單位希望將來與個人進一步進行共同合作。

(5) 本次會議成果豐碩，除了研究成果的順利發表，聆聽不少最新的研究成果，同時亦帶回會議論文集與 CD，並與國際間相同領域的人士進行學術交流，可謂不虛此行。

(6) 最後附上個人與歐陽浩教授及吳文偉教授在會場的合照。

出席國際學術會議心得報告

計畫編號	NSC 98-2218-E-009 -013 -MY2
計畫名稱	三維積體電路(3D IC)關鍵技術之研究
出國人員姓名 服務機關及職稱	陳冠能 國立交通大學電子工程學系副教授
會議時間地點	14-18 Feb 2009, Seattle, USA
會議名稱	2010 TMS Meeting
發表論文題目	1. Investigation and Effects of Wafer Bow in Different 3D Stacking Schemes 2. Polymers Investigation for 3D IC Stacking Technology

一、 參加會議經過

(1) 為拓展國際視野，及將研究成果發表於世界，個人此次參加此項於美國西雅圖所舉辦的國際學術會議。於二月十二日搭乘長榮客機經於十三日晚上抵達西雅圖國際機場。

(2) TMS Meeting 在微電子與材料方面是一個相當重要的國際會議，同時也是材料界領域最重要的國際會議。

(3) 參加其間亦有許多台灣學界人士參加，個人在會場交談的即包括台灣大學高振宏教授、清華大學陳信文教授、成功大學林光隆教授與東華大學宋振銘教授，及來自中央大學與中興大學的教授們。

(4) TMS 大會這次著眼於三維積體電路在半導體領域的積極發展，特地在 Lead-Free Solder Technology Workshop 增加在三維積體電路的部分，本人有幸名列其中兩篇。

二、 與會心得

(5) 本次的會議參加的人數眾多，同時有許多知名的國際學者應邀演講，如台灣知名的中研院院士杜經寧教授。

(6) 個人本次所參加的研討會，是有關先進封裝製程方面的研究。受邀或最後接受的論文皆是在先進封裝業界素有名聲的專家及機構，如 UCLA、TI 與 Samsung。

(7) 因為個人在此三維積體電路的方面已經研究快十年，故大會在籌辦此次會議時，因為重點項目包括此項研究領域，個人基於與國際方面多交流的原則，同時也希望增加台灣與交通大學在三維積體電路與先進封裝界的知名度，遂決定投稿，並以台灣國立交通大學的名義在大會發表專題演講。

(8) 個人本次發表論文有兩篇，第一篇是有關於 wafer bow 在晶圓級接合技術的影響與在三維積體電路上的應用，第二篇則是高分子與金屬異質晶圓接合的研究，因為這些研究成果相當重要，為三維積體電路發展所需要必備技術，同時也因為與知名的國際級研究單位合作，研究成果發表期間與之後，受到為數不少的與會人士注目，同時就研究成果與個人進行廣泛的討論。並有單位希望將來與個人進一步進行共同合作。

(9) 本次會議成果豐碩，除了研究成果的順利發表，聆聽不少最新的研究成果，同時亦帶回會議論文集與 CD，並與國際間相同領域的人士進行學術交流，可謂不虛此行。

(10) 最後附上個人與宋振銘教授在會場的合照。

國際合作國際研究學術心得報告

計畫編號	NSC 98-2218-E-009 -013 -MY2
計畫名稱	三維積體電路(3D IC)關鍵技術之研究
出國人員姓名 服務機關及職稱	陳冠能 國立交通大學電子工程學系副教授
國際合作時間地點	1-9 Aug 2009 and 16-24 Aug 2009 New York, USA
國際合作機構名稱	IBM TJ Watson Research Center
國際合作主要負責人	Dr. Steven J Koester

一、 國際合作機構之簡介

本計畫進行國際合作研究的單位為美國IBM的華生研究中心，美國IBM華生研究中心為享譽全球極富盛名的研究單位，目前有多位諾貝爾獎得主、美國國家科學院或是工程院院士、與台灣中央研究院院士，目前台灣有不少電子業的傑出人才亦是出自此單位。本中心已在半導體與電子元件上研究建立起相當堅強的實力。

二、 本合作機構在此研究領域之背景

美國IBM公司大約在本世紀初期開始投入3D IC的研究，靠者堅強的研究團隊(Watson Research Center)及半導體製程中心(Fishkill, NY and Albany, NY)的支援，已經有一些初步成果，同時IBM有完整的無塵室製程線與必要的3D IC所需製程設備，在本計畫的初短期或是重要的儀器現階段台灣無法提供者，均可透過IBM華生研究中心提供幫助。

三、 本國際合作研究模式

本國際合作計畫雙方並無相對義務，故可以共同發表論文即進行研究。合作模式為雙方各自發展技術及研究，但若有任何需要IBM的協助與合作，則可透過討論來執行，故台灣人員前往IBM旅費及生活費部分要由台灣負擔，但是使用的儀器無須額外付費，結果則共同發表。

四、 本次國際合作國際研究進展與心得

(1) 如本國科會計畫內所提，此項研究計畫有一部份需透過國際合作及國際研究來完成。此國際合作的細部內容，包括如何進行合作、選定哪些研究領域及範圍，還有一些初期研究計畫的執行，均須在IBM華生研究中心面對面進行討論及親自進行研究，因此個人利用暑假期間出國開會與無授課壓力的機會，親自前往IBM華生研究中心進行國際合作之國際研究。

(2) 本國際合作計畫於IBM華生研究中心之主要負責人為Exploratory Group的經理Dr. Steven Koester,合作的意願並經過資深經理Dr. Wilfried Haensch、處長Dr. Ghvam Shahidi、與資深副總裁陳自強博士(Dr. TC Chen)的支持。

(3) 到達IBM華生研究中心之後，先後與Dr. TC Chen 、 Dr. Steven Koester 、 Dr. John Knickerbocker 、 Dr. Eric Joseph 、 Dr. Fei Liu 、 Dr. Bing Dang、Dr. Yu-Ming Lin 與Dr.Yu Zhu 進行晤談，晤談的內容包括合作的項目細節，及合作的模式之再度確認，同時也著手安排一些可以馬上進行的研究項目。整體而言，IBM華生研究中心的人員相當歡迎此項國際

合作計畫，更希望透過這兩年的國際研究，雙方能夠在三維積體電路的領域上共同發表令人振奮的研究成果。

(4) 在確認本次國際合作的研究時程與細部項目之後，個人與華生研究中心的團隊即開始進行實際的研究，在回國前，目前已執行了以下的研究項目:

1. 銅晶圓接合的文獻調查與研究目標
2. 制定共同研究計畫
3. 制定研究時程與細部項目
4. 銅膜晶圓接合的製程
5. 銅晶圓接合的最佳化
6. 銅Pad的晶圓接合
7. 銅 Pad 如何製程最佳化以達到最佳接合效果
8. 銅晶圓接合的機械測試
9. 銅晶圓接合的材料分析

(5) 上述的某些研究成果，如第七項的"銅 Pad 如何製程最佳化以達到最佳接合效果"，在本次國際合作研究期間，已經有令人滿意的研究成果，因此，雙方已決定將共同撰寫會議論文與投稿國際學術期刊，以在國際間發表。

(6) 此外，在共同研究製造元件的過程中，雙方也發現某些特殊製程可以製造出高強度且自我對準的奈米級管狀物，可進一步用於元件製程及應用。雙方亦已決定將共同撰寫會議論文與投稿國際學術期刊，以在國際間發表。

(7) 其餘的研究項目，在本次的國際合作研究中，均有良好的初步結果，接下來雙方將各自進行研究，同時透過電郵與網路視訊充分進行溝通，定期開會，以達到持續合作的目標，預計於明天夏天將繼續進行第二年的國際合作計畫。

五、 結論

本次的國際合作研究計畫，達到令人滿意的效果，雙方人員對於如何執行此項合作，均有高度的共識。在本次的實際執行研究上，也達到了許多研究成果，並預期會有國際期刊的發表。

最後，透過與國際知名機構的合作，使用其先進的儀器設備，更對此國科會研究的成功，有著高度的影響力。預期在第二年的國際合作，將會有更多的研究成果產出。

六、國際合作所衍生的論文成果:

已發表或接受之國際期刊論文

1. **Kuan-Neng Chen,** and John C. Arnold, "Wafer-level Self-aligned Nano Tubular Structures and Templates for Device Applications", *Journal of Nanoscience and Nanotechnology,* 10, pp. 1-6, 2010.

2. **Kuan-Neng Chen,** and Lia Krusin-Elbaum, "The fabrication of a programmable via using phase-change material in CMOS-compatible technology", *Nanotechnology*, 21 (13), 134001, 2010.

審查中之國際期刊論文

3. **K.N. Chen,** Y. Zhu, W.W. Wu, and R. Reif, "Investigation and Effects of Wafer Bow in 3D Integration Bonding Schemes", submit to *Journal of Electronic Materials*.
4. **Kuan-Neng Chen,** Chung Seng Tan, "Integration Schemes and Enabling Technologies for Three-Dimensional Integrated Circuits (3D IC)", submit to *IET Computers and Digital Techniques.*
5. **K. N. Chen,** C. K. Tsang, W. W. Wu, S. H. Lee, and J. Q. Lu, "Fabrication of Nano-Scale Cu Bond Pads with Seal Design in 3D Integration Applications", submit to *Journal of Nanoscience and Nanotechnology*.

已發表或被接受之國際會議論文

1. **K. N. Chen,** C. Cabral, Jr., S. H. Lee, P. S. Andry, and J. Q. Lu, "Investigations of Cu Bond Structures and Demonstration of a Wafer-Level 3D Integration Scheme with W TSVs", International Symposium on VLSI Technology, Systems and Applications (2010 VLSI-TSA), Hsinchu, Taiwan, Apr. 26-28, 2010.
2. **K. N. Chen,** Y. Zhu, W.W. Wu, and R. Reif, "Investigation and Effects of Wafer Bow in Different 3D Stacking Schemes", 2010 TMS Conference, Seattle, WA, Feb 14-18, 2010.
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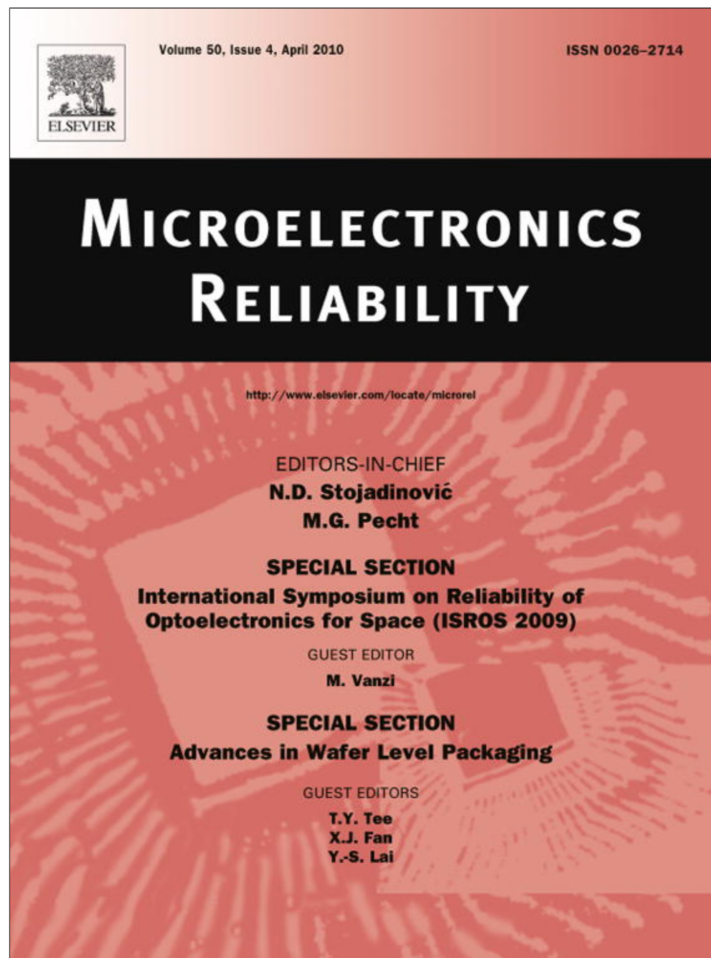

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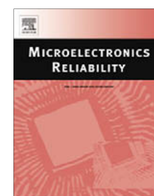

Wafer-level bonding/stacking technology for 3D integration

Cheng-Ta Ko, Kuan-Neng Chen *

Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan

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ABSTRACT

Enhanced transmission speeds, lower power consumption, better performance, and smaller form factors are reported as advantages in many devices and applications when using 3D integration. One core technique for performing 3D interconnection is stacked bonding. In this paper, wafer-level bonding technologies are reviewed and described in detail, including bonding materials and bonding conditions. The corresponding 3D integration technologies and platforms developed world-wide are also organized and addressed.

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1. Introduction

Three-dimensional integrated circuits (3D IC) has been generally acknowledged as the next generation semiconductor technology with the advantages of small form factor, high-performance, low power consumption, and high density integration [1–3]. Through silicon via (TSV) and stacked bonding are the core technologies to perform vertical interconnect for 3D integration. For the fabrication approach, there are three stacking schemes in 3D integration: chip-to-chip, chip-to-wafer, and wafer-to-wafer. Wafer-to-wafer technology can be applied for homogeneous integration of high yielding devices. Wafer-to-wafer bonding maximizes the throughput, simplifies the process flow, and minimizes cost. The drawback for this wafer-to-wafer method is the number of known-good-die (KGD) combinations in the stacked wafers will not be maximized when the device wafer yields are not high enough or not stable. In this case, chip-to-chip or chip-to-wafer will be adopted to ensure vertical integration with only good dies. Considering mass production in future, the chip-to-wafer and wafer-to-wafer technologies have gradually become the mainstream for 3D integration.

Wafer-level bonding/stacking technologies can be further differentiated by the method used to create TSVs: either via-first or via-last. The common definition for via-first and via-last is based on TSVs formed before and after BEOL process. TSV fabrication after the wafers are bonded, using a "drill and fill" sequence, is definitely via-last approach. Whereas via-first and pre-bonding via-last approaches, build TSVs on each wafer prior to the bonding process, are generally more efficient and cost-effective. The leading wafer-level bonding techniques used in 3D integration include adhesive bonding (polymer bonding), metal diffusion bonding, eutectic bonding, and silicon direct bonding. Additionally, one emerging approach with high yield and high reliability is hybrid bonding technology. In this review paper, these wafer-level bonding techniques are introduced in detail. Corresponding 3D integration schemes using these bonding technologies and platforms developed in companies or research institutes are also reviewed.

2. Adhesive/polymer bonding

Adhesive bonding is a low temperature and patternable technique suitable for 3D IC, MEMS, VLSI packaging, and microsensor packaging. In 3D IC integration scheme, adhesive material can be used for wafer-to-wafer bonding followed by fabrication of TSV on proper position to form vertical interconnection between stacked wafers. The advantages of this bonding technology include low bonding temperature with required bonding strength, no metal ion contamination to device, excellent surface planarization property, and high plasticity to absorb the stress induced during bonding process.

In this bonding scheme, however, because TSV is fabricated after bonding, the higher aspect ratio increases the process challenge and cost especially for small via size. In addition, the high shrinkage characteristic of polymer materials decreases the bonding accuracy, which also limits its application. Therefore, adhesive bonding is usually adopted on wafer bonding with lower accuracy requirement, or collocated with other bonding methods to be an auxiliary to increase the bonding strength. The potential contamination of adhesive materials on devices and fabrication tools during process is a significant concern for the manufacturing line. As for the selection of adhesive material, in addition to the basic requirements such as excellent adhesion, low residual stress, a high thermal and chemical resistance is also the requirement to endure the follow-up processes.

Based on the application, the adhesive materials can be divided into photosensitive and non-photosensitive types. The photosensitive materials are usually used as photoresist model to define the

* Corresponding author.
E-mail address: knchen@mail.nctu.edu.tw (K.-N. Chen).

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patterns. The non-photo ones are generally adopted for the passivation layer to protect circuits, or used to be the build-up layer. The bonding strengths of four different patternable materials (SU-8 from MicroChem Co., AZ-4620 from Shipley, SP-341 from Torray Co., and JSR-137N from Japan Synthesis Rubber Co.) have been thoroughly investigated by Pan et al. [4] with respect to bonding temperature and bonding force dependence. The bonding strength between identical materials exhibits the same behavior for all four materials. Fig. 1 shows the relationship between bonding strength and bonding temperature, which indicates the SU-8 has the maximum bonding strength of 20.6 MPa among the four materials, whereas the other three are all about 10 MPa. Other polymer materials such as benzocyclobutene (BCB) (Dow chemical), Polyimide (DuPont), Parylene, and several photoresists are also evaluated and compared [5,6]. The results illustrate the BCB has the highest bonding strength (>20 MPa) with very small void formation. Currently, BCB and SU-8 are the most common materials used for wafer-level adhesive bonding in 3D integration and applications.

As aforementioned, BCB is one of the adhesive wafer bonding materials that have been researched extensively for 3D IC platforms because of its outstanding wafer bonding capabilities, thermal resistance, bonding strength, chemical resistance, and wide acceptance in IC manufacturing environments. Researchers from RPI use CMOS silicon on insulator (SOI) wafers and BCB as the dielectric to develop 3D integration platforms by adhesive wafer bonding [7,8]. Fig. 2 shows a schematic 3D IC structure of RPI approach [7]. In this 3D integration platform, the pre-processed IC wafers are aligned and bonded with BCB adhesive by face-to-face wafer bonding scheme. One of the bonded wafers is thinned to an etch-stop layer, the buried oxide layer (BOX) in SOI wafer. Subsequently, vias are etched in the wafer stack, followed by the inter-wafer interconnects formation using Cu/barrier deposition and CMP. If required, a third wafer (or more) can be aligned, bonded, thinned and inter-wafer interconnected with the same process flow by face-to-back bonding method to achieve multi-layer 3D structures.

RTI develops the 3D integration platform for the infrared focal plane array detector (IR FPA device) application, using similar adhesive bonding and TSV approaches from RPI [9]. Fig. 3 demonstrates the cross section of the advanced 3D integrated IR FPA structure. The epoxy material is used as the bonding adhesive, and the via density in this structure is 65,536 cm^2 (256 × 256 vias). The signal conductive yield is over 99.9% with the successful demonstration of thermal image detection.

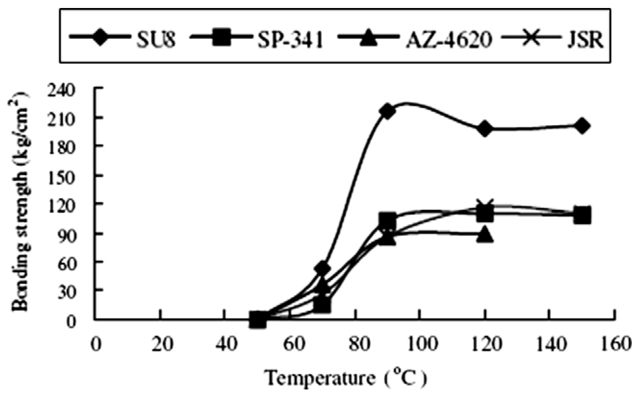

Fig. 1. The relationship between bonding strength and bonding temperature of the four adhesive materials [1].

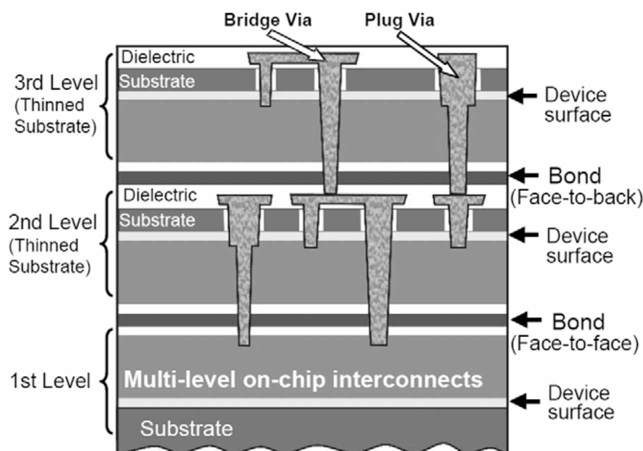

Fig. 2. Schematic representation of stacked bonding structure in the RPI 3D integration platform [7].

3. Metal diffusion bonding

The use of metal diffusion bonding (thermo-compression bonding) in 3D applications allows the mechanical and electrical connections to be made between two wafers in one step process. In this scheme, the metal pads are usually directly adopted for metal diffusion bonding. The common metal materials include Cu–Cu and Au–Au wafer bonds. Table 1 shows and compares the relative bonding conditions and bonding strength. In general, the Cu–Cu bonding temperature needs to be higher than 350 °C, and the bonding time larger than 30 min is also necessary. The research team of Professor Reif in MIT has done a series of extremely in-depth investigation on Cu–Cu bonding [10–12]. Fig. 4 demonstrates the morphology and strength map for copper wafer bonding under different bonding temperatures and conditions. Fig. 5 shows an example of the bonding interface comparison with and without annealing treatment [12]. Under this bonding condition, after annealing, no interface but Cu grain structure appears. Finally the bonding strength is increased and higher than 50 MPa.

For Au–Au wafer bonding, the general bonding temperature is about 300 °C with around 10 MPa bonding strength. However,

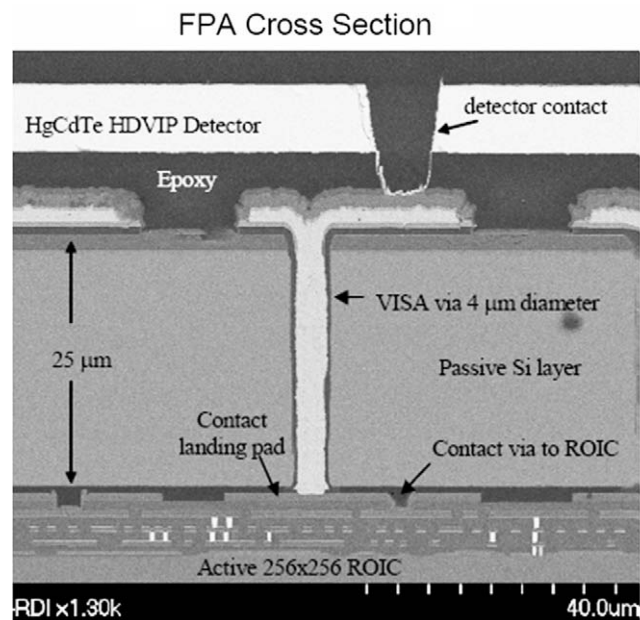

Fig. 3. The cross section of the advanced 3D integrated IR FPA structure developed in RTI [9].

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Table 1
Comparison of different metal bonding conditions and strengths (the values inside bracket indicate specific conditions disclosed in few papers).

	Cu to Cu	Au to Au	Au to Au
Plasma treatment	N/A	N/A	Ar or N_2, >150 W, 10 min
Bonding temperature (°C)	350–400	~300 (298)	150–200
Bonding pressure (mbar)	140–8000	>10,000 (5000)	8000 (4000)
Bonding time	>30 min	45 min	10 min (30 min)
Tensile bonding strength (MPa)	~50	>10	30–50
Annealing	350–400 °C, 60 min	N/A	200 °C, 30 min or not

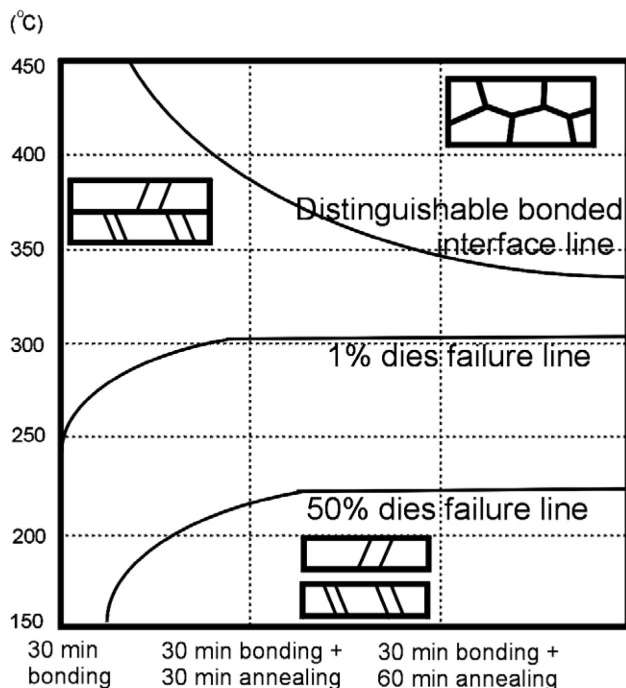

Fig. 4. Morphology and strength map for copper wafer bonding under different bonding temperatures and conditions [12].

the bonding process requires a high bonding pressure (generally >10,000 mbar except a few show 5000 mbar) [13]. According to the research from ITRI, if Ar or N_2 plasma treatment is performed to clean and activate the metal surface before bonding, the bonding

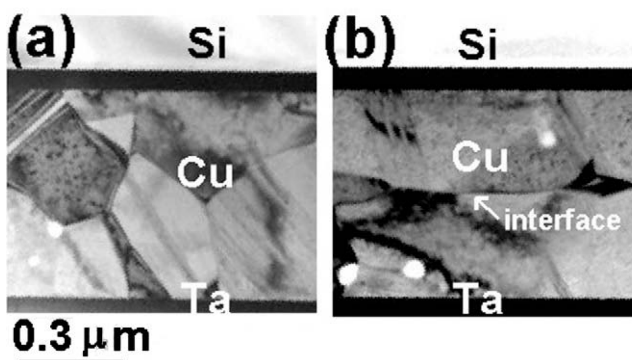

Fig. 5. TEM morphologies of (a) "grain" (bonded at 350 °C for 30 min followed by N2 annealing for 60 min) and (b) "interface" (bonded at 350 °C for 30 min) [12].

Table 2
The bonding technology comparison (Ref: EVG).

Bonding technology	Cu–Cu thermo-comp	Polymer (BCB)	Direct oxide
Bond accuracy (µm)	1.8–2	1.8–2	1.3–1.5
Future bond accuracy (µm)	1.2	1.2	<0.5
Process time per wafer (min)	60–120	30–60	3–6
Process chambers	4	4	1
Throughput (wafers/h/chamber)	2–4	4–8	10–20

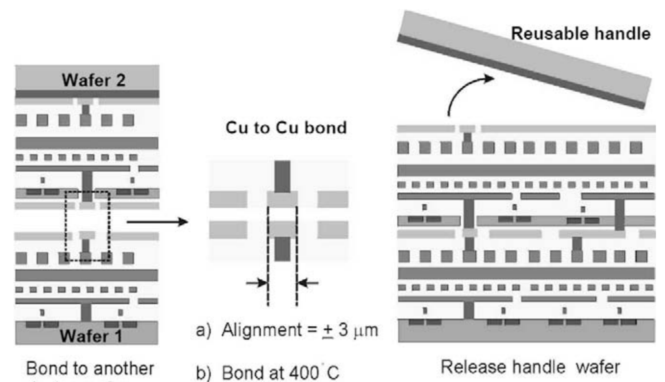

Fig. 6. The 3D integration scheme using Cu–Cu wafer bonding in MIT [16].

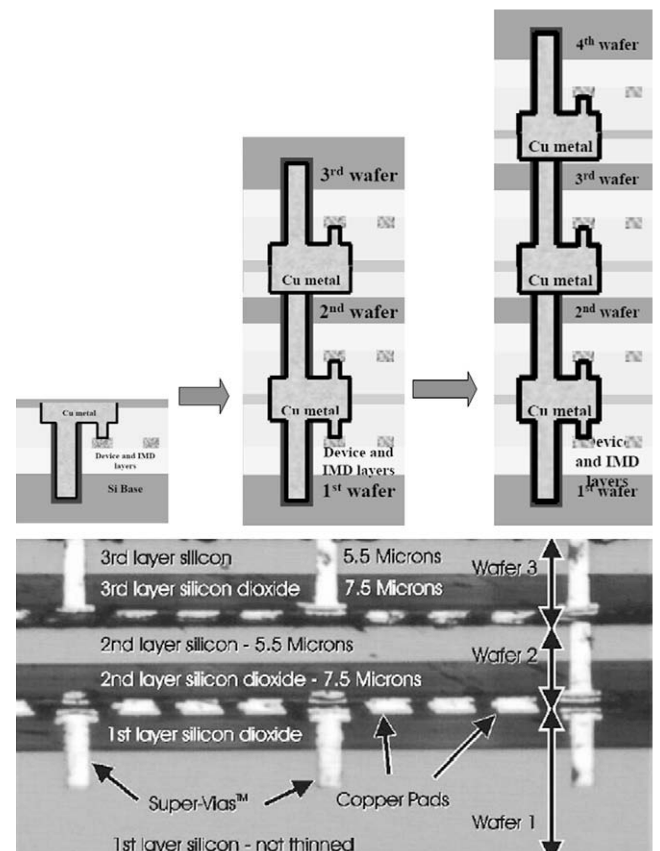

Fig. 7. The stacked scheme and cross section structure in the Tezzaron 3D integration platform [18].

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temperature can be effectively dropped to 150 °C or lower, and the bonding pressure can be reduced under 1 MPa as well. The tensile test results also indicate that the bonding strength is increased to 30–50 MPa. With annealing after bonding, the strength can be further raised about 20% [14].

With outstanding electrical properties, compatible with current IC processes, and lower cost than gold, copper diffusion bonding is still the mainstream for 3D applications, though Au–Au bonding method has the superiority of lower bonding temperature than Cu–Cu bonding. Table 2 shows the bonding technology comparison from EVG. The long process time and small throughput are still the issues in Cu–Cu diffusion bonding technology. Considering mass production for 3D IC applications, Cu–Cu bonding with high yield and throughput will be the must requirement and important target in the future.

The 3D integration scheme developed in MIT is shown in Fig. 6 [15,16]. Two FEOL active device wafers are stacked in a back-to-face fashion and bonded together by means of Cu–Cu diffusion bonding method. To start with, the front side of the top layer on SOI wafer is attached to a handle wafer. The SOI wafer is then thinned back, created the Cu vias and pads, aligned, and bonded to the bottom device layer. The bonding temperature is 400 °C, followed by post-bonding annealing step for further inter-diffusion at the Cu–Cu interface to promote grain growth. After the handle wafer is released, the 3D structure is complete as shown in Fig. 6.

Tezzaron has used Cu–Cu stacked bonding technology to fabricate fully functional devices, including a variety of standalone memories, CMOS sensor, 3D FPGA, mixed signal ASIC, and processor/memory stack [17]. The stacking method uses (a) wafer-level, (b) via-first, (c) face-to-face first followed by face-to-back stacked fashion, and (d) Cu–Cu diffusion bonding. Fig. 7 illustrates this 3D stacked scheme and cross-sectional structure using copper metal bonding higher than 300 °C [18]. The total height of the stack with several layers increases only by about 15 μm per wafer. Therefore, even a stack of many layers can be housed in the normal packaging. After the stack is completed, the substrate of the bottom wafer can be thinned and finished with standard wire bonding or flip chip assembly.

4. Eutectic bonding

Eutectic wafer bonding is another option for advanced MEMS packaging and 3D integration. Since the eutectic temperature of two metals is lower than their melting points, the wafer bonding with the binary (or more) metal system under their eutectic point can be achieved at low temperature. A unique feature of eutectic metals is the melting of the solder-like alloys that facilitate surface planarization and provides a tolerance of surface topography and particles. At present, the commonly used materials include Cu–Sn, Au–Sn, Au–Si, and Sn–Pb. For Cu–Sn case, the bonding temperature is 150–250 °C. A post aging process, 250–300 °C for 5 min, is necessary to let the unstable Cu_6Sn_5 IMC completely transfer to the stable Cu_3Sn phase. However, the electromigration (EM) intrinsic reliability issue of the Cu–Sn microconnections has to be addressed because of the increased demand for higher interconnect densities and reduced bump size [19]. The eutectic bonding temperatures for Au–Sn and Au–Si are 290 °C and 363 °C, respectively [20]. The temperature for Sn–Pb is 183 °C, which is a mature and low temperature electrical bonding method. However, this approach is

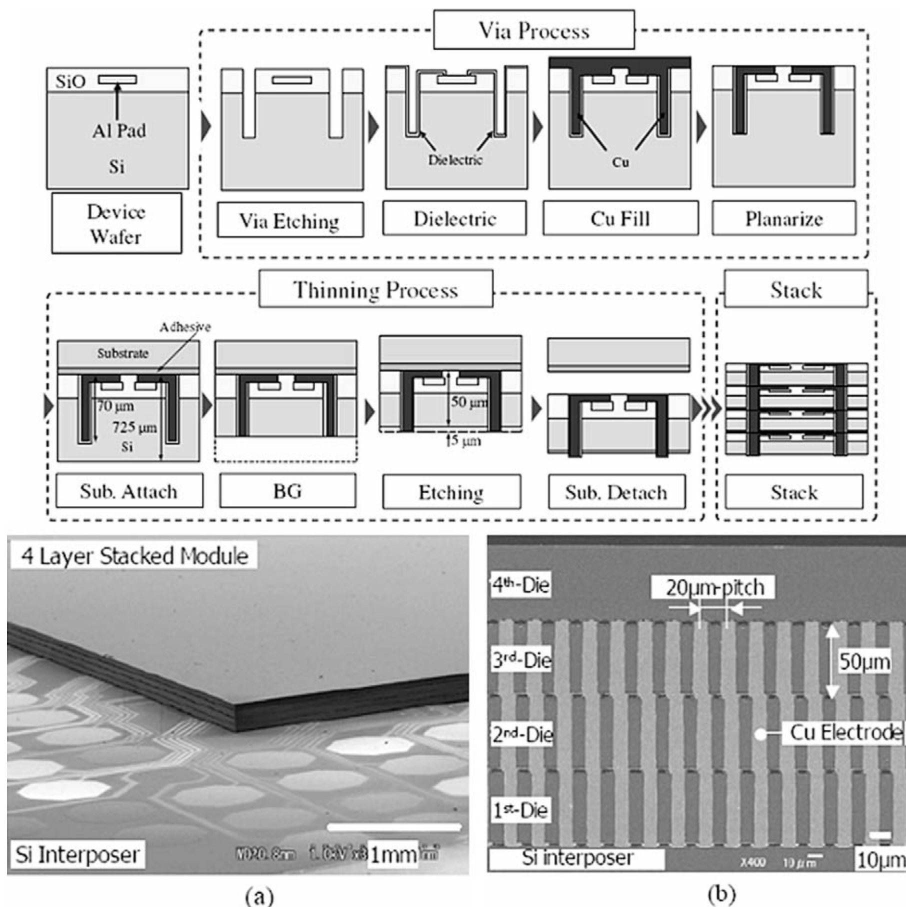

Fig. 8. The process flow and finished four layer stacked module developed in ASET [18].

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not preferred due to the lead-free tendency for all electronic products.

ASET has developed Cu–Sn connection technique in stacking integration for micro-pitch connection and stacking connection of thin chips [21,22]. Fig. 8 shows the process flow and finished four layer stacked module developed in ASET. The via-first process is used, followed by thinning process to protrude the TSV stick for Cu–Sn stacked bonding. Here tin is deposited by electroless plating method, and finally forms the Cu_3Sn IMC with copper after eutectic bonding. Four layer stacked module on Si interposer is achieved with 20 μm pitch TSV and 50 μm each chip thickness, as shown in Fig. 8.

In IZM, the so called ICV-SLID technology [23] is optimized for chip-to-wafer stacking and provides a very high vertical interconnect density ($>10^5$ cm^{-2}) based on inter-chip vias (ICV) between metallization levels of stacked dice. Both the mechanical and vertical electrical connections are realized by solid–liquid-inter-diffusion (SLID) of thin electroplated and structured copper/tin layers [24]. Fig. 9 shows the 3D integration structure developed with ICV-SLID technology. The thinned chips with tungsten- or copper-filled inter-chip vias are connected to the bottom device wafer by the SLID system (Cu, Cu_3Sn, Cu). Here the wafer thickness is down to 10 μm with ICV size 2 μm only. Thermal bonding conditions (260–300 °C and 5 bar) are used to compose the stable Cu_3Sn alloy. The fully modular concept allows the formation of multiple device stacks.

ITRI's research mainly focuses on the integration of low cost Laser-drilled Through Silicon Interconnect (LTSI) technology [25–27]. There are four major processes in the LTSI process flowchart, including wafer thinning, direct laser drilling/patterning, insulation layer formation and PCB compatible via filling/wet etching. This provides more advantages than other competing technologies not only in the compatibility with low cost silicon-through processes but also in the flexibility to the inter-chips or inter-wafers assembly of connecting different components. The feature of this structure is the through-hole copper interconnect with polymeric material insulation. In addition, Cu–Sn eutectic bonding is studied for chip-to-wafer silicon-through vertical interconnect of 3D stacking packaging. The average value of contact resistance ranges from 0.74 mΩ to 1.5 mΩ, and the reliability test also shows good results on the 3D chip stacking structure. Fig. 10 demonstrates the 20-chip stacking performed with LTSI and Cu–Sn bonding technologies [28]. The corresponding X-ray image is shown to realize the well 3D interconnection and integration on the stacked chips.

5. Silicon direct bonding

Silicon direct bonding, also as known as fusion bonding, is the spontaneous adhesion of two wafers placed in direct contact. The Si-to-Si and SiO_2-to-SiO_2 wafer bonding are the major targets. This method describes the room temperature bond between wafers with or without dielectric layers, followed by a wet chemical or plasma activation step. The wafer surface needs to be very smooth with small total thickness variation (TTV). In bonding process, two-step technique is performed with room temperature contact followed by a high temperature anneal, typically, 1000 °C, to let the interface change from hydrogen bonds to strong covalent bonds (Si–O–Si). It offers a high bonding strength in combination with stress free and hermetic sealed bonded structures. However, the high anneal temperature is higher than thermal budgets of some applications, and the method is very sensitive to particle contamination. It has been reported that a particle with a diameter of 1 μm can cause a 1 cm in diameter void when bonding an 8-in wafer [29].

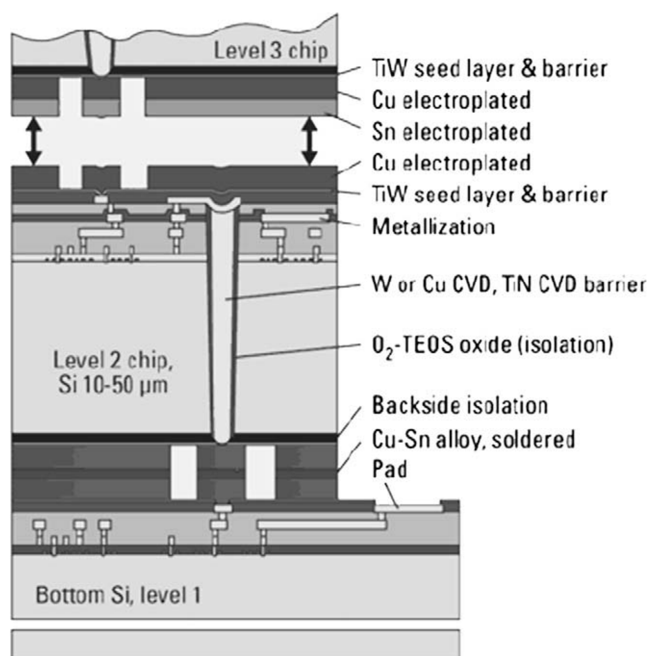
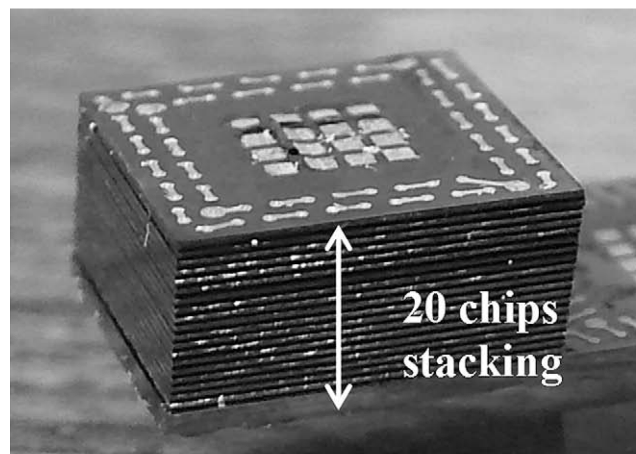


Fig. 9. The 3D integration platform developed with ICV-SLID technology in IZM [24].



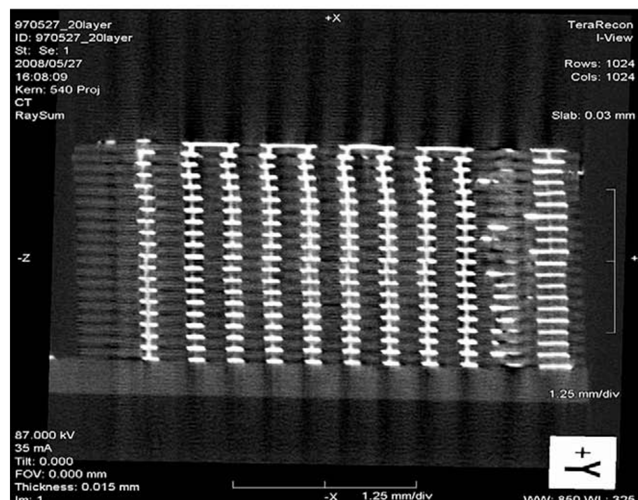


Fig. 10. 20-Chips stacking performed with LTSI and Cu–Sn bonding technologies in the ITRI 3D platform, and the corresponding X-ray image [28].

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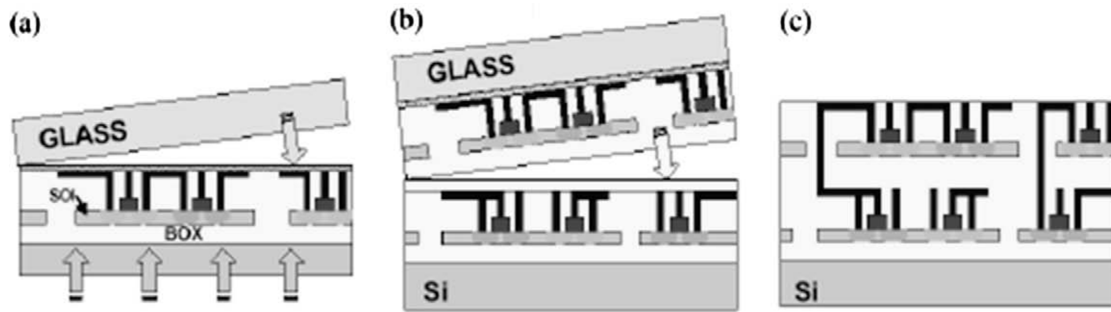

Fig. 11. Schematic representation of layer transfer and silicon direct bonding technologies in the IBM 3D integration platform [8].

One method of IBM 3D integration platforms uses silicon direct bonding approach for the permanent wafer bond [30]. As shown in Fig. 11, the front side of device SOI wafer is temporary bonded first to a glass handling wafer by organic adhesive. The device SOI wafer is then thinned to an etch-stop layer, the oxide layer (BOX) in SOI wafer, sequentially aligned and bonded to a second pre-processed device Si wafer using wafer bonding with inorganic dielectric layers (SiO_2). The wafer bonding process is chemically or plasma activated oxide-to-oxide fusion bonding, which is compatible with BEOL wafers. After the temporary glass handle wafer release, the inter-wafer vias are fabricated using Cu damascene process. The via size is 0.2 μm only with 2 μm depth around, which means each stacked layer is about 2 μm increase in total thickness, and the via density reaches to a high number of $10^8\,cm^{-2}$. If required, a third wafer (or more) can be further added to achieve multi-layer 3D structures. Another approach for comparison is the integration where SiO_2 direct bonding takes place without a handling substrate, which means the bulk lower wafer and SOI upper wafer are fabricated and bonded face-to-face, and then TSVs are formed after backside thinning to the BOX of SOI wafer [31].

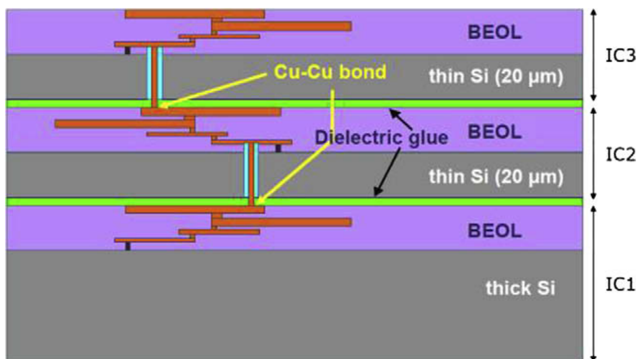

Fig. 12. Illustration of the 3D-SIC concept in IMEC: dies are separated by a thin dielectric glue layer, and interconnected through silicon Cu vias (TSVs) [34].

6. Hybrid bonding

Hybrid bonding is one emerging approach for wafer-level 3D integration [32–36]. It combines metal-to-metal bonding and wafer bonding with organic adhesives (ex. BCB) or inorganic dielectrics (ex. oxide), which can achieve intrinsic metal interconnection with adhesive serving reinforcement of the mechanical stability between stacked ICs. Because the adhesives or dielectrics can simultaneously act the roles of bonding material and underfill, they effectively increase the bonding strength and raise the device reliability. Moreover, because the electrical interconnect and micro-gap filling can be fabricated at the same time, it simplifies the process flow and avoids the micro-gap filling challenge, and therefore increases the throughput and yield.

IMEC is developing the simultaneous Cu–Cu and compliant dielectric bonding for 3D stacking, named collective hybrid bonding [34,36]. It combines fixation of a thin wafer or die by means of dielectric adhesives with the formation of metal interconnects. Fig. 12 shows the illustration of the 3D-SIC (3D-Stacked IC) concept with the hybrid bonding concept by IMEC. The introduction of a tacky polymer as an intermediate glue layer in the direct bonding scheme offers the possibility for die-to-wafer throughput optimization. The method includes pick-and-place of die and then bonding operations, as shown in Fig. 13. First, the TSV-dies are aligned and placed onto a landing wafer on which the polymer glue layer has been previously processed and patterned. This patterned tacky dielectric weakly bonds the stacked dies and fixes them during further handling. The operation is performed ideally at low temperature with the pick-and-place process repeated until the full wafer is populated. In second step, the fully populated wafer is moved to a wafer-level bonding tool where pressure and heat are applied to all stacked dies at once. Thus, the dielectric layer reflows and the metallic interconnect bonding is performed for all stacked dies simultaneously. BCB is one of the candidates as the glue material in this approach. After collective hybrid bonding of TSV-dies to a landing wafer, electrical measurements of daisy chains show a comparable and reproducible yield of 80% with working chains up to 1000 TSVs.

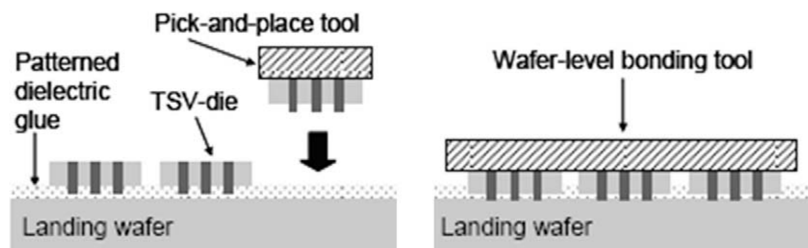

Fig. 13. Illustration of the die pick-and-place and the collective hybrid bonding process [36].

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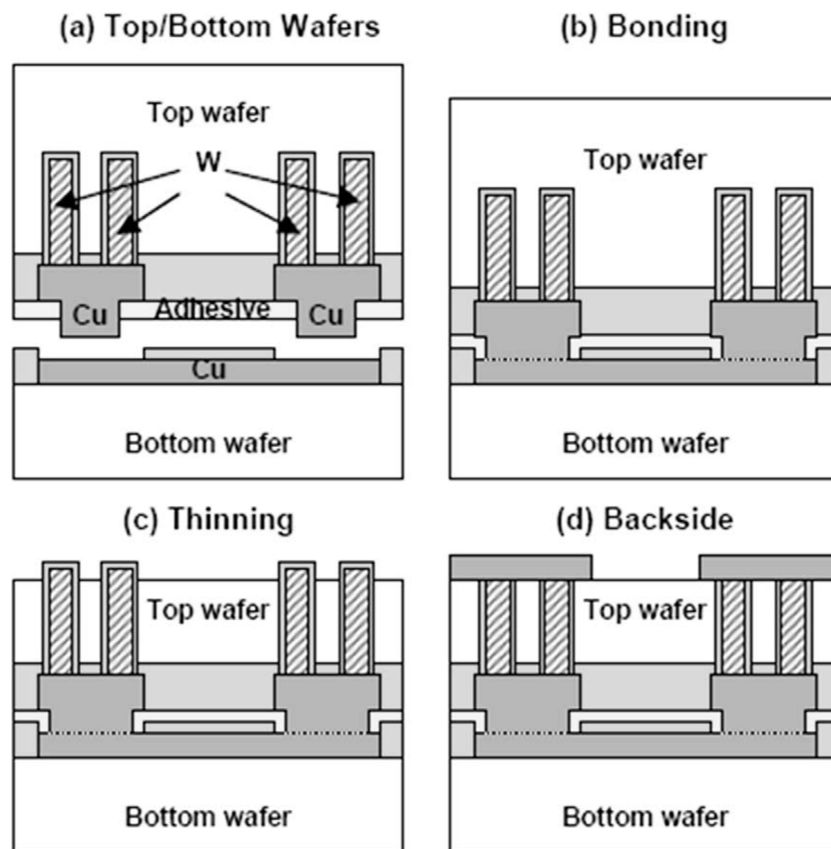

Fig. 14. Schematic diagram of 3D process flow developed in IBM [35].

In IBM, a 300 mm wafer-level three-dimensional integration (3DI) process using tungsten TSVs and hybrid Cu/adhesive wafer bonding is demonstrated [33,35]. The process flow for 3DI technology is shown in Fig. 14. The W TSVs have fine pitch (5 μm), small critical dimension (1.5 μm), and high aspect ratio (17:1). Lower CTE mismatch with surrounding Si and associated thermo-mechanical reliability benefits are included by using W TSV fill. However, because CVD W deposition results in very high stress film during deposition and is difficult to deposit more than about 1 μm thickness, design of W vias is suggested as less than 2 μm diameter with tight pitch. After W TSV formation, oxide insulation and Cu studs are formed on the top wafer. The bottom wafer utilizes Cu pads with recessed polymer adhesive openings. The wafers are then aligned and bonded in vacuum using hybrid Cu/adhesive bonding approach, also called transfer-join (TJ) method. After bonding, the top wafer is thinned to 20 μm in feature, and backside Cu metallization is patterned. The image of a completed 300 mm 3DI wafer after depositing and patterning of the backside Cu BEOL metallization is shown in Fig. 15. The electrical and physical properties of the TSVs and bonded interconnects are presented. RLC values show that both the power delivery and high-speed signaling requirements are satisfied for high-performance 3D systems.

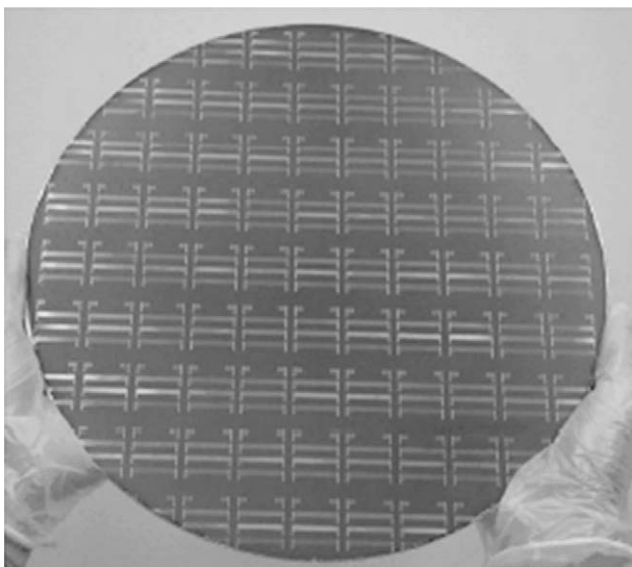

Fig. 15. Photograph of a completed 300 mm 3DI wafer [35].

7. Conclusions

This review paper summarizes wafer-level bonding technologies for 3D integration. Corresponding 3D integration technologies and platforms developed in world-wide companies or institutes are also introduced. Advantages and disadvantages of each bonding technology are discussed. Adhesive bonding has better particle contamination tolerance on wafer surface. However, this technology has potential contamination concerns on devices and fabrication tools. Metal diffusion and eutectic bonding provides direct interconnection, but un-bonded area with air gap may result in reliability issues. Silicon direct bonding provides high via density and better alignment, but the requirements of clean surface and bonding environment are very significant. Hybrid bonding, combines metal and adhesive/oxide bonding, can simultaneously achieve interconnect with adhesive serving reinforcement of the mechanical stability between stacked ICs. With high yield and

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reliability superiority, hybrid bonding has become an emerging approach for 3D integration.

Acknowledgements

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Wafer-Level Self-Aligned Nano Tubular Structures and Templates for Device Applications

K. N. Chen[1,*] and J. C. Arnold[2]

[1] Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan
[2] IBM T. J. Watson Research Center, Yorktown Heights, NY 10598, USA

A method to fabricate self-aligned nano-scale tubular structures is introduced and investigated. These tubular structures, can be fabricated on wafer-level using common CMOS technologies, are robust and cannot be removed through standard etching or resist strip techniques. This method has shown the potential to be used in different nano device applications since the size of nano-scale tubular structures is adjustable. In addition, these structures can be fabricated as nano-scale templates in advanced device applications.

Keywords:

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1. INTRODUCTION

Nano-scale materials and structures have attracted a lot of attention because of their unique mechanical and chemical properties.[1–3] Potential applications include medical devices, chemical sensors and nano-manipulators in micro-electromechanical systems (MEMS).[4–6] In addition, the semiconductor industries also look into possible applications from nano-scale structures due to the limitation of current semiconductor development in technology nodes.[7–9] Thus, fabricating nano-scale structures with existing semiconductor processing technologies becomes an attractive option for nano electronic devices. In this paper we report a technique for robust self-aligned nano-scale structures on wafer-level in a standard CMOS technology. The result was first observed when fabricating electrode heater in programmable via devices using e-beam lithography and reactive ion etching process (RIE) processes. These tubular structures and fabrication method can be applied for different nano devices. In addition, a template concept based on this technique is introduced for advanced device applications.

2. FABRICATION OF TUBULAR STRUCTURES

TaSiN is a candidate material for the electrode heater in electronic devices because of its low thermal conductivity and suitable sheet resistance. Its low resistivity and high thermal stability are also against high temperature processing.[10] For an ideal TaSiN electrode fabrication, the process flow should be as described in Figure 1. After TaSiN deposition above silicon oxide film on wafers, pattern definition is performed with patterned photo resist by lithography process. Then photo resist above TaSiN acts as a mask during RIE. The etching process should remove unnecessary TaSiN materials and stop at the oxide layer underneath. Finally, the electrode is completed after stripping the photo resist.

Optical lithography technique is the standard CMOS technology to define patterns. However, if the pattern dimension is too small (nano-scale) to use optical lithography, e-beam lithography is the only option. In this study, when the negative photo resist and e-beam lithography were used to define the pattern, the fabrication results did not match what were expected. As shown in Figure 2, instead of fabricating patterned electrodes, tubular structures right above the electrode pads were observed. The formation of tubular structures was happened along the edge of electrodes, regardless the wafer location. Most of all, these tubular structures were observed after standard photo resist removal, indicating they are robust with different composition from the original photo resist. Since the size and shape of these tubular structures are highly depended on the electrodes underneath, tubular structures can be self-aligned to the electrodes and fabricated as small as nano scale.

3. EXPERIMENTAL AND INVESTIGATION OF PROCESS STEPS

Materials and process steps were investigated to understand the details of tubular structures and the corresponding

*Author to whom correspondence should be addressed.

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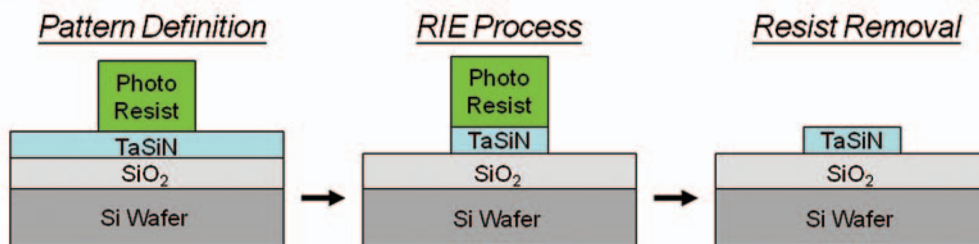

Fig. 1. Schematic diagram of ideal process sequence for TaSiN electrode fabrication.

mechanism of formation. A 500-nm silicon oxide film was first deposited on silicon wafers followed by the deposition of a 20-nm TaSiN film using a sputtering system. E-beam lithography process is used to fabricate small features of TaSiN electrodes. Because the total area of pattern electrodes on each wafer is small, a negative photo resist for e-beam lithography (NEB) is preferred to be used in this experiment. The name of NEB is 1-Methoxy-2-propanol acetate (PGMEA) and its chemical formula is $CH_3OCH_2CH(CH_3)OC(O)CH_3$, also as known as $C_6H_{12}O_3$. The detailed description of this e-beam lithography is as below:

1. HMDS vapor prime;
2. Spin NEB-31A at 3000 spin rate with approximately 200–220 nm thickness of resist;
3. Bake: 2 min at 100 degree C on a hotplate;
4. Exposure:- Tool: Leica VB6, Current: 0.5 nA, Voltage: 100 kV, Dose: 100 μC/cm^2;
5. Bake: 2 min at 80 degree C on a hotplate;
6. Develop: 30 sec in MF-321.

Figures 3(a) and (b) show the SEM images of photo resist profile for 200 nm and 800 nm pads after e-beam lithography process, respectively. Both images show the photo resists have good shapes with approximately correct heights, indicating the e-beam lithography process was performed normally.

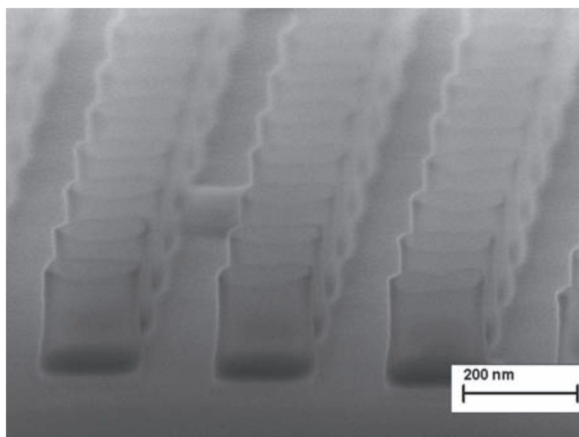

Fig. 2. SEM image of self-aligned tubular structures.

The unnecessary TaSiN region, without the photo resist protection, was next removed by reactive ion etching (RIE). The etching process was completed when the gas chemistry reaching the silicon oxide layer underneath. The gas chemistry to etch TaSiN includes the mixture of Cl_2 and Ar with the option of O_2 usage. Figures 4 (a and b) show the results of etching profiles after etching TaSiN. Both the profiles of photo resist remain good shapes without any observable damages. Images also show clearly no residual TaSiN materials remained outside the photo resist region and the etching was stopped at the oxide.

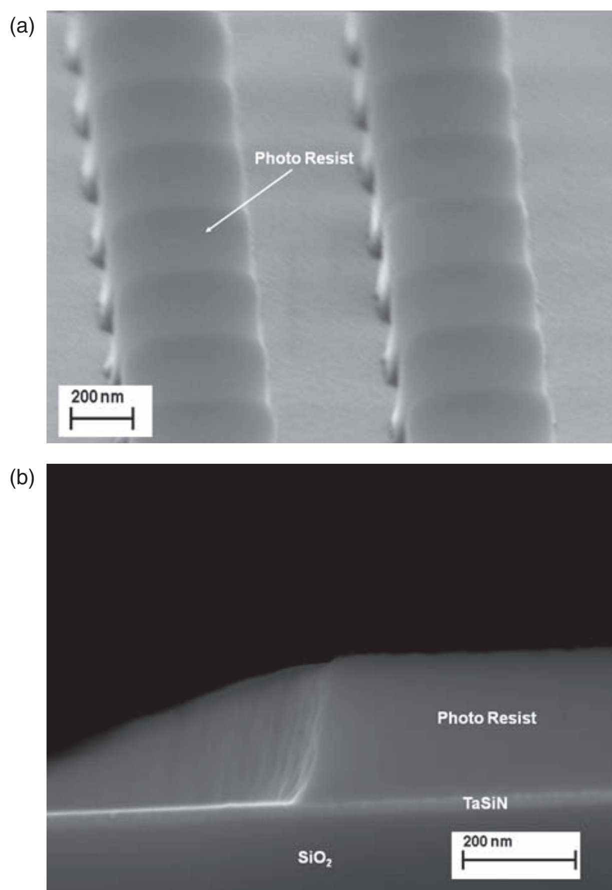

Fig. 3. (a) Negative photo resist profile after e-beam lithography process; (b) photo resist profile of 800-nm pad definition on TaSiN layer after e-beam lithography process.

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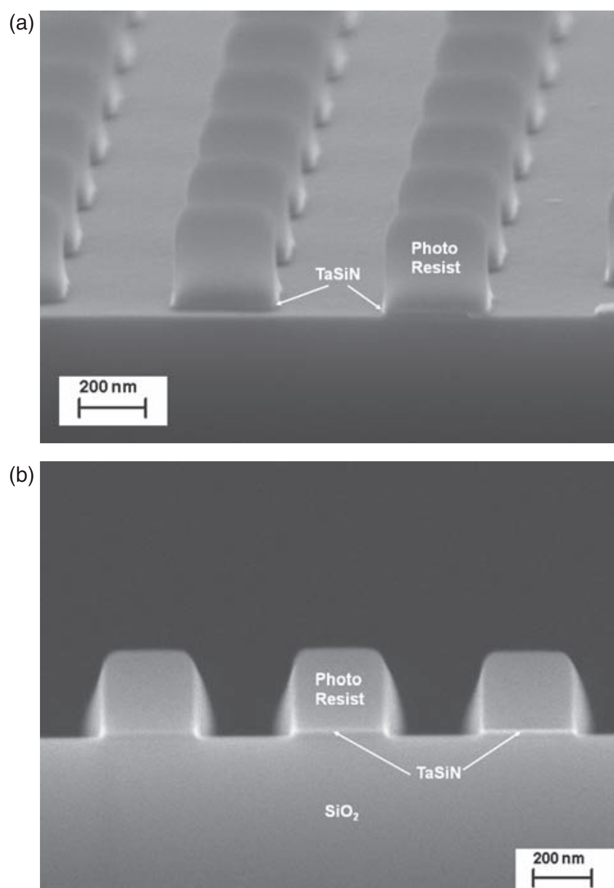

Fig. 4. (a) SEM image after TaSiN etching process. The photo resist profile keeps clean without damages during the etching process; (b) cross-sectional SEM image of structure profile after TaSiN etching process. The etching process removed TaSiN and stopped in silicon oxide layer.

The resist strip was performed right after TaSiN etching in the RIE chamber. Typical gas chemistry for resist strip includes O_2. However, as shown in Figure 2, the photo resist was not removed completely. Instead, the tubular structures were formed above TaSiN. Figure 5 shows that

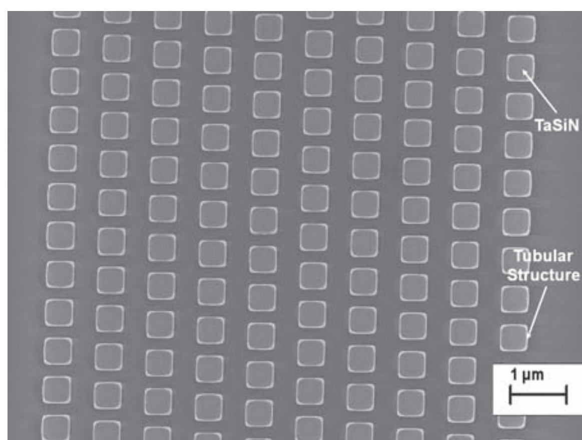

Fig. 5. Nano-scale tubular structures formed and aligned perfectly in a large array of TaSiN pads.

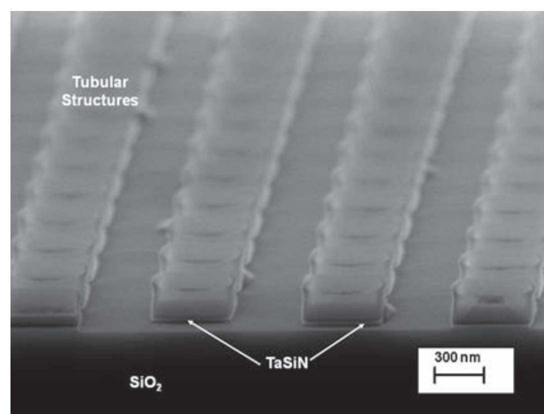

Fig. 6. SEM image of large self-aligned tubular structures.

these nano-scale tubular structures can be formed and aligned perfectly in a large array of TaSiN pads. Figure 6 shows different size (430 nm) of tubular structures other then 180-nm tubular structures in Figure 2. Since these two samples were fabricated with the same experimental parameters, it means that the size of the tubular structures can be controlled by the size of TaSiN.

4. INVESTIGATIONS OF TUBULAR STRUCTURES

In Figure 7, enlarged tubular structures are shown in this top-down SEM image. These tubular structures, fabricated on 150-nm TaSiN pads, have an average size of 180 nm between two edges. The films to compose each tubular structure are similar and the average thickness of these films is around 15 nm. Figure 8 shows the cross-sectional SEM image of a tubular structure with a 15-nm film on one 800-nm TaSiN pad. Since the tubular structures were always formed along the edge of TaSiN pads and the size of tubular structure equals the size of TaSiN pad plus thickness of two films of tubular structure, it is suggested that the tubular structure was formed on the side of photo

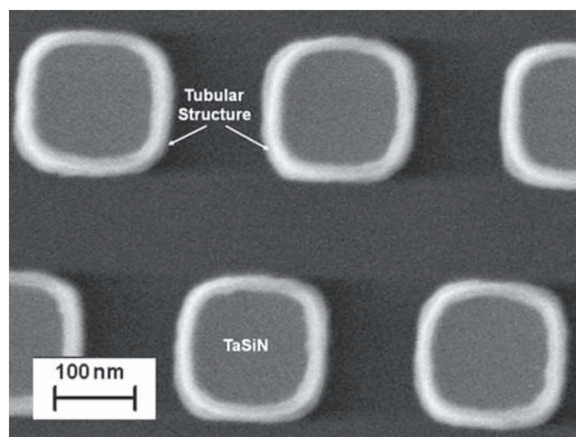

Fig. 7. SEM image of enlarged tubular structures on TaSiN pads.

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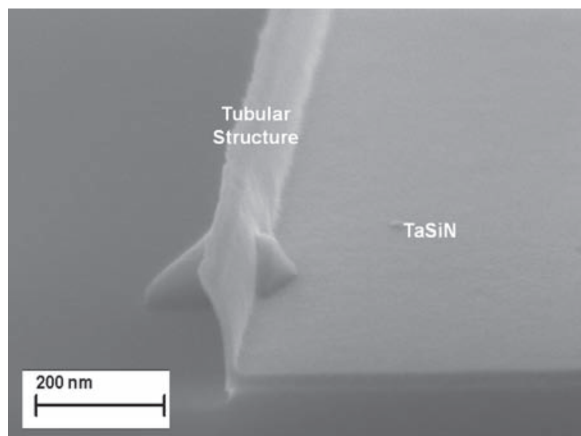

Fig. 8. Cross-sectional SEM image of a tubular structure. The film thickness of tubular structure is around 15 nm.

resist during TaSiN etching. Therefore, the composition of tubular structures may include photo resist, Ta, Si, and N.

Based on investigation results of this method, the actual process sequence of the tubular structure fabrication is shown in Figure 9. The choice for lithography in the process sequence, same as the regular process, should be e-beam lithography. During TaSiN etching, etching products coat on the side walls of photo resist and TaSiN to form tubular structures. Therefore, after the resist strip process, only the original photo resists are removed but tubular structures remain.

In order to understand the strength of tubular structures, several methods including different gas chemistries of RIE and several wet etching techniques were applied to remove the tubular structures. Table I lists trials of different removal methods and details. None of them were successfully to remove the tubular structures. Results show the tubular structures are very robust against the gas etching from O_2, CF_4, or combination in RIE chamber. Wet etching such as HCl and HF solution and standard resist strip using AZ300T could not remove the tubular resist, either. Therefore, it is suggested that the nano-scale tubular structures are not only self-aligned but also robust against standard etching processes.

Contrast to the e-beam lithography process, optical lithography process is more common in the standard

Table I. Methods and details of tubular structure removal trials. None of these methods can remove tubular structures.

Option	Methods of Removal	Gas Chemistry or Solution	Duration	Resist Removal
(a)	RIE	O_2	2 min	N
(b)	RIE	O_2	5 min	N
(c)	RIE	CF4 + O_2	1 min	N
(d)	RIE	Ar + CF4 +O_2	1 min	N
(e)	Wet Etching	Dilute HF (100:1)	1 min	N
(f)	Wet Etching	Dilute HF (100:1)	2 min	N
(g)	Wet Etching	Dilute HCI (100:1)	1 min	N
(h)	Wet Strip	AZ300T	20 min	N

CMOS technology. UVN30 is the negative photo resist for optical lithography, with the following composition:
—Propylene Glycol Monomethyl Ether Acetate: 60–95%
—Phenolic Resin: <20%
—Ethyl Lactate: <15%
—Photoactive Compound: <2%
—Polymeric Dye: <5%
—Amidomethyl ether crosslinker: <3%

Figure 10(a) shows tubular structures still formed after resist strip when optical lithography process with negative photo resist (UVN30) was used. However, they were weak and could be removed by soaking in dilute (100:1) HF solution for 1 min, as shown in Figure 10(b).

5. TEMPLATES FOR ADVANCED DEVICE APPLICATIONS

With this robust structure and the fabrication technique, a nano-scale pattern can be achieved to further fabricate nano devices. In addition to possible direct applications, because tubular structures are robust against standard CMOS etching process, template concept can be applied for device applications. Figure 11 shows the process sequence for this concept. Steps (a)–(c) are process steps for forming tubular structures, same as shown in Figure 9. Then TaSiN etching process can be applied again to remove the TaSiN materials inside the tubular structure, as shown in Step (d). Step (e) shows using silicon oxide etching to remove unnecessary area. Here nano-scale tubular structures react as masks in lithography process. Since

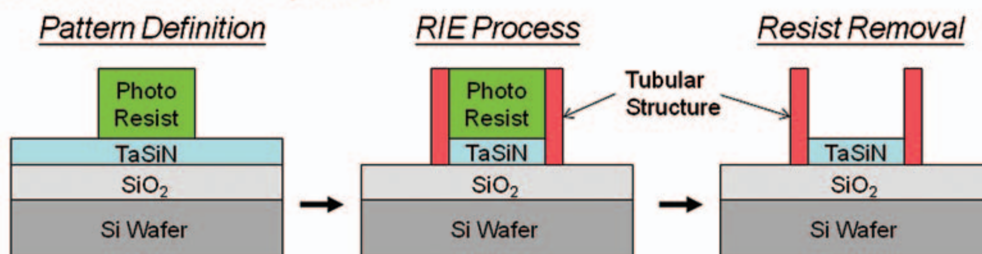

Fig. 9. Schematic diagram of actual process sequence to fabricate tubular structures by e-beam lithography and its negative photo resist.

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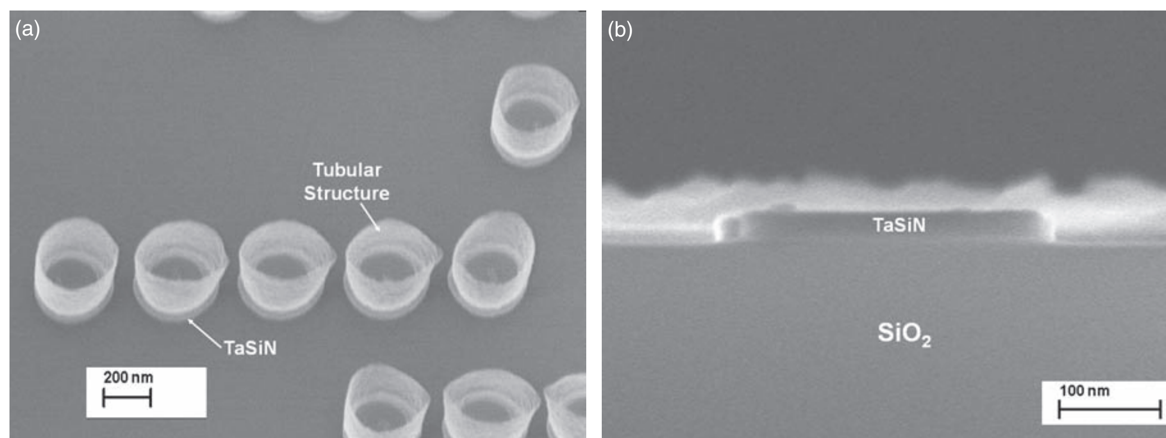

Fig. 10. (a) Tubular structures fabricated by optical lithography and negative photo resist UVN30. These structures look weaker than those fabricated by e-beam lithography; (b) SEM image of a TaSiN pad fabricating by optical lithography and negative photo resist UVN30 after soaking in dilute HF (100:1) solution for 1 min. The original photo resist UVN30 and tubular structures shown in (a) are removed.

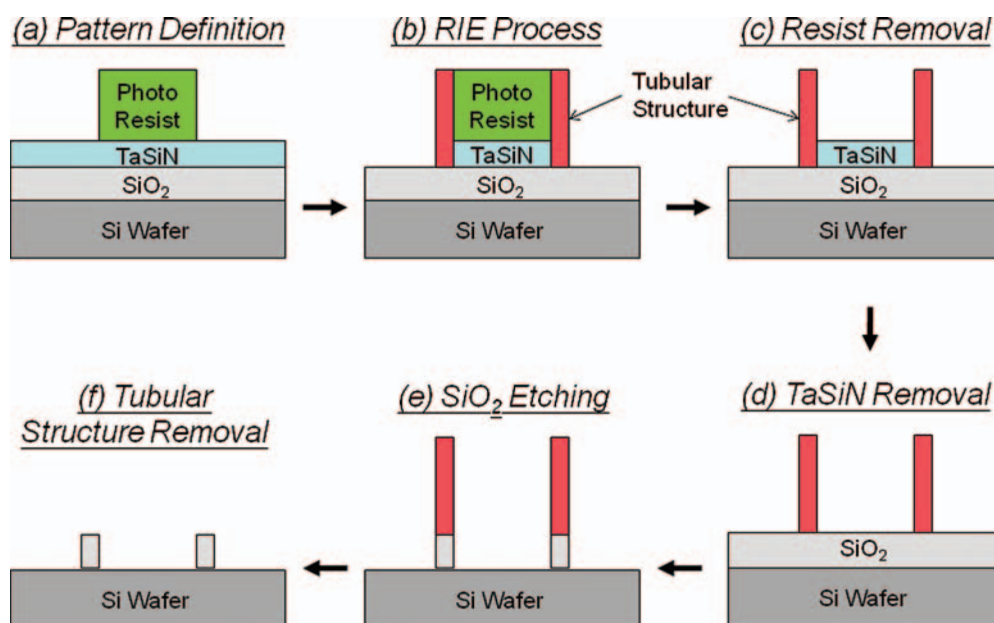

Fig. 11. Schematic diagram of template concept using tubular structure fabrication for advanced device applications.

the shape of tubular structures is flexible and the feature size is smaller than the host e-beam pattern (tubular structure only forms along the pattern edge), this technique can be used as templates for advanced device applications or growing other nano-scale materials. Finally the tubular structures can be removed by chemical mechanical planarization (CMP) or laser ablation, as shown in Step (f).

6. CONCLUSION

Fabrication and investigation of nano-scale self-aligned tubular structures are reported in this paper. These tubular structure fabricated on wafer-level are robust against etching and resist strip techniques if fabricating with negative photo resist by e-beam lithography. Process sequence and possible mechanism of tubular structure formation are discussed. Concept of template usage in semiconductor process is proposed for advanced device applications.

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The fabrication of a programmable via using phase-change material in CMOS-compatible technology

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The fabrication of a programmable via using phase-change material in CMOS-compatible technology

Kuan-Neng Chen[1] and Lia Krusin-Elbaum[2]

[1] Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan
[2] IBM T J Watson Research Center, Yorktown Heights, NY 10598, USA

E-mail: knchen@mail.nctu.edu.tw

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Abstract
We demonstrate an energy-efficient programmable via concept using indirectly heated phase-change material. This via structure has maximum phase-change volume to achieve a minimum on resistance for high performance logic applications. Process development and material investigations for this device structure are reported. The device concept is successfully demonstrated in a standard CMOS-compatible technology capable of multiple cycles between on/off states for reconfigurable applications.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

A programmable via using phase-change materials is an enabling technology for high performance reconfigurable logic applications with disruptive improvements in area and power efficiencies. Reconfigurable circuits play important roles in a wide range of microelectronic applications, such as repair of defective memory elements [1, 2] and field-programmable gate arrays (FPGAs) [3]. For repair of defective memory elements, the anti-fuse approach, often applied to DRAM repair, and the electrical fuse (eFUSE) are utilized for programmable circuits. However, both structures can be only used once and require high programming voltages [1, 2] or currents [4–6]. Regarding the FPGA concept, an array of configurable logic blocks is arranged with switches to rearrange the interconnections between the logic blocks. However, current FPGAs use flash memory and require extra space for the flash transistor. In particular, the process is not standard CMOS-compatible. Therefore, it can be seen that the current challenges for programmable circuits include 'multiple operation' and 'CMOS-compatible fabrication'.

To date, phase-change materials have drawn the most attention from semiconductor memory developers as a possible replacement for flash memory [7–10]. In contrast to phase-change memory, in which the phase-change volume is to be minimized for the smallest possible memory cell size, the volume of the phase-change material in a programmable via is to be maximized for the lowest contact resistance. In this paper, we introduce and review an indirect-heating concept to fabricate a programmable via with minimal consuming area [10]. Logic circuits associated with the programmable via are decoupled from the configuration circuits by using an independently contacted heater electrode. Since this device structure can be fabricated with CMOS-compatible processes and can be operated for multiple cycles between OFF/ON (RESET/SET) states, it shows the great potential in future reconfigurable applications. In addition, process development and material investigations of this device are reported.

2. Concept of the device structure

The schematic diagram of this programmable via device structure is shown in figure 1. The via is filled with phase-change material ($Ge_2Sb_2Te_5$), which can be switched between resistive (OFF–amorphous–RESET) and conductive (ON–crystalline–SET) states. An external heater using doped TaN material is integrated with the programmable via. The switching process is based upon the 'programming' current pulse passed through the heater. During the OFF switching operation, an abrupt high-current pulse is used to melt and quench/amorphize a thin region of phase-change via adjacent to the heater. The ON switching operation is accomplished by

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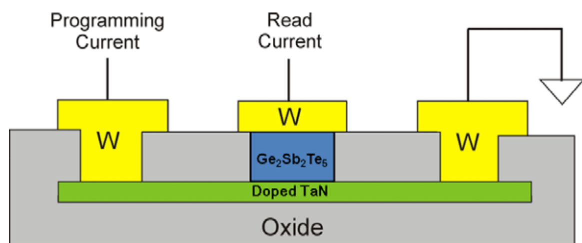

Figure 1. Schematic diagram of the programmable via concept using phase-change material ($Ge_2Sb_2Te_5$) and indirect-heating material (doped TaN). Tungsten (W) is used for electrical connection.

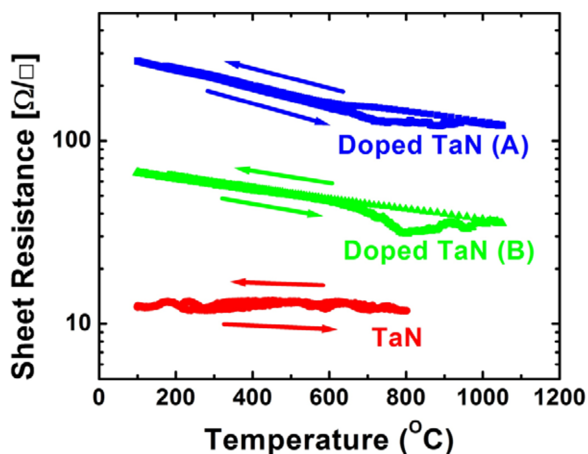

Figure 2. Sheet resistance behaviors of pure and doped TaN materials during temperature operation.

a relatively low but long current pulse applying through the heater. The heat generating from the current on the heater is capable of annealing the amorphous phase-change materials to the crystalline state. It should be noted that, in this concept demonstration, the via resistance has been measured between the top contact of the via and one of the heater contacts by a 'read' current, as shown in figure 1.

For the heater design, in order to achieve the best efficiency of electrical–thermal transformation from heater to via, the heater should be a thin layer and its material should be a refractory metal with relatively high resistivity and low thermal conductivity. Therefore, a doped TaN material is used as the heater because of its low thermal conductivity and high sheet resistance [11]. Figure 2 shows two examples of doped TaN materials with different doping concentrations.

3. Device fabrication

The device fabrication includes three sections using a standard CMOS technology: (a) heater, (b) programmable via and (c) electrical connection. First, the heater fabrication started from deposition of the doped TaN film above the silicon oxide film on the Si wafer. After the pattern of the heater was defined on the doped TaN film by RIE (reactive ion etching), another silicon oxide film was deposited to cover the heater.

The programmable via fabrication was followed by the heater fabrication. The via was defined by lithographic process

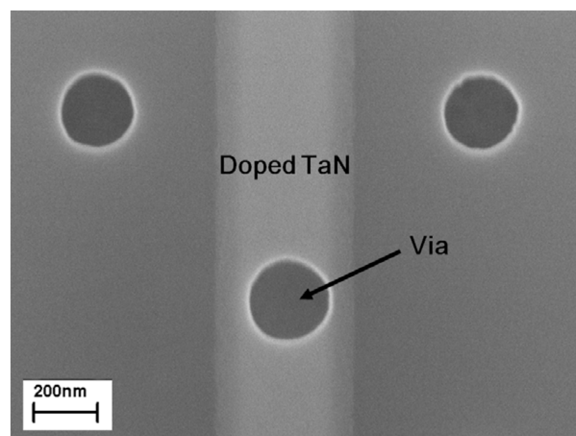

Figure 3. SEM image showing the via hole clearly defined on the doped TaN heater region.

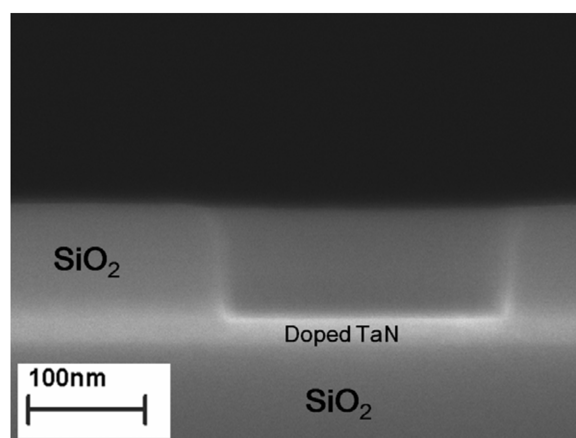

Figure 4. Cross-sectional SEM image showing that the bottom of the via hole lands well on top of the doped TaN heater.

then etched by RIE. The etched process required a good etching selectivity between oxide and doped TaN. Figures 3 and 4 show the via hole is clearly defined and its bottom lands well on top of the doped TaN heater. The aspect ratio of the via is better than 1:1, which is helpful for the later phase-change material ($Ge_2Sb_2Te_5$) deposition. After depositing TiN (diffusion barrier), Ti (adhesion layer) and $Ge_2Sb_2Te_5$ onto the via, a CMP (chemical–mechanical polishing) process was performed to removed $Ge_2Sb_2Te_5$/Ti/TiN materials outside the via. In order to prevent any contamination into the $Ge_2Sb_2Te_5$ via, a TiN cap layer, which was designed to be larger than via size, was fabricated to fully coverage the $Ge_2Sb_2Te_5$ via. Figures 5 and 6 show SEM images of device structures after the cap layer was fabricated. During the $Ge_2Sb_2Te_5$/Ti/TiN CMP process, when the CMP polishing pad was reaching the oxide surface, the polishing rate of $Ge_2Sb_2Te_5$ in the via was higher than that of oxide. This rate difference led to the via level lower than the adjacent oxide level after the CMP process. Therefore, it can be seen that the central region of the cap layer, which is corresponding to the via area, is lower than the adjacent region, as shown in figure 6.

The final section of device fabrication is electrical connection. Two W vias were fabricated to connect the

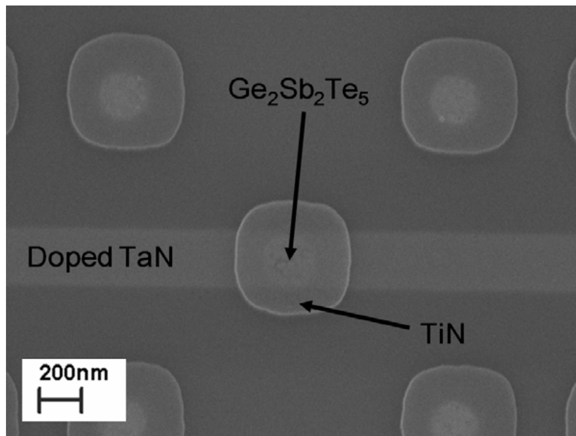

Figure 5. Top-down SEM image of the device structure after the cap layer was fabricated.

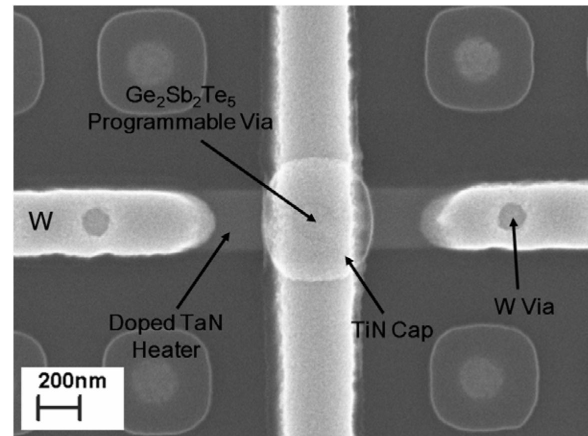

Figure 7. SEM image of the programmable via region of the final device.

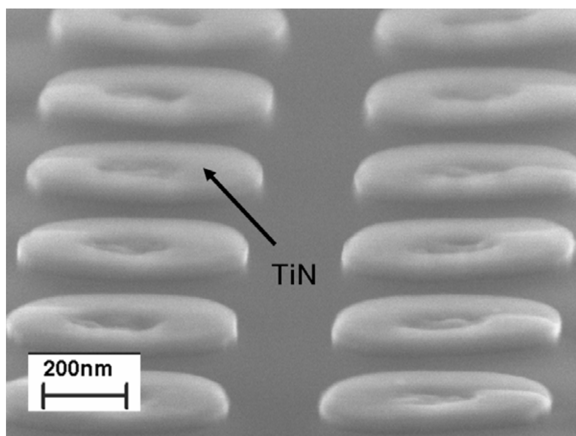

Figure 6. SEM image of the device structure after the cap layer was fabricated. The central region of the cap layer, which is corresponding to the via area, is lower than the adjacent region.

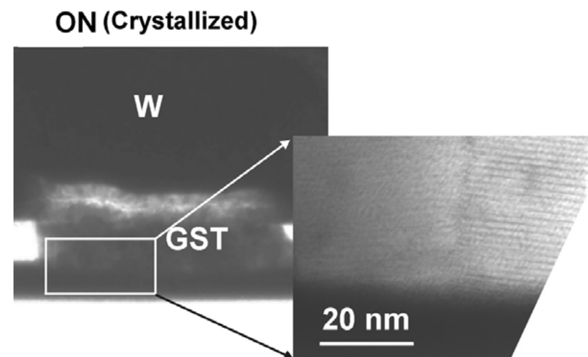

Figure 8. Cross-sectional TEM image of the via–heater interface region after ON switching operation.

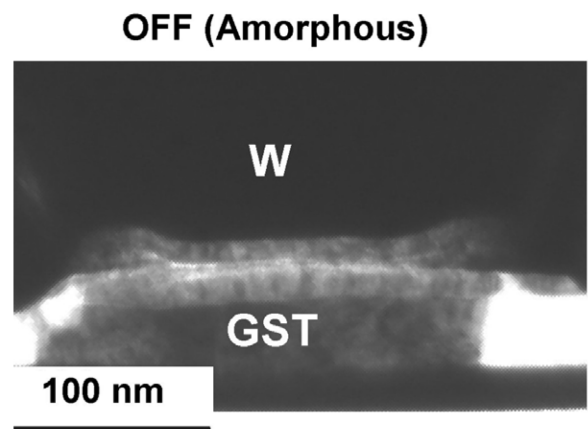

Figure 9. Cross-sectional TEM image of the via–heater interface region after OFF switching operation.

heater for electrical current delivery in the heater. The device structure was completed after the testing W pads were fabricated. Figure 7 shows the SEM image of the programmable via region of the final device. Vias with diameters of 200–280 nm were fabricated atop 20 nm thick TaN heaters that had the same width as the via diameter, and a length-to-width ratio of 6. The resistance of the doped TaN heater is ∼1700 Ω and the resistivity of the doped TaN is 6×10^{-4} Ω cm.

4. Electrical characterization

Figure 8 shows a TEM image of the via/heater interfacial region after ON switch operation. Clear crystalline and grain structures of the phase-change material are observed near the heater interface after the ON operation, indicating a crystalline state. Figure 9 shows a TEM image of the via/heater interfacial region after OFF switch operation. No crystalline and grain structure of the phase-change material are observed near the heater interface after the OFF operation, indicating an amorphous state.

Figures 10 and 11 show the R–I switching characteristics of the programmable via without device history. In figure 10, starting from the OFF state, 1 μs pulses with gradually increased power were applied to the heater. When the pulse current reached around 0.9 mA, the via resistance started to

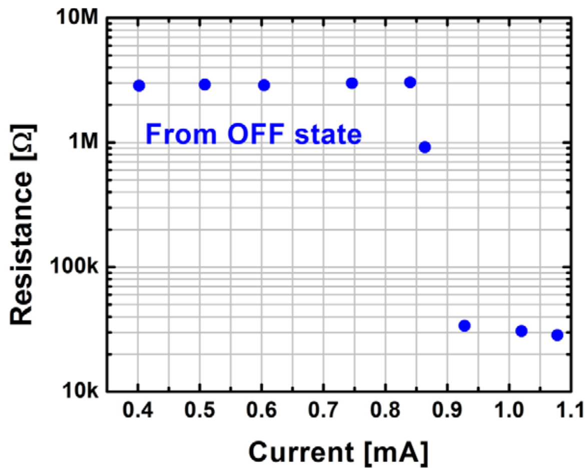

Figure 10. R–I characteristics for switching to the ON state. Via size = heater width = 280 nm; heater length = 1680 nm; heater thickness = 20 nm. ON pulse = 200 ns ramp up + 1000 ns plateau + 200 ns ramp down.

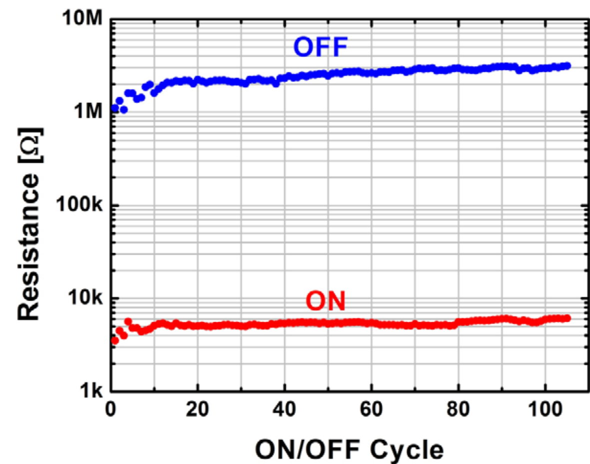

Figure 12. Cycling data from endurance tests at room temperature. Device geometry and pulse conditions are as listed in the captions of figures 10 and 11.

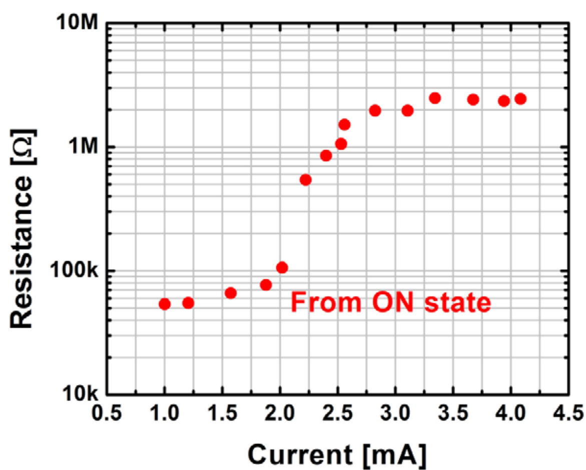

Figure 11. R–I characteristics for switching to the OFF state. Device geometry is as listed in the caption of figure 10. OFF pulses are 19 ns rise time and 2 ns fall time.

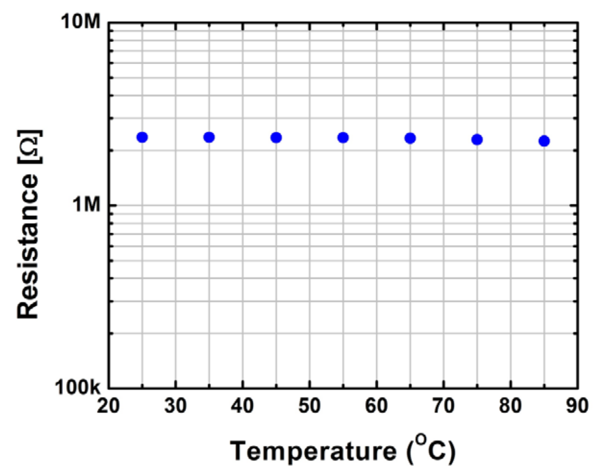

Figure 13. Measured temperature dependence of resistance in OFF state.

decrease and finally implemented switching of the device to the ON state. In figure 11, 50 ns pulses with gradually increased power were applied to the heater from the ON state. After each pulse, the via was switched back to the ON state. When the pulse current reached around 2 mA, the via resistance started to increase and finally reached the OFF state. The endurance test results in figure 12 show stable OFF/ON ratios around 400 without obvious degradation. An estimated OFF/ON ratio of an ideal four-terminal device can reach 1000 when resistance contribution from the heater to ON resistance becomes small. The temperature dependence of resistance in the OFF state is shown in figure 13.

5. Simulation

In order to further understand the behavior and predict the performance of this energy-efficient programmable via structure, several simulations were performed and compared with the experimental results of the prototype device. Figure 14 shows simulated required OFF current and programmable via dimension. Here via size = heater width = $1/6 \times$ heater length; heater thickness = 20 nm; 50 ns width OFF pulses with 19 ns rise time and 2 ns fall time. The experimental data of this device structure is also marked in the figure, showing good prediction. Figure 15 shows the simulated OFF current and pulse time at plateau. Here, via size = heater width = 280 nm; heater length = 1680 nm; heater thickness = 20 nm. OFF pulses were 19 ns rise time and 2 ns fall time. Again, the experimental data, as marked in the figure, showing good prediction within reasonable range from the simulation. These simulation results provide references for future device performance predictions.

6. Conclusions

A programmable via using an indirectly heated phase-change switch is proposed and demonstrated in this paper. In addition

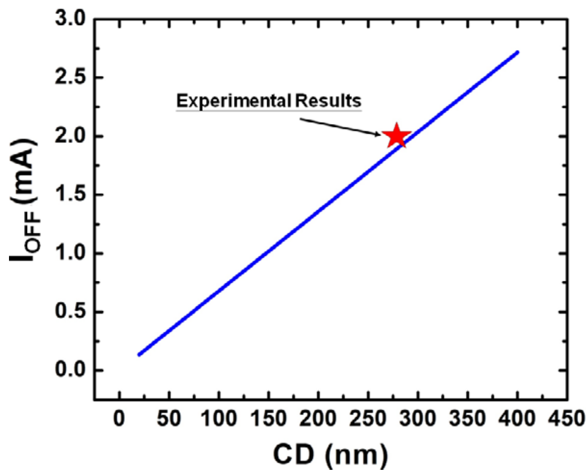

Figure 14. Simulated required OFF current and programmable via dimension. Via size = heater width = 1/6 × heater length; heater thickness = 20 nm; 50 ns width OFF pulses with 19 ns rise time and 2 ns fall time.

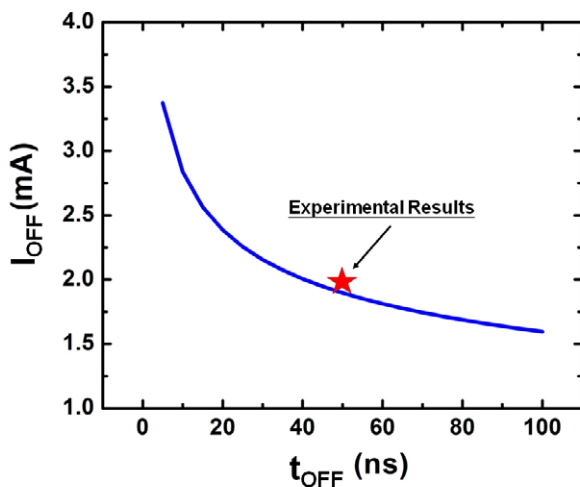

Figure 15. Simulated OFF current and pulse time at plateau. Via size = heater width = 280 nm; heater length = 1680 nm; heater thickness = 20 nm; OFF pulses with 19 ns rise time and 2 ns fall time.

to excellent electrical characterization, the device fabrication is processed in a standard CMOS technology and the device is capable of multiple operations. Therefore, this structure can be utilized for reconfigurable logic applications. Finally the good experimental data matching the simulated results demonstrates the feasibility of advanced device applications.

Acknowledgments

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