行政院國家科學委員會專題研究計畫 期中進度報告

極紫外光(EUV)微影技術從光源建造、光罩、材料、製程到奈米元件可靠度研究(2/3)

期中進度報告(精簡版)

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計 畫 主 持 人：黃遠東
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李佳翰、林俊宏、崔秉鉞、謝健

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行政院國家科學委員會專題研究計畫成果報告

極紫外光微影技術-從光源、光罩、材料、製程到奈米元件可靠度研究 2/3

Investigations on extreme ultraviolet lithography from beamline construction, masks, materials, processes, to reliability of nano devices 2/3

計畫編號：NSC 98-2120-M-009-007

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謝健 奈米元件實驗室

一、中文摘要

在第二年計畫完成後，本計畫已成功建構包括高精度 EUV 反射儀，配備四極質譜儀的光阻釋氣分析系統以及干涉微影系統等重要設備，並配合同步輻射 EUV 光源，建立相關實驗分析技術。EUV 可能造成奈米元件輻射損傷也被有系統的研究。上述分析技術與設備，目前均有國內半導體廠實際委託，合作或參與研究，並借用本計畫所建構的儀器與技術在同步輻射中心進行研究分析。國內半導體廠也已著手建構類似設備，進行 EUVL 相關研究。本計畫已由零開始，順利啟動台灣的 EUVL 研究。

關鍵詞：極紫外光、微影技術、半導體、同步輻射

Abstract

Based on synchrotron-EUV light source, this project has established several important endstations and analytical technologies for EUVL-related researches. They include a high-resolution EUV reflectometer, a resist evaluation system coupled with QMS, and a EUV interference lithography system. The issue of EUV radiation damage on the nano-devices is also systematically studied. Based on the above achievements, domestic semiconductor companies have coupled with this project via commission projects or join researches, and even begin to design/ construct their own EUVL equipments. This project has successively initiated EUVL-related researches in Taiwan.

Keywords: Extreme UV, Lithography, Semiconductor, Synchrotron

二、緣由與目的

半導體相關工業是台灣的兆元產業，但是因應次世代微影技術發展，迄今並無極紫外光微影技術相關的大型研究計畫。本計畫嘗試整合國家實驗室(國家同步輻射中心，國家奈米元件實驗室)與大學(交通大學、台灣大學、成功大學與高雄大學)之儀器與人力資源以啟動台灣極紫外光微影技術之相關技術研究。在這個計畫中，主要建立在極紫外光微影技術中最必要的技

術，即分析和檢測技術。

本計畫根據工作屬性區分為(I).基礎研發、(II)光學與檢測技術、以及(III)極紫外光微影技術之相關應用研究等三組。其中基礎研發(I)的主要目的是建立基礎的儀器設備(極紫外光微影技術之光束線，反射儀和光化學檢測平台)以量測分析基本的材料性質與行為；光學與檢測技術(II)的主要目的是研發創新的檢測設備(高效率光罩檢測與極紫外光微影技術之干涉微影設備)以進一步提升極紫外光微影技術之檢測應用；極紫外光微影技術之相關應用研究(III)的主要目的則是研究探討極紫外光微影技術應用於元件製造時可能發生的關鍵問題(輻射損傷、抗反射層、混合微影製程和奈米元件圖形化製程之研究)，以提供可行的解決方案。

三、結果與討論

根據第二年計畫目標，本年度主要的研究成果包括:

3.1 設計與建造一真空系統以四極質譜儀測量光阻釋氣 (圖 1)

為了要量測絕對釋氣量，本團隊發展出一套標準作業流程以標訂釋氣的量測系統，此流程可導出個別粒子的抽氣效率、離子壓力計的絕對量測標訂及四級質譜的穿透效率。藉此系統參數的校正與修正，不同流量及不同種類氣體的定量相符程度可達±20%。目前已求得初步的絕對釋氣量結果：量測標訂(benchmarking)光阻樣品 round robin resist (RRR) 的釋氣量(SEMATECH 組織八個研究團量測[K. R. Dean , et al., Proc. SPIE 6519 (2007) 65191P])，測得在 0.4 W cm^{-2} 能量密度的 EUV 光照射下之 RRR 釋氣量為 7x1015 粒子/s，此數值落在標訂樣品合理的釋氣範圍內。某一底層樣品在 IMEC 的 0.4 W cm^{-2} EUV 照射量下釋氣速率為 2x1014 粒子/s，而本實驗室之估計量為 1x1014 粒子/s。

目前，本組人員正與 TSMC 及 NCI 合作，利用已在 IMEC 測得釋氣速率的新穎樣品，在 NSRRC 進行標竿釋氣速率實驗。藉此，本團隊除具備光阻釋氣的基礎研究能力外，並將在台灣建立起具世界標準光阻釋氣評估能力之設施。

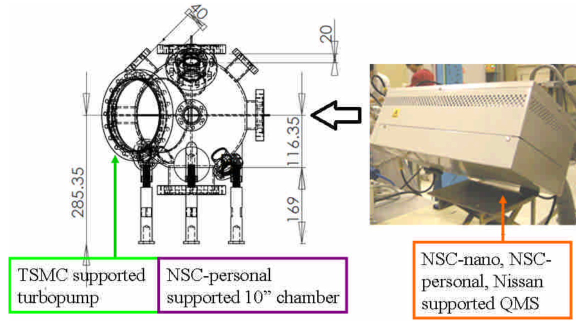

Fig.1 A new QMS system for resist outgassing evaluation will be ready in July. Major components including a turbmolecular pump, load-lock chamber, and a 10" measurement chamber.

3.2 極紫外光干涉式曝光平台之建置

目前，極紫外光干涉式曝光平台(圖 2a)已建置於同步輻射中心光束線 U9，可針對 15x20 mm 的試片進行曝光試驗。在穿透式繞射光柵的製作上，使用電子束微影(Leica Weprint 200, NDL)製作 300 奈米間距(光阻劑為 PMMA)，線寬與間隔 1:1 的繞射光柵。鉻光柵層的厚度 60 奈米，一階繞射效率經計算約 5%。實驗結果發現，干涉所得之一維線寬縮減至 75 奈米。二維繞射光柵是使用四道光束的干涉，繞射光柵週期為 400 奈米。經由模擬可知，二維繞射光柵曝光後的圖案是格子點陣列，並且間距為原光柵間距的 1/2 。圖二(b)是實際曝光結果，可以發現光阻圖案上間距縮減為約 282 奈米。在未來我們將繼續進行更小線寬的曝光試驗，目標在間距 100 奈米(干涉條紋線寬約 25 奈米)以下的光柵製作以及曝光，並針對不同光阻劑 PMMA 及 HSQ 等尋求更佳曝光結果。

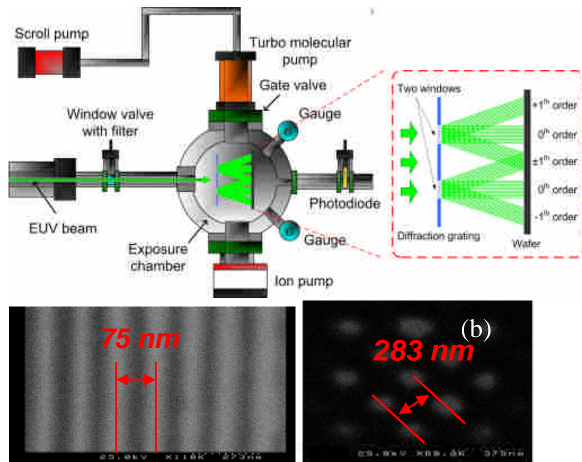

Fig. 2 (a) Scheme for the four beams exposure; (b) SEM picture of the 1D and 2D interference-lithographed pattern.

3.3 設計及模擬菲涅耳波帶片極紫外光光罩檢測系統

利用純量繞射理論來模擬複合式菲涅耳波帶片在空間中或聚焦平面上的電場強度以及光強度之分佈，進而討論傳統菲涅耳波帶片以及設計於極紫外光下的複合式菲涅耳波帶片其聚焦特性。圖三(a)為七種不同的結構在聚焦平面上之場強度分佈圖，七種結構皆以製程極限 50 nm 之最小線寬為考量來進行設計。由於菲涅耳波帶片其線寬為由內往外遞減，如何穩定製程的準確度，使其達到每圈的變化在菲涅耳波帶片的製作上是一個問題。因此，利用臺灣大學電子束實驗室之電子束微影系統，其型號為 ELS-7500EX 的電子束直寫儀，並且使用 ZEP-520A 為電子束光阻在矽基板上進行結構製作測試，圖三(b)為線寬測試顯影之後的電子顯微鏡相片，圖三(c)則為圖三(b)之局部放大，其右下角線寬約為 200 nm。

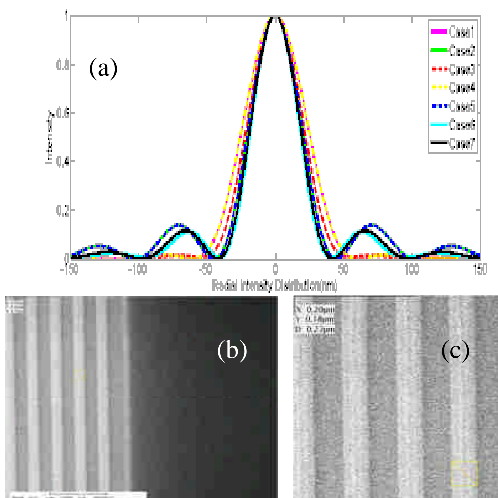

Fig. 3 (a) The field intensities in the focal planes of seven different structures. (b) the SEM photos of the grating lines; (c) zoom in of (b).

3.4 極紫外光輻射對先進非揮發性記憶體及高介電常數介電質的影響

在此高介電常數介電質的研究中，為了符合半導體產業未來的發展趨勢，探討 EUV 輻射對金屬閘極/高介電常數介電層(High-κ dielectronic)的影響。選用氮化鈦(TiN)為金屬閘極材料，並選用兩種介電層，分別為二氧化矽(SiO2)、氧化鋁(Al2O3)，製作成 MOS 電容器。結果顯示 SiO2 的抗 EUV 輻射能力不錯(圖四)，可能和 SiO2 內部的電洞缺陷密度以及吸收 EUV 的效率有關。

另一部份是探討 EUV 輻射對非揮發性記憶體的影響。本次研究針對先進的 TFT-SONOS、多閘極氮化鈦(TiN)奈米晶粒非揮發性記憶體進行輻射傷害及特性變化的研究。SONOS NVM 元件結構為 SiO2(4nm)/Si3N4(7nm)/SiO2(20nm)。NC NVM 元件結構為 SiO2(4nm)/TiN+Al2O3(7.5nm)/Al2O3(20nm)。結果顯示 NC 結構相較於 SONOS 結構擁有良好的 EUV 輻射抵抗能力(圖五)。

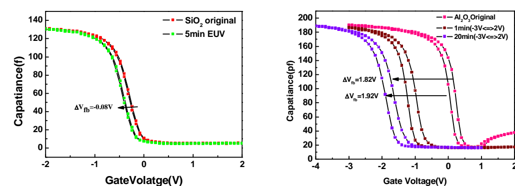

Fig. 4 C-V characteristics of the capacitors with (a) SiO_2, (b) Al_2O_3 before and after EUV exposure.

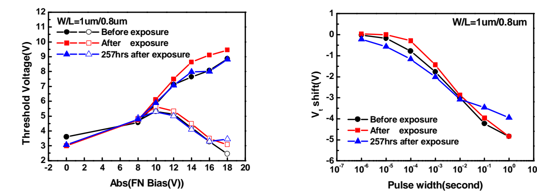

Fig. 5 (a) Memory window and (b) erase speed characteristic of the TFT-SONOS NVM before, after 3 minutes EUV exposure, and 257hrs storage after exposure.

四、計畫成果自評

本計畫由零開始，啟動台灣的 EUVL 研究。在第二年計畫完成後，目前主要的成果效益包括:

(1)成功建構包括高精度 EUV 反射儀，配備四極質譜儀的光阻釋氣分析系統以及干涉微影系統等重要設備，並建立相關實驗分析技術。

(2)上述分析技術與設備，目前均有國內半導體廠實際委託，合作或參與研究，並借用本計畫所建構的儀器與技術在同步輻射中心進行研究分析。

(3)國內半導體廠已著手建構類似設備，進行 EUVL 相關研究。

(4)本計畫已投入超過 30 位師生從事 EUVL 相關研究，並已有超過 10 篇的碩士論文

產生，期刊論文陸續發表中。

根據上述成果，計畫成員自評本計畫大致依據原規劃進行，並達成預期目標，特別是延伸的產業應用。本計畫將根據第一期計畫成果，配合未來產業的實際需求，提出第二期的國家奈米學研計畫。

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行政院國家科學委員會補助國內專家學者出席國際學術會議報告

99 年 3 月 5 日

報告人姓名	鄭秀英	服務機構及職稱	國立高雄大學應用化學系 副教授
會議 時間 地點	2010/02/21 – 02/26 美國聖荷西	本會核定 補助文號	
會議 名稱	(中文)2010 年 SPIE 先進微影研討會 (英文)2010 SPIE Advanced Lithography		
發表 論文 題目	**(中文)** 光阻及底層材料經 13.5 奈米光照射的光吸收與薄膜厚度損失(第一及通訊作者) **(英文)** Absorption and loss of film thickness in photoresists and underlayer materials upon irradiation at 13.5 nm (first and corresponding author)		

報告內容應包括下列各項：

一、 參加會議經過

The proceeding included three plenary presentations, six technical conference sessions, and four panel discussions. The six technical conferences ran in parallel; therefore, I attended the plenary presentation section, two panel discussion sessions, and the extreme-ultraviolet lithography (EUVL) or resist conference session depending on the subjects, which were of my interest.

(1) Plenary presentations (02/22, Mon., 8:30 – 10:30)

-- "The future of optical lithography" by K. Ushida of Nikon Corp.

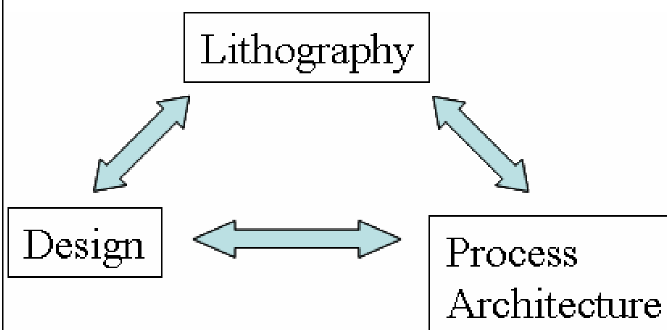
Nikon showed its roadmap to extend the 193 nm-immersion down to the 22 nm half-pitch (HP) technology node with a double patterning (DP) method, and predicted that EUVL is too late for the 22 nm HP node and a strong candidate for the 16 nm HP node. To realize the DP method for high-volume manufacturing (HVM) at the 22 nm node, a source-mask optimization, overlay budget, and cost-of-ownership (COO) are critical issues. On the other hand, a zero-defect mask, mask inspection, powerful EUV source are current issues that have to be solved to make EUVL possible as a next-generation lithography (NGL) technology.

-- "Investing in technology industries in the reset economy" by Eric Chen of Silver Lake Partners

Dr. Chen provided a global view of the evolution of the IC industries. He predicted that the service of data trafficking will be doubled each year. He also pointed out that Asia, especially China, will play a new role in the future technology development, with its low R&D cost and short R&D period. He gave examples of "山寨版" consumer products to show to the fact that US is no longer dominates in R&D.

-- "Lithography of the future: a technical and economic challenge" by S. Kivakumar of Intel Corp.

Dr. Kivakumar explained the role that lithography has played from the early, current to the future IC manufacturing. At an early stage, the lithography process was just a module along the Research-Development-Manufacturing pipeline. Lithography evolved further to applying the optical proximity correction method to accommodate the IC design; further down to the 45 nm HP node, the lithography technology started to influence the overall process architecture, using the decision of using ArF-dry or ArF-immersion to pattern 45 nm HP as an example. Nowadays, computational lithography, mask technology, mask making are also key enablers for the success of a technology node. The role of lithography is now a key of a "triumvirate":



He also mentioned about COO will be the key to select the future litho technology for HVM. Fab. EUV inspection needs include 100% confidence on defect detectability and mask cleanness.

(2) Panel Discussions

-- "EUV source $10M. EUV scanner $100M. Defect free EUV photomask, priceless! For some there's NIL, for everyone else, there's EUV." (02/22, Mon., 19:00 – 20:30)

Intel: Using DUV mask inspection tool, Intel was able to detect 70 nm mask defects; with such a capability, the 32 nm HP manufacturing posts no immediate risk for HVM. The target of this year is to detect 50 nm defects on masks. The actinic mask inspection will be needed for driving the IC technology down the road, it has to equip with the capability not smaller particle size, but also mask phase defects. The mask repair technique is also needed.

TSMC: TSMC announced that its EUVL application will be ready in the time frame of 2013-2014. It showed a COO calculation in the 2013-2014 time frame with EUVL much cost effective than multiple patterning; however, the mask cost was not included in the COO calculation. That brought a big laugh from the audiences.

Toshiba: Toshiba showed their investigation results and tabulate the current and needs for mask and imaging inspection as the following:

	Phase defect	Pattern inspection	Aerial image inspection
Ideal	Actinic	Actinic	AIMS™ EUV
Reality	Position DUV ↓ Actinic	HP 2X nm DUV ↓ HP 1X nm EB	AIMS™ EUV

SEMATECH/Intel**:** Sematech proposed the priority concerning about to develop the mask and imaging inspection capability as AIMS for the aerial inspection, actinic substrate and mask blank inspection, and actinic or advanced tech for the pattern inspection. It is widely said that the mask inspection is more critical, cost effective, and practical than the pattern inspection occurred later on.

Carl Zeiss: Sematech organized an EUV mask infrastructure consortium (EMI) in late 2009. Carl Zeiss layouts its roadmap to have the first AIMS system ready within 3 years.

-- "**The trial of EUV and DPT ArF for the 22 nm 1/2 pitch node**", 2/23, 19:45 – 21:00

(I lost notes of this section.) In brief, each side swore to tell the truth and only the truth in a humorous way, and showed their results on imaging, overlay, and COO. The jury (audiences) clapped hands to vote, and at the end it was no conclusion about which technology will be the winner for the 22 nm 1/2 pitch node.

(3) Poster Session (02/23 and 02/24, 18:00 – 20:00)

There were more than 300 posters in these two-day sessions. I posted my result, and discussed with IMEC (EU), CNSE (USA), NIST (USA), and SELETE (Japan) researchers who work on resist outgassing, and exchanged information about each other's latest progress. IMEC's witness-plate result drew a much attention to the rest, because they showed the first evidence of sulfur contamination on the EUV optical surface, in addition to the fluorine-contamination they have reported last year.

(4) Conference sessions
-- Extreme Ultraviolet (EUV) Lithography

Date	Affiliation	Description of the presentation
2/22	SELETE	Actinic mask inspection status at SELETE, capture rate 99% for mask blank but poorer of patterned mask.
	Carl Zeiss	The EUV optic progress made by CZ. Pre-production Starlith (NA=0.32, six mirror design), production Starlith 3300 (NA = 0.5, 8 mirror design).
	Sematech	For the resist evaluation of PAG-bound, PHS, and PAG-blended resist, Samsung assignee at Sematech reported that Samsung will use PAG-bound photoresist for its 30 nm HP node.
	Fujifilm	Fuji studied factors of PAG loadings, cation design, increasing ionization efficiently of resists, PAG diffusivity, quencher loading, and PEB temperature for improving the EUV resist sensitivity.
	LBNL	LER ~ 1/image gradient, and Z factor was mentioned here. Z factor was later reported repeatedly by all resist studies. Z-factor = $(\text{Resolution})^3 \times (\text{LER})^2 \times (\text{Sensitivity})$.
	MIT	The study mentioned that the thickness loss of PMMA is KrF > ArF > EUV as a function of photon absorbed. This result is very different from what we found on literature reports. Its observation of very little FT-IR peak change is consistent with ours. We will wait for its full paper to compare with our findings.
2/23	Gigaphoton	Gigaphoton reported its current status and roadmap of EUV sources. The current output of 14 W at IF was said to be able to deliver 200 W in 2012 and 400 W in 2014.
	Energetiq	Energetic delivered 15 systems worldwide for outgassing and mask blank inspection. It layout the roadmap of its improvement for more EUV power enough for the actinic mask inspection.
	NIST	NIST reported its latest progress, in addition to its TD/MS facility, now it has XPS and ellipsometry to examine hydrocarbon contamination on a witness-plate.
	Rutgers U	The hydrocarbon contamination model was proposed as a ML chemisorption and multilayer physisorption of C-contaminants by a thermodesorption study.
	Albany U	The C-contamination on patterned masks was examined. Non-uniform deposition of carbon on absorber patterns to form a T-top topography was found.
	Globalfoundries	No observable carbon contamination was observed for a globalfoundries' mask, which was exposed by ~500 wafers at ADT. Notable that ADT was equipped with a contamination mitigation facility, it is less sensitive to C-contamination than MET at ALS.
	Intel	Intel showed its investigation on improving EUV resist performance, and gave the improvement by the reduction of the Z factor. Process parameters included etch/trim, vapor smoothing, hard bake, ozonation, and rinse. Underlayer material + champion resist (positive-tone molecular glass) by the dipole exposure shows the Z-factor of this year to be a number of 7.1. LWR and pattern collapsing remain critical.
	Samsung	Samsung reported its roadmap for EUVL to be inserted in the 30 nm DRAM generation. It reported results on bound-PAG with sensitizer, using underlayer, rinse, chemical treatment, and dry etch for improving the EUV performance.
	KLA-Tencor	It reported the latest simulation capability to predict resist blur in a stochastic way.
	SELETE	Using the EUV1 exposure too, it reported alternative developer solution using TBAH, optimal developing time, using underlayer materials, optimal rinsing processes as effective means to improving resist patterning.
	JSR	Molecular glass "Noria" was again mentioned to have a good resist performance for patterning 22 nm HP. To improve resist sensitivity and LER, detailed acid amplifier and photodestructive anion PAG approaches was given, respectively.
1/24	XTREME	The progress of using tin DPP as an EUV light source was reported. The current ADT's light source used DPP. The roadmap to fulfill HVM was given as a 500 W at IF light source.
	U Illinois	Debris at the IF position was studied by a "sniff" setup, which included a QCM, faraday cup, MCP, and witness plate. The fast ion beam slowed by buffer gases demonstrated by the study.
	LBNL	Actinic inspection can detect phase and pit defects, which can not be achieved by DUV inspection.
	IMEC	The current status of AIMS was reviewed.
	Sematech	Showed results and suggested that at 16 nm HP node, actinic inspection is required, which leaves the development of the metrology tool a 6-year time frame.
	SELETE	It reported a new EUV reticle pod, a box-in-box design, which meets the SEMI requirement.

表 Y04

Date	Affiliation	Description of the presentation
2/25	Nikon	Nikon gives its technology roadmap. ArF-immersion + DP will be used for the 22 -16 nm HP nodes, the insertion of EUVL starts at the 16 nm HP node. It also showed the EUV1 performance, COO calculation, results from fundamental R&D works with collaborations with several Japanese research groups.
	ASML	ASML reported its current EUVL status with many field data on machine performance, EUVL process capability, and tool roadmap. 6NXE preproduction tools will be shipped in the 2010-2012 timeframe.
	Cymer	Cymer is the only EUV source supplier, who can show field data. The LPP source will be improved by increasing CO2 gain, high conversion efficiency by a pre-pulse step, H2 purging to eliminate debris deposition.
	LBNL	The most advanced resist evaluation work was lead by Patrick Naulleau of LBNL, he showed the champion resist performance of 2009 by dipole illumination, pseudo phase-shift; and using resist "BBR3" for resist patterning down to 18 nm HP, negative resist inpria down to 15 nm. A new MET with a NA=0.5 upgrading project is ongoing.
	LBNL	Effective test patterns to measure image aberrations was proposed and tested at ALS.
	IMEC	The performance of ASML ADT at IMEC was reported, which included the imaging performance, CDU, overlay, and imaging performance down to 27 nm HP.
	Globalfoundries	Wood reported Globalfoundries' test of using EUVL at the 22 nm HP node operated in the mix-match mode. EUV-contact performed much better than DP-contact.
	SELETE	Selete gave two consecutive talks about using EUVL or DP for different layers at different technology nodes. It showed that M1 of 2X nm HP with a complicated film stack, DP had no common window with the etch processes.

-- Advances in Resist Materials and Processing Technology

Date	Affiliation	Description of the presentation
2/23	IMEC	To study the EUV-RLS tradeoff issue, the EUV resist properties were measured that 1 EUV photon generates ~8 PAG, diffusion length of typical PAG~8nm, underlayer material reduces pattern collapsing but loses contrast.
	IBM	PAG-bound polymers with optimal amount of quenchers were again reported to improve EUV lithographic performance.
	Georgia Tech	Molecular negative-tone resist was demonstrated to have a better performance down to 1X nm HP regime.
	Cornell	Molecular photoresist of star-like was reported for ArF lithography (presumably DP).
	TOK	Promoting acid diffusion by main-chain cleavage in the exposed area improves image contrast.
	Toshiba	Noria(molecular resist) with the modification at side-chains can improve imaging, an example of the approach was shown as the leaving group changes from hydrophobic to hydrophilic.
2/24	Georgia Tech	The surface tension was reduced by reactive rinsing to become more hydrophobic, or substrate modification to enhance the resist adhesion.
	NIST	Acid diffusivity was studied by the neutron reflective method. A newly developed method to study the acid diffusion from the exposed area to the unexposed area directly.
	JSR	Acid amplifier (AA) has been reported again as a mean to increase resist sensitivity. The loss of resolution and thermostability of adding AA were studied.
	Albany	A way to increase the quantum yield without the loss of resolution was achieved by the design of AA is a way that autocatalysis (2nd order reaction) can be effective. An effective 3º alkyl formulation was given as a good candidate.
	IBM	Patterning density as a loading effect to worsen resist patterning was studied by engineering design developing tubes.
	IMEC	Using the LWR power spectral density (PSD) to judge the effectiveness of post-litho processes such as UV-vapor, Ion-beam sputtering, rinse, plasma treatment. It noted that rinse can improved LER by the definition current used for the CD SEM measurement, but its PSD indicated an increase in its low frequency part, which can not be detected by a typical CD SEM measurement.
	C. Mack	The lithoguru described the stochastic nature of photon shot, chemical shot (acid), and dissolution effect.

-- Optical Microlithography

Date	Affiliation	Description of the presentation
2/23	UCBerkeley	Negative index materials may be used for NGL.
	IMEC	New materials to increase the electron mobility (GaAs, InP, InAs, InSb), new devic (STI Ge pMOS), ALD Ge-Ox, Quantum well device, heterojunction, graphene were mentioned as ways to improve the performance of microelectronics. For all these ef IMEC said, "we are not lost, we are exploring."
	Globalfoundries	The concept of design-enable manufacturing was mentioned by Intel, and again by globalfoundries. The strength of the company was mentioned as a great source of lil pattern checking and automated process-aware design.

二、 與會心得

EUVL for the first time became a conference session at the annual advanced microlithography of SPIE. The aims of my trip included to show the current R&D status in Taiwan and to learn the latest progress of EUVL. Since we are not members of SEMATECH or any international EUVL organization, SPIE is the best event for us to learn the latest progress of the lithography technology. It is clear that DP will be used for the 22 nm HP node, while DRAM companies are eager to utilize EUVL for their next generation products. I did not attend the session of alternative litho technology; however, along the meeting it is said that self-assembly contact materials is a likely new technology for contact and via filling. R&D works reported by universities are minor; however, LBNL (using ALS synchrotron light as the EUV source) and SUNY at Albany are two places in the States, actively participating in this event.

三、 考察參觀活動(無是項活動者省略)

No visiting activity.

四、 建議

Some of our EUVL team should attend 2010's meeting for updated EUVL information. We may organize our own workshop to learn more about each other's research.

五、 攜回資料名稱及內容

Agenda and abstracts. See http://spie.org/advanced-lithography.xml for the detail.

六、 其他

無。

附件四

國科會補助專題研究計畫項下出席國際學術會議心得報告

日期：99年7月7日

計畫編號	NSC－98－2120－M－009－007		
計畫名稱	極紫外光(EUV)微影技術從光源建造、光罩、材料、製程到奈米元件可靠度研究(2/3)		
出國人員姓名	鄭秀英	服務機構及職稱	國立高雄大學應用化學系
會議時間	2010年6月22日至2010年6月25日	會議地點	美國夏威夷茂宜島
會議名稱	(中文)2010國際極紫外光微影會議 (英文)2010 International workshop on EUV lithography		
發表論文題目	(中文)(1) 光阻與底層材料的極紫外光釋氣及光化學(會議報告)(2) 計量釋氣分子(壁報) (英文)(1) Outgassing and extreme-ultraviolet photochemistry of photoresist and underlayer materials (oral) (2) Counting outgassing molecules (poster)		

一、參加會議經過

Day 0 (06/21): Travel to Maui.

Day 1 (06/22), speaker prep: I have put on my presentation to the workshop's computer, and tested the presentation to make sure that my presentation file can be run by the workshop's computer. The reception was in the evening.

Day 2 (06/23):

- Keynote -I, Jos Benschop (ASML): ASML presented its roadmap for EUV scanners, and proposed the EUV double patterning will bring the technology to 7 nm HP regimes. Six machines will be shipped in the coming two years. He also mentioned ASML's assessment to masks, sources (LPP and DPP), and resists. The inspection of mask and mask blank is ranked as the number one issue for the realization of EUVL. He also mentioned the upcoming new light source at 6.X nm.
- Keynote -II, Obert Wood (Global foundry): Global foundry presented their current status on mask blank inspection, resist performance, pellicles search, mask flatness, and the reduction of line-edge

roughness (LER) by approaches of underlayer materials, rinse materials, etc.

- EUV sources: Gigaphoton reported its current status as 104W from Sn droplets excited by CO2 laser, expects a 250 W output in 2011. Prof. Dune of UC Dublin reports the latest progress on extracting 13.5 nm light from Tin plasma. EUVA describes the EUV consortium in Japan, and its current status as 100W at IF. Vivek Bakshi summarized the current EUV source status as 60 W, conversion efficiency 2.5 %, and predicted up to 7% might be possible. He noted that a next generation beyond 13.5 nm is undergoing development.
- A section of the next generation EUV sources include Prof. Dunne from UC Dublin and Sasaki from Japan talking about Tb and Gd at λ = 6.5 nm.
- AIMS and Mask blank inspection: Besides the exposure source, there is a need to develop the actinic mask inspection source. Energetiq and NANO-UV gave introduction of their inspection products.
- Contamination section: Selete reported the progress of optical cleaning using oxidation and/or reduction methods. I gave our EUV photochemistry results, and got feedback from global foundry (Obert Wood) and U. Hyogo (Kinoshita).
- My student, Chih-Hua Shao presented “Counting outgassing molecules” in the poster section.

Day 3 (06/24):

- Keynote-III: Nishiyama reported the EUVL development in Japan, he showed the EUVL project from ASET, EUVA, MEXT, to SELETE. He also told the “first” events of EUVL reported by Japan scientists.
- EUVL R&D status: Given by Prof. Denbeaux, he described the research status at Berkley (coming soon a new NA=0.5 exposure tool), NIST, U Illinois, and SUNY CNSE. Prof. Kinoshita presented the facility of U. Hyogo at NewSubaru, he welcomed every one to go there. Prof. Dunne of UC Dublin gave a review of England’s EUVL project (30 researchers, 2 million EU/yr). Prof. CH Lin of NCKU reported Taiwan’s project. Prof. Ahn of Hanyang U. updated Korean’s project, the EUVL project of Korea obtained supports from Samsung for the coming eight years or so.
- EUVL mask: Asahi Glass updated its mask manufacturing status, and reported a new Ru-capping process to reduce the reflectance loss due to Ru-capping. Dr. Goldberg of LBNL gave a thorough review of mask inspection up to date including all reports that can be found from various conferences, symposium, and literatures. Prof. Kinoshita showed the mask inspection tool of U. Hyogo at NewSubaru.
- Resist sections include LER and EUV resist. LER now include the effect from mask LER, as LBNL now focuses on. Chris Mack has been reported on his development on the LER simulation for quite some time, and the key issue to be solved is the capture range of the deprotection region. Prof. Tagawa and Kozawa collaborate, and have developed EUV reaction mechanisms to include the secondary electron’s effect.
- Vivek made a wrap up summary.

二、與會心得

The scope of the workshop as stated by the organizer, Dr. Bakshi, aims on R&D. The participants are mostly R&D scientists from worldwide research institutes and universities; unlike Proc. SPIE where most

reports are contributed by industrial participants. I have more chances to discuss with scientists.

三、考察參觀活動(無是項活動者略)

無

四、建議

EUV lithography is coming. Taiwan should put more R&D effort from universities, research institutes, and industrial companies.

五、攜回資料名稱及內容

Agenda and abstract. See https://www.euvlitho.com/index.php?_a=viewDoc&docId=21&ccUser=393a0aec1952d24011223874497df0a2 for the detail.

六、其他

無。

附件四

國科會補助專題研究計畫項下出席國際學術會議心得報告

日期：99 年 7 月 15 日

<table>
<tr><td>計畫編號</td><td colspan="3">NSC－98－2120－M－009－007</td></tr>
<tr><td>計畫名稱</td><td colspan="3">極紫外光(EUV)微影技術從光源建造、光罩、材料、製程到奈米元件可靠度研究(2/3)</td></tr>
<tr><td>出國人員姓名</td><td>林俊宏</td><td>服務機構及職稱</td><td>成大光電所</td></tr>
<tr><td>會議時間</td><td>99 年 6 月 21 日至
99 年 6 月 25 日</td><td>會議地點</td><td>夏威夷茂宜島</td></tr>
<tr><td>會議名稱</td><td colspan="3">(中文) 2010 極紫外光微影術國際研討會
(英文) 2010 International Workshop on EUV Lithography</td></tr>
<tr><td>發表論文題目</td><td colspan="3">(中文) 台灣在極紫外光微影術研究之現況介紹
(英文) An Overview of EUVL Related R&D in Taiwan</td></tr>
</table>

一、參加會議經過

微影技術是半導體製程技術中最重要的關鍵技術，微影技術的製程能力，影響了電子元件臨界尺寸的定義，進一步影響到產品的效能與成本。光學微影術由於具有極佳的量產能力，目前仍為微影技術中的主流，光學系統的解析能力，與所使用的光源波長成正比的關係，因此，若要提昇光學系統的解析能力，就必需要使用較短波長的光源為曝光光源。圖一顯示 ITRS (International Technology Roadmap for Semiconductors) 2009 年版本[1]的微影技術未來具潛力的解決方案，在 22 奈米節點，EUVL (Extreme UltraViolet Lithography, 極紫外光微影術，波長為 13.5 奈米) 是最具潛力的微影技術之一。

此行到美國夏威夷茂宜島是參加一年一度的 International Workshop on EUV Lithography，此國際研討會是從 2008 年開始，由 EUV Litho, Inc. 的 Dr. Vivek Bakshi

籌辦，至今已是第三屆。本人此次是受研討會之邀請，在 Session 9: EUVL R&D Status 的議程中，介紹台灣在 EUVL 的研究現況，在此議程中，共有美國、日本、歐洲、台灣、韓國等五國的與會代表，負責介紹各自區域的研究現況。

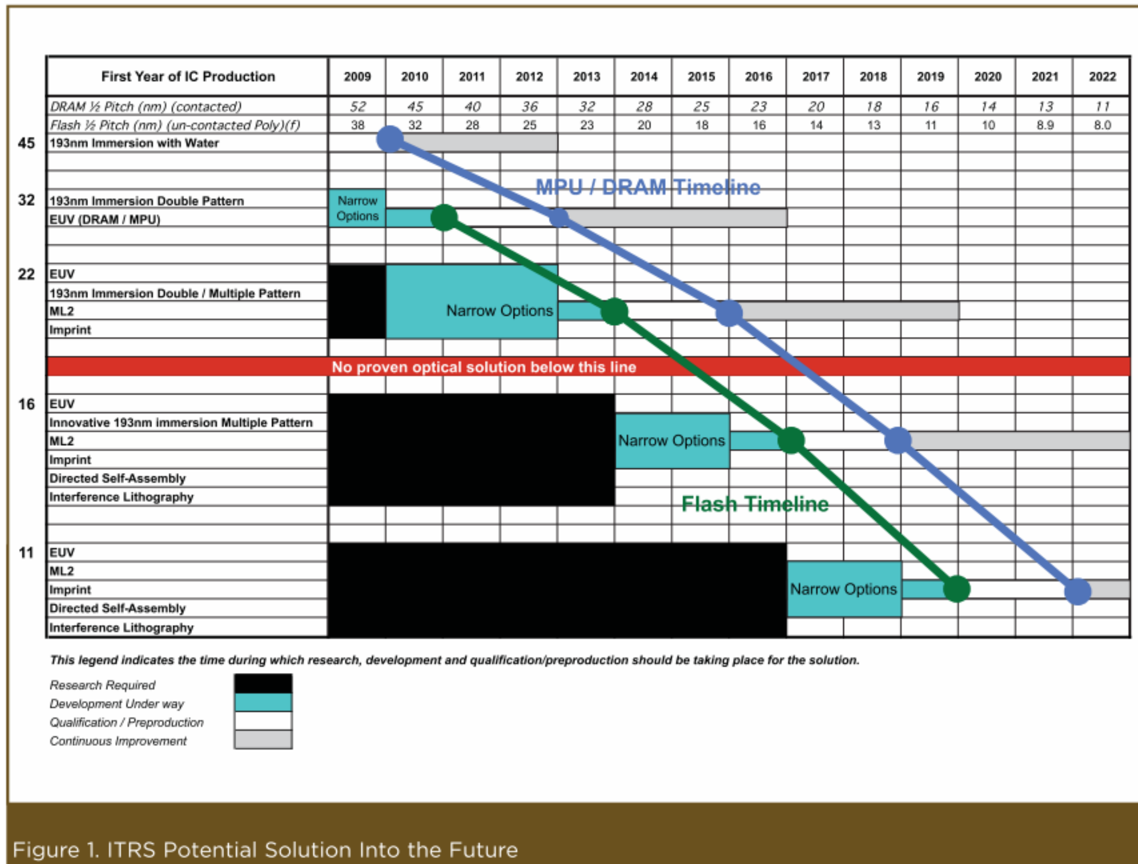


Figure 1. ITRS Potential Solution Into the Future

圖一、ITRS 2009 年版本，微影技術未來具潛力的解決方案。[1]

以下是本研討會的議程，主要共分成 12 個 Session。

6/21~22 是 關於 EUVL 的 Short Courses，包含以下課程，需要另外付費。

- EUV Lithography
- Resist Materials for High Resolution Patterning
- EUV Physics
- Introduction to Optical Lithography

6/22~25 是研討會主體，包含以下項目及議程：

6/22 註冊及歡迎會

6/23

Session 1: Keynote -1

- Keynote -1: EUV: Status and Challenges Ahead, Jos Benschop, ASML, Eindhoven, Netherlands
- Keynote-2: EUV Lithography: Approaching Pilot Production, Obert Wood, GlobalFoudries, Albany, New York, USA

Session 2: High Power EUV Sources

Session 3: Next Generation EUV Sources

Session 4: EUV Sources for Metrology

Session 5: EUV Optics

Session 6: Contamination

Session 7: Poster Session

6/24

Session 8: Keynote – 2

Session 9: EUVL R&D Status

Panelists:

- Greg Denbeaux – USA (University of Albany)
- Hiroo Kinoshita –Japan (Hyogo University)
- Padraig Dunne – Europe (University College, Dublin)
- Chun-Hung Lin – Taiwan (National Cheng Kung University)
- Jinho Ahn – Korea (Hanyang University)

Session 10: EUVL Mask

Session 11: LER

Session 12: EUV Resist

6/25: EUVL Workshop Steering Committee Meeting

二、與會心得

由於 EUVL 是 22 奈米節點最具潛力的微影技術之一。EUVL Workshop 每年舉辦的目的，是集合世界各地在 EUVL 研究的學者與專家，研討 EUVL 在進入高產量半導體量產中，所遭遇的挑戰與解決方案。本次研討的主題包含了高能量 EUV 光源、下世代光源、奈米檢測技術、EUV 光學系統、光罩與系統污染、EUV 光阻與光阻之

邊緣粗造等課題。透過與會的過程，使我進一步瞭解 EUVL 目前最急迫且重要的議題，包含光源、光罩檢測、光阻、及污染等等。因為本人目前正在執行 EUV 干涉式微影技術的研究，University of Hyogo 的 Prof. Hiroo Kinoshita 在 EUVL R&D Program in NewSUBARU 的演講中，提到他們研究關於 EUV 干涉式微影技術的相關資訊，對於我們有相當的參考價值。Osaka University 的 Prof. Seiichi Tagawa 在 Radiation Chemistry of EUV and EB Resists 的演講中，所提到 EUV 和 Ebeam 微影術的光阻之反應機制，亦讓我們對光阻反應機制有更進一步的瞭解。

三、建議

此次在 EUVL Workshop 遇到韓國 EUVL 計畫的總主持人(Director of National EUVL R&D Program) 漢陽大學的安鎮浩(Prof. Jinho Ahn)教授，與他聊天的過程中，他告訴我他們這個 EUVL 計畫，到明天夏天為止，就執行了八年，每一年的的經費總預算為 150 萬美金，經費由韓國政府和多家業界聯合支持，其中韓國政府支持的經費至少占總經費的一半，其研究經費比我們大了一個數量級，整個 EUVL 的研究團隊，並擁有一個專屬的 EUV 同步輻射光束，隨時都能做 EUVL 相關研究。韓國對於先進微影技術的重視，值得我們關注。

四、攜回資料名稱及內容

相關的會議資料，均可在以下 2010 EUVL Workshop 的網頁中查詢。

https://www.euvlitho.com/index.php?_a=viewDoc&docId=21

可查詢資料包含：

- Workshop Proceedings 大部分與會演講者的投影片
- Workshop Agenda 會議議程
- Workshop Abstract Book 會議摘要
- Keynote Talk (Benschop-ASML) Keynote 演講的投影片
- Kenynote Talk (Wood-GLOBALFOUNDRIES) Keynote 演講的投影片

- Kenynote Talk (Nishiyama-SELETE) Keynote 演講的投影片

參考文獻

1. Greg Hughes, “ITRS CHAPTER: Lithography,” FUTURE FAB International **32**, 77 (2002).

附件四

國科會補助專題研究計畫項下出席國際學術會議心得報告

日期：99 年 6 月 25 日

<table>
<tr><td>計畫編號</td><td colspan="3">NSC－98－2120－M－009－007</td></tr>
<tr><td>計畫名稱</td><td colspan="3">極紫外光(EUV)微影技術從光源建造、光罩、材料、製程到奈米元件可靠度研究(2/3)</td></tr>
<tr><td>出國人員姓名</td><td>劉致為</td><td>服務機構及職稱</td><td>台灣大學電機系</td></tr>
<tr><td>會議時間</td><td>99 年 6 月 1 日至
99 年 6 月 2 日</td><td>會議地點</td><td>日本・東京</td></tr>
<tr><td>會議名稱</td><td colspan="3">（中文）高功率電子論談
（英文）Power Electronics Japan Forum 2010</td></tr>
</table>

一、參加會議經過

This 2-day seminar began with a review the main market metrics from devices to applications and current state of the art of the Silicon-based power electronics. It then explored the capabilities of GaN and SiC to disrupt that equilibrium and highlighted the recent developments in a selection of applications.

二、與會心得

Due to the low efficiency of EUV light source, the high power electronic module is necessary to drive. SiC has high power, high efficiency, and high power density. It will be ideal material for EUV source.

Power electronics are currently facing a huge transition as the demand for

efficient power conversion systems is increasing along with the “Green-Tech” introduction. The Green revolution is now impacting all application fields in power electronics pushed by regulations: from low power with the need for improved cell-phone battery chargers; to mid-range where motor control, home appliances, PV inverters, EV/HEV and white goods may consume less energy; to higher power in which train traction, wind turbines and energy T&D are expecting new solutions to reduce conversion losses.

This battle for an efficient world starts at the heart of every system: the power devices. These devices today are mainly based on silicon technology. Silicon diodes and silicon transistors (MOSFET, IGBT, Thyristors…) are the key components and are constantly improving their performance, reliability, life-time and efficiency. However, year-to-year improvements are slowing as they approach maximum theoretical specs.

New materials have emerged in recent years and some may be able to displace existing silicon devices with enhanced characteristics, less loss, higher operation temperature, longer life-time and greater robustness to cycles. SiC was the first technology commercially introduced in the early 2000’s and GaN is now coming to market as well.

三、考察參觀活動(無是項活動者略)

四、建議

五、攜回資料名稱及內容

The agenda is the following:

Day 1

Session 1 (9:00 – 10:30)	Overall Power Electronics market	• Yole Développement: *Power electronics market: a global overview* By Dr Philippe Roussel, Project Manager • STMicroelectronics: *Innovative power device technologies and system solutions for a greener world.* By Jean-Benoit MOREAU, Product Marketing Director • On Semiconductor: *Technology Trends in Energy Efficient Power Semiconductors* By Marnix Tack, Senior Director Power Technology Centre, Corporate R&D
Break (10:30 – 11:00)	–	
Session 2 (11:00 – 12:30)	High Voltage applications	• Yole Développement: *Market for IGBT module in the rail traction* By Brice Le Gouic, Market Analyst • Alstom: *New trends in power system thermal management* by Michel Mermet . R&D innovation technical director PRIMES • Arkansas Power Electronics International, Inc.: *High Performance Silicon Carbide Power Electronics for Extreme Environment Applications* By Jared Hornberger, Director of Manufacturing
Lunch (12:30 – 2:00)	–	
Session 3 (2:00 – 3:30)	EV and HEV	• Yole Développement: *Power electronics market for EV and HEV* By Brice Le Gouic, Market Analyst • R&D Association for Future Electron Devices: *"Japanese National SiC Projects – Past, Present, Future"* By Dr. Hajime Shimizu • Raytheon Systems ltd.: *Power Electronics in More Electric Transportation* By Jim McGonigal, Executive, Power and Control Technologies

Break (3:30 – 4:00)	–
Round table (4:00 – 5:00)	*Green-tech is pushing for improved power devices: what, where, when and how?*
(5:00 – 7:30)	Welcome reception

Day 2

Session 4 (9:00 – 10:30)	SiC power electronics	• Yole Développement: *SiC market: a 10-year projection* By Dr Philippe Roussel, Project Manager • CREE: *"SiC device recent developments"* By Greg Mills, Materials Business Sales and Marketing Manager • SemiSouth: *"SiC J-FET recent developments"* By Jeff Casady, CTO
Break (10:30 – 11:00)	–	
Session 5 (11:00 – 12:00)	SiC and GaN new substrates	• Yole Développement: *Technical trends and market size of SiC and GaN substrates* By Dr Philippe Roussel, Project Manager • Azzurro: *"GaN-on-Silicon: a revolution to make GaN technologies affordable"* By Markus Sickmöller, VP Operations
Lunch (12:00 – 2:00)	–	
Session 6 (2:00 - 4:00)	Silicon wafer market and technology	• Yole Développement: *Silicon wafer market for Power Electronics: CZ, FZ and thin wafers* By Brice Le Gouic, Market Analyst • SUSS MicroTec: *Temporary Wafer Bonding Process Development and Production for Power Device Manufacturing* By Bill Crouch, Product Manager • Topsil: *In Search of Excellence: Pushing the Limits of Silicon* By Jørgen Bødker, VIP, Logistics, Sales and Marketing • EV Group: *Cost effective approach for thin wafer handling process*

		optimization By Yuichi Otsuka, Representative Director
Round table (4:00 － 5:00)	*How fast could SiC and GaN take market shares over silicon*	

六、其他

國科會補助專題研究計畫項下出席國際學術會議心得報告

日期：99 年 7 月 15 日

<table>
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<tr><td>出國人員姓名</td><td>顏志展</td><td>服務機構及職稱</td><td>國立交通大學電子工程學系及電子研究所 碩士班研究生</td></tr>
<tr><td>會議時間</td><td>99 年 6 月 13 日
至
99 年 6 月 14 日</td><td>會議地點</td><td>夏威夷,檀香山</td></tr>
<tr><td>會議名稱</td><td colspan="3">（中文）2010 矽奈米電子研討會
（英文）2010 Silicon Nanoelectronics Workshop</td></tr>
<tr><td>發表論文題目</td><td colspan="3">（中文）極紫外光照射對非揮發性記憶體產生之傷害
（英文）Extreme Ultra-Violate Exposure Induced Damages on Non-Volatile Memories</td></tr>
</table>

一、參加會議經過

本研討會錄取學生投稿之論文為壁報論文，在出國前需準備海報及一分鐘英文口頭報告。研討會期間為6/13～6/14 共兩天，學生幾乎都待在研討會會場，並且專心聽講，紀錄各篇論文重點。6/14 上午十一點三十分，學生上台進行一分鐘口頭報告招攬聽眾。6/14 下午一點三十分至三點三十分，學生站在自己論文海報前面，針對對我論文有興趣或是提出疑問的人，用英文回答他們的疑惑。

二、與會心得

以本次研討會錄取的論文比例來說，學術界的論文數量比業界的多出不少，這可能是業界論文大部分都是被 VLSI 研討會所錄取的關係。而學術界錄取的論文又以日本及中國為最多，台灣則主要錄取為海報的部份，因此還需要再加油。整體來說，會議進行的時間控制的還不錯，每段皆有在預定的時間內結束。

以下說明此研討會中幾篇令我印象比較深刻的論文重點：

新加坡大學 Genquan Han 等人發表引入 N^+ pocket 到 TFETs 元件，介於 source 和 channel 之間，稱作 Dopant Profile Steepening Implant (DPSI) 的方法，可以得到陡峭的 source 摻雜輪廓來提高橫向電場，以致於可以大大提昇 drain current，大約是 15 uA/um，這對於 TFETs 元件是極有幫助的。我們知道 TFETs 元件相對於傳統 MOSFETs 元件的優點就是它有極低的 subthreshold swing（SS<60 mV/decade)且 supply voltage 可以低至 0.5 V，不過最大的罩門是 low I_{on}，因此運用此篇提出的結構可以改善它的主要問題。TFETs 元件的研究在此次研討會上了蠻多篇，這篇是我

認為比較不錯的改善，所以提出來分享。

日本的 NIRC 和 AIST 研究機構提出一個新穎的方法可製作出小於 10nm 直徑的 Si nanowire FETs 元件。首先利用 SOI 的基板沈積一層 oxide layer 來當作 hard mask，接著用 EBL & RIE 先蝕刻出 SiNW channel 的圖形，經過 H_2 的 anneal 後，利用高溫(900 度)低壓的 O_2 氣體來蝕刻 Si channel，又因為 O_2 的高 Si/SiO_2 選擇比，因此上方經 oxide layer 保護不被蝕刻，側邊未被保護的則可蝕刻出極小的 dimension。對於同樣的 gate length，此 SiNW FETs 元件相較於 SOI-FETs 元件有比較低的 subthreshold swing，顯示抑制了短通道效應的效果。由於 Si nanowire FETs 元件製作是我們實驗室學長在做的主題，相較於學長先挖溝槽再蝕刻成 Si nanowire，我們在這看到了不同的新方法，相當有趣。

北京大學發表利用 Nitrogen doped SiO_x 來當作 RRAM 的 active layer，可產生比較多的 traps 且弱化 SiO_x 裡的化學鍵結，如此一來適合 copper atoms 的遷移及擴散，因此 switching volatage 可大大地降低，此 $Cu/Si_xO_yN_z/W$ 結構的元件在 80 度的 set～1V， reset～0.4V。HRS 及 LRS 在 Retention 表現上不管是室溫或 80 度皆十分穩定。Endurance 的表現在 80 度時，HRS 及 LRS 在測試中雖有些許 fluctuation，不過經過 50 cycles 後仍然穩定。RRAM 是現今很紅的非揮發性記憶體，相較目前都以 transition metal oxide (TMO)來當作 active layer，此篇運用非金屬性的 $Si_xO_yN_z$ 來作 RRAM，是蠻新穎的方法。

三、考察參觀活動(無是項活動者略)

無

四、建議

由於此研討會每年都是接在 VLSI 研討會前，因此到了第二天會出現出席率明顯減少的情形，使得會場變得比較冷清，提問的人數也沒 VLSI 研討會來的熱烈，建議有參加此研討會的人應當保有學習的態度參與到研討會結束。

此研討會同時間只有一個 session 在進行，因此不會碰到同時有兩篇論文皆想聽的問題。會場也提供桌子方便參加者紀錄重點及閱讀論文。研討會時間幾乎都是從一大早開始到晚上五點左右，建議與會者每天一定要養足精神，才能有清晰的思緒吸收研討會的論文內容。

五、攜回資料名稱及內容

2010 SNW 研討會論文集紙本一本，內容包含大會的議程手冊、錄取的論文摘要等資料，大會無提供論文集的電子檔案。

六、其他

無

國科會補助專題研究計畫項下出席國際學術會議心得報告

日期：99 年 7 月 15 日

計畫編號	NSC－98－2120－M－009－007		
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出國人員姓名	顏志展	服務機構及職稱	國立交通大學電子工程學系及電子研究所 碩士班研究生
會議時間	99 年 6 月 15 日至 99 年 6 月 17 日	會議地點	夏威夷,檀香山
會議名稱	（中文）2010 超大型積體電路技術研討會 （英文）2010 Symposium on VLSI technology		
發表論文題目	無		

一、參加會議經過

此研討會接續學生所參加的 SNW 研討會，是一個國際頂級的會議。老師希望學生也能參與這個國際級的饗宴，增廣見聞，因此報名了此研討會。研討會期間為 6/15～6/17 共三天，學生幾乎都待在研討會會場，專心聽講並紀錄各篇論文重點。

二、與會心得

以此研討會錄取的論文比例來說，主要是業界發表的論文，所以在會場聽到的幾乎都是最先進的技術及製程，對於碩士生的我在瞭解上有點吃力。此研討會發問的踴躍度很高，常常時間還不夠用，到休息時間會看到上台報告者仍被人圍著問問題，這樣的研討會才真正有達到互相討論的效果，很不錯。除了聆聽錄取論文的作者上台報告外，還有另一個會議是台上坐著一些重量級的人士，針對半導體未來發展提出自己的看法，當然台下的人也可以跟他們討論甚至是挑戰他們的言論，是個十分有趣的活動，令我印象深刻。整體來說，會場的氣氛的確與我參加過的會議不相同，可以感受到頂級會議的氣氛。

以下說明此研討會中幾篇令我印象比較深刻的論文重點：

韓國 S.J. Choi 等人發表新穎無 Spacer 結構的 dopant segregated schottky barrier (DSSB) TFT SONOS 元件可運用於 3D TFT 邏輯元件與快閃記憶體元件。其元件寫入 V_t 的分佈比傳統 TFT SONOS 元件還來的好，program speed 也比傳統優異，因為傳統 TFT SONOS 元件主要受限於 poly-Si channel 有 grain boundary effect 的問題，而此元件則可以靠 DSSB S/D 端來提供電子，改善 program speed。此外，Retention 和 Endurance 在不同寫入條件下也有不錯的 performance。利用 S/D 端的 bandgap 調整來

製作 TFT SONOS 元件是我們實驗室學長也有在做的研究，這篇除了先 implant 再 silicidation 與我們做的步驟相反之外，其餘都很類似，只是學長的論文比較晚發表，否則是有機會被 VLSI 錄取的。

美國 SEMATECH 公司提出利用 Al implant silicide integration 的方法，可使 fin 小於 20nm 的 n-FinFETs 元件，降低其 S/D resistence 而增進 19%的 drain current。因為 Al implant 可以降低 n-Si contact 的 schottky barrier height 達 0.4eV，改善了原本以 Pt 為基底的 NiPtSi 矽化物其高的 electron barrier 而提昇電阻的問題，使其 electron barrier height 調整往 conduction band 移動。此論文建議 NiPtSi 適合運用在 p-FinFETs 而 Al implanted NiPtSi 則適合運用在 n-FinFETs。這篇會讓我提出來是因為我們實驗室有在研究利用 Carbon implant 來改善 S/D 端的 resistence，此篇運用 Al implant 讓我看到新的觀點。

日本 NIRC-AIST 研究機構發表第一個成功用 Ge nitride interfacial layer (NIL)作成的 Metal Gate/High-k Ge-nMISFETs 元件，相較於一般常用的 oxide interfacial layer (OIL)，由於它的一些主要問題如 EOT 的 scale down 及在製程中很難和 high-k 材料相容因為 chemical 和 thermal 的不穩定性，所以提出了以 NIL 來取代 OIL。與 OIL 相比，NIL 可以抑制 positive fixed charges 的產生和減少 high-k/Ge gate stacks 裡的 electron trapping centers。作者利用 NIL 搭配 HfO_2 作成的 Ge-nMISFETs 元件可得到比 Si-MOSFETs 還要好的電性，如 SS 只有 74mV/dec 及 870cm^2/Vs 的高 electron mobility。Ge-based 的 MOSFET 是我們實驗室接下來要研究的主題，此篇提供我們研究的一些目標和方向。

三、考察參觀活動(無是項活動者略)

無

四、建議

由於此研討會參與的人數眾多，台下提供給聽者的只有椅子，不像 SNW 研討會有桌子可以方便聽者閱讀和紀錄重點或是使用筆電，建議主辦單位以後可以考慮此因素。

此研討會同時間有二個至三個 session 在進行，不過每個 session 的會場都緊鄰著，不會有找不到會場的麻煩，建議聽者最好前一天就先看會議議程表，知道自己想聽的論文及其場地，才不會當天顯得匆忙。另外，研討會時間幾乎都是從一大早開始到晚上五點左右，建議與會者每天一定要養足精神，才能有清晰的思緒吸收研討會的論文內容。

五、攜回資料名稱及內容

2010 VLSI 研討會論文集紙本一本及 CD 光碟一片，內容包含大會的議程手冊、錄取的論文摘要等資料。

六、其他

無

附件四

國科會補助專題研究計畫項下出席國際學術會議心得報告

日期：99 年 6 月 20 日

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出國人員姓名	李勃學	服務機構及職稱	交通大學電子研究所
會議時間	99 年 6 月 15 日 至 99 年 6 月 17 日	會議地點	美國檀香山市希爾頓飯店
會議名稱	(中文)2010 超大型積體電路技術及元件技術研討會 (英文)2010 Symposia on VLSI Technology and Circuits		
發表論文題目	(中文) (英文)		

一、參加會議經過

本研討會屬於國際級頂尖之超大型積體電路技術的研討會，研討會期間是6/15~6/17 號，在這段期間學生相當珍惜這寶貴的經驗，與會期間幾乎全程參予會議，並且仔細聆聽報告並且勤做筆記。其間並與國際人士做意見交換。

二、與會心得

本討會為超大型積體電路之國際研討會，蒐羅了世界頂尖各國在超大型積體電路中最先進的研究，投稿之國家包括美國，日本為大宗並且也有歐洲各個研究機構，台灣以及韓國也各有幾篇論文。與會的人士來自世界各國，但主要以美國，日本為

主。

本次研討會所蒐羅之論文，從最先進的 CMOS Technology、SOI 技術、3D integration 等，到記憶體元件，如 NAND Flash memory、RRAM、PCRAM、MRAM，另外還有新穎的 Device structure、 GeMOSFETs、Heterogeneous integration 共分為 22 session。。業界論文數跟學界論文大約各半，但絕大部分的論文都有相當改進或是良好的 Performance，或是有些世界級的紀錄。整體來說整個會議進行的十分順利流暢，延誤脫時的情形鮮少發生。

以下說明研討會進行中，幾篇令我映象深刻的 Paper 重點內容

IBM 發表了 Gate all around 結構之 Silicon nanowire 並且將元件的尺寸微縮到 3nm，此種 GAA 的結構使用 High-k/metal gate 的結構，並且達到高品質且平滑的結晶性 NW channel。另外此論文也使用此種 GAA 在 NW 從 3-14nm 直徑以及通道長度從 25nm 到 55nm 的元件，製作出 ring oscillators。並且在小於 10nm 的元件之中觀察到了 Self-heating 現象。另外 Strain 的技術也證實可以應用在 SW 之上。由於實驗室對 GAA 的元件有一定程度的研究。此篇論文將可以成為我們實驗室的參考方向。

另外韓國研究單位 *EECS, KAIST, Daejeon* 的 Sung-Jin Choi, Jin-Woo Han, Sungho Kim 等人使用了 Dopant segregated Schottky barrier(DSSB) 之 TFT SONOS 元件應用在 3D IC 上面的可能性，也因 DSSB 的結構減少了 S/D 的阻抗使得驅動電流得以有 300%之增加而不犧牲漏電流。另外 DSSB 的結構可以使得電子得到額外的動能能量，故 DSSB 元件可比一般性的元件有更快的寫入速度。由於實驗室最近也有學長使用類似的 S/D 結構，希望製作出有相同效果的 TFT SONOS 元件。此篇論文給予我們很大的鼓舞，並證實了類似的 S/D 工程有機會做出 performance 更好的 SONOS

元件。

另外台灣旺宏公司也在此次研討會中發表了3D的記憶體技術，此篇論文中使用了75nm helf-pinch之技術製作出8-Layer 3D Vertical-Gate (VG) TFT NAND Flash。此技術首先堆疊了多層的TFT Poly-Si/SiO_2，向下蝕刻之後，可在側壁堆疊BE-SONOS的結構並且完成Vertical-Gate的TFT，並且每一個元件都有雙閘極。在此篇論文雖使用了75nm half-pinch 但作者也使用了TCAD 模擬在25nm half-pinch之下雖然channel lateral dimension 只有8nm左右。但是讀取的電流卻不會有大幅度的下降。這是因為有效通道長度被Z方向的厚度所主宰。故可以在這狀況之下保持讀取電流之大小。

三、考察參觀活動(無是項活動者略)

四、建議

由於這次參加的VLSI研討會包含了許多項目，但是在短短的三天之中需要把這些主題講完，所以說必須分成兩個會場。很多有興趣的主題要是在一起同時演講時就必須作一些取捨。另外演講者的投影片內容並沒有一並給予與會的人員。此次研討會也是從一大早就開始，所以說保持著一個清醒的頭腦來聆聽演講者也是相當的重要，可以在一大早或是下午研討會開始時喝一些提神的飲料如咖啡、茶等。有助於更加專心的聆聽研討會內容。

五、攜回資料名稱及內容

2010 VLSI研討會論文集紙本一本，內容包含大會的議程手冊、錄取的論文摘要等資料，以及論文集的電子檔案。

六、其他

國科會補助計畫衍生研發成果推廣資料表

日期:2011/01/07

<table>
<tr><td rowspan="3">國科會補助計畫</td><td colspan="2">計畫名稱: 極紫外光(EUV)微影技術從光源建造、光罩、材料、製程到奈米元件可靠度研究(2/3)</td></tr>
<tr><td colspan="2">計畫主持人: 黃遠東</td></tr>
<tr><td>計畫編號: 98-2120-M-009-007-</td><td>學門領域: 儀器設備與發展</td></tr>
<tr><td colspan="3">無研發成果推廣資料</td></tr>
</table>

98 年度專題研究計畫研究成果彙整表

計畫主持人：黃遠東	計畫編號：98-2120-M-009-007-
計畫名稱：極紫外光(EUV)微影技術從光源建造、光罩、材料、製程到奈米元件可靠度研究(2/3)	

成果項目			量化			單位	備註（質化說明：如數個計畫共同成果、成果列為該期刊之封面故事...等）
			實際已達成數（被接受或已發表）	預期總達成數(含實際已達成數)	本計畫實際貢獻百分比		
國內	論文著作	期刊論文	0	0	100%	篇	
		研究報告/技術報告	0	0	100%		
		研討會論文	0	0	100%		
		專書	0	0	100%		
	專利	申請中件數	0	0	100%	件	
		已獲得件數	0	0	100%		
	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（本國籍）	碩士生	0	0	100%	人次	
		博士生	0	0	100%		
		博士後研究員	0	0	100%		
		專任助理	0	0	100%		
國外	論文著作	期刊論文	9	0	40%	篇	
		研究報告/技術報告	0	0	100%		
		研討會論文	11	0	40%		
		專書	0	0	100%	章/本	
	專利	申請中件數	0	0	100%	件	
		已獲得件數	0	0	100%		
	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（外國籍）	碩士生	10	0	100%	人次	
		博士生	8	0	100%		
		博士後研究員	0	0	100%		
		專任助理	1	0	100%		

其他成果 (無法以量化表達之成果如辦理學術活動、獲得獎項、重要國際合作、研究成果國際影響力及其他協助產業技術發展之具體效益事項等，請以文字敘述填列。)	本計畫由零開始，啟動台灣的 EUVL 研究。在第二年計畫完成後，目前主要的成果效益包括: (1)成功建構包括高精度 EUV 反射儀，配備四極質譜儀的光阻釋氣分析系統以及干涉微影系統等重要設備，並建立相關實驗分析技術。 (2)上述分析技術與設備，目前均有國內半導體廠實際委託，合作或參與研究，並借用本計畫所建構的儀器與技術在同步輻射中心進行研究分析。 (3)國內半導體廠已著手建構類似設備，進行 EUVL 相關研究。 (4)本計畫已投入超過 30 位師生從事 EUVL 相關研究，並已有超過 10 篇的碩士論文產生，期刊論文陸續發表中。 根據上述成果，計畫成員自評本計畫大致依據原規劃進行，並達成預期目標，特別是延伸的產業應用。本計畫將根據第一期計畫成果，配合未來產業的實際需求，提出第二期的國家奈米學研計畫。

	成果項目	量化	名稱或內容性質簡述
科教處計畫加填項目	測驗工具(含質性與量性)	0	
	課程/模組	0	
	電腦及網路系統或工具	0	
	教材	0	
	舉辦之活動/競賽	0	
	研討會/工作坊	0	
	電子報、網站	0	
	計畫成果推廣之參與（閱聽）人數	0	

國科會補助專題研究計畫成果報告自評表

請就研究內容與原計畫相符程度、達成預期目標情況、研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）、是否適合在學術期刊發表或申請專利、主要發現或其他有關價值等，作一綜合評估。

1. 請就研究內容與原計畫相符程度、達成預期目標情況作一綜合評估

■達成目標

□未達成目標（請說明，以 100 字為限）

□實驗失敗

□因故實驗中斷

□其他原因

說明：

2. 研究成果在學術期刊發表或申請專利等情形：

論文：■已發表 □未發表之文稿 □撰寫中 □無

專利：□已獲得 □申請中 ■無

技轉：□已技轉 □洽談中 ■無

其他：（以 100 字為限）

台灣積體電路製造公司研發投資 93 萬。

Nissan Chemical Industries, Ltd.研發投資 30 萬。

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3. 請依學術成就、技術創新、社會影響等方面，評估研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）（以 500 字為限）

本計畫由零開始，啟動台灣的 EUVL 研究。在第二年計畫完成後，目前主要的成果效益包括:

(1)成功建構包括高精度 EUV 反射儀，配備四極質譜儀的光阻釋氣分析系統以及干涉微影系統等重要設備，並建立相關實驗分析技術。

(2)上述分析技術與設備，目前均有國內半導體廠實際委託，合作或參與研究，並借用本計畫所建構的儀器與技術在同步輻射中心進行研究分析。

(3)國內半導體廠已著手建構類似設備，進行 EUVL 相關研究。

(4)本計畫已投入超過 30 位師生從事 EUVL 相關研究，並已有超過 10 篇的碩士論文產生，期刊論文陸續發表中。

根據上述成果，計畫成員自評本計畫大致依據原規劃進行，並達成預期目標，特別是延伸的產業應用。本計畫將根據第一期計畫成果，配合未來產業的實際需求，提出第二期的國家奈米學研計畫。