行政院國家科學委員會專題研究計畫 成果報告

以 I-line 雙重曝影技術研製次 100 奈米線寬穿隧式場效電晶體
研究成果報告(精簡版)

計 畫 類 別 ： 個別型
計 畫 編 號 ： NSC 98-2221-E-009-160-
執 行 期 間 ： 98 年 08 月 01 日至 99 年 07 月 31 日
執 行 單 位 ： 國立交通大學電子工程學系及電子研究所

計 畫 主 持 人 ： 黃調元

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處 理 方 式 ： 本計畫可公開查詢

中 華 民 國 99 年 10 月 20 日

行政院國家科學委員會補助專題研究計畫成果報告

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※以 I-line 雙重曝影技術研製次 100 奈米線寬穿隧式場效電晶體※

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計畫主持人：黃調元 教授

共同主持人：

計畫參與人員：蔡子儀、簡敏峰、許家維、林庭輔

執行單位：國立交通大學電子工程研究所

中 華 民 國 99 年 7 月 31 日

以 I-line 雙重曝影技術研製次 100 奈米線寬穿隧式場效電晶體

“Fabrication and characterization of sub-100nm tunneling field-effect transistors with I-line double patterning lithography technique”

計畫編號：NSC98-2221-E-009-160-

執行期間：98 年 8 月 01 日 至 99 年 7 月 31 日

主持人：黃調元 交通大學電子工程系教授

一、摘要

中文摘要

在本報告中，我們發展出一種新穎的技術可利用 i 射線(i-line)光學步進機來製作次世代小於 100 奈米的閘極圖形，並應用其來製作元件。這技術包含了兩次光學微影以及後續蝕刻製程。因為它不會受到如同一般製程中的繞射效應，其複雜製程帶來的好處是突破一般 i 射線光學微影方法的解析度極限(~0.3μm)。這技術的解析度在本報告中已被證實可進展到約 100 奈米左右。在本報告中非對稱源極/汲極元件-穿隧式場效電晶體(TFET)也用此技術來製作與分析。

關鍵字：微影、雙重曝影、解析度提升、穿隧式場效電晶體。

英文摘要

In this work, we have developed a novel double patterning technique utilizing an i-line stepper for the formation of sub-100nm gate patterns and implemented this technique to the fabrication of devices. This technique consists of 2-step lithography and following etch process to form the gate patterns. Reward for the complicated process steps is the shrinkage of resulted patterns beyond the resolution limit of the conventional i-line lithographic method (~0.3μm), since this technique doesn’t suffer the diffraction effect encountered in conventional process. Resolution capability of this technique has been confirmed to improve at least to 100nm in this thesis. Asymmetrical source/drain structure, such as tunneling field-effect transistors (TFETs), was fabricated with this technique and characterized in this work.

Keywords: lithography, double patterning, resolution enhancement, tunneling FET.

二、計畫的緣由與目的

The well-known Moore’s Law states that the number of transistors on an integrated circuit (IC) chip will double every 18 months [1]. Since the advent of IC manufacturing, this law has been in force for decades. In order to keep up with the Moore’s Law, shrinkage in device dimensions is indispensable, which also promotes device density, operation speed, and chip functionality. In other words, for better performance and cheaper manufacturing cost, the continuous scaling of the devices is evitable. To keep pace with the law, it requires innovation to overcome several fundamental physical barriers lying ahead, and first of all is to extend the photolithography limit. According to the Rayleigh’s criterion, the resolution, R, of a photolithography technique can be expressed as follows [2]:

$$R = {k_1 \lambda}/{NA} \quad \text{..........................(eq.1)},$$

where k_1 is a system constant, λ is the wavelength of incident light, and NA is the numerical aperture of the lithography system. Based on such criterion, we could adjust the three factors of the criterion so as to boost the resolution of a lithography system [3-5]. Nowadays, state-of-the-art mass production of nano-scale ICs employs the immersion lithography tools with the 193 nm excimer laser as the exposure light source, which has been widely adopted in 300-mm wafer fabrication for manufacturing chips with sub-100 nm technology node. However, the extremely high cost on the lithography tool and related processes hinders these tools from being used in the laboratories of universities. On the other hand, electron-beam lithography [5] is therefore far more popular in these environments for generating sub-100 nm patterns, although the throughput is dramatically limited, and thus its proliferation in mass manufacturing is prohibited. Recently, it was reported that the double exposure (DE) technique [6], and double patterning (DP) technique [7-9] were being considered as promising candidates to extend lithography processing beyond the 45 nm node at k_1 factors below 0.30. DP is a process that splits one patterning step into two to relax the imaging fidelity requirements for small technology nodes. The most common form of DP typically decomposes a target layout pattern into two separate photomasks employing two exposure steps and subsequent etching steps. Consequently, the dimensions of the final target patterns can easily break the resolution limit with single exposure. Usually I-line stepper is not capable of sub-100 nm pattern generation owing to its long exposure wavelength of 365 nm. In this work, we develop a DP technique with conventional I-line stepper to generate sub-100 nm photoresist (PR) patterns with the goal to fabricate nano-scale MOSFETs. Although this technique consists of two times the lithographic and subsequent etching steps, we show that the DP method could reliably generate line patterns with dimension down below 100 nm. Our results indicate that the method developed in this work is promising for both the research works carried out at universities and for practical manufacturing in terms of much lower cost (as compared with state-of-the-art DUV lithography) and decent throughput.

In addition, TFET is an inherently asymmetrical device and usually need more mask counts than conventional MOSFETs to fabricate, it is thus well suited for the DP scheme reported in this work as far as nano-scale gate length is concerned.

三、研究方法及成果

研究方法

A: Development of double patterning with i-line stepper

For all lithographic steps carried out in this work, we used an I-line stepper (Canon FPA-3000i5+) to generate the photoresist (PR) patterns. Figure 1 shows an example of the proposed process scheme for forming the test patterns. The poly-Si film was deposited by a low-pressure chemical vapor deposition (LPCVD) on a six-inch Si substrate capped with a thermal oxide layer (100 nm) as shown in Fig. 1 (a), followed by the first lithographic step.

After the generation of the first PR patterns, the regions of exposed poly-Si layer were etched away with a reactive plasma step, as shown in Fig. 1 (b). After the first PR removal, the next lithographic step was employed to generate the second PR patterns which covered portions of the poly-Si layer remaining on the surface of the substrate, followed by a reactive plasma etching step to complete the final poly-Si structure [Fig. 1 (c)]. With suitable design and process control, the dimension of final poly-Si line patterns [Fig. 1 (d)] could be scaled well below 100 nm. Both in-line and cross-sectional scanned electron microscopic (SEM) techniques were used to characterize and verify the resultant PR and etched poly-Si structures.

B: Device fabrication of pMOSFETs

PMOSFETs were fabricated on 6-inch n-type Si wafers with conventional local oxidation of silicon (LOCOS) isolation. Thermal gate oxide of about 3 nm was subsequently grown in an N_2O ambient, followed by the deposition of 200 nm undoped poly-Si and gate implantation (BF_2^+, 10 keV, $5\times10^{15}cm^{-2}$). Afterwards a LPCVD tetraethoxysilane (TEOS) oxide of 50 nm was deposited to serve a hard mask layer, as shown in Fig. 2 (a). After gate definition using the DP method (Fig. 1) as shown in figs. 2 (b) and 2 (c), shallow source/drain (S/D) extension regions were formed by implanting BF_2^+ (10 keV, $5\times10^{14}cm^{-2}$), as shown in Fig. 2 (d). After forming a 100 nm TEOS sidewall spacer, deep S/D junctions were formed by implanting BF_2^+ (15 keV, $5\times10^{15}cm^{-2}$), and then annealed at 1000 ℃ for 5 seconds as shown in Fig. 2 (e). Finally, a conventional AlSiCu metallization was carried out to form the metal pads (Fig. 2 (f)). Electrical characterizations were performed using an HP 4156 system.

C: Device fabrication of TFETs

TFETs were fabricated on 6-inch p-type Si wafers with conventional local oxidation of silicon (LOCOS) isolation without anti-punchthrough or threshold voltage (Vth) adjustment implant. 2.5 nm N_2O thermal gate oxide and 100nm in-situ n-doped poly-Si were formed by vertical furnaces. After gate definition using the DP method, n-type drain formation was performed with As^+ implantation at 10 keV and $5x10^{14}$ cm^{-2}. A BF_2^+ implantation (10 keV and $1x10^{15}$ cm^{-2}) was used to form the p-type source. A 1000 ℃ spike rapid thermal anneal (Spike RTA) was subsequently applied for dopant activation. Finally, a conventional AlSiCu metallization was carried out to form the metal pads.

研究成果

A: Feasibility of the DP process

In-line SEM images of several etched poly-Si structures with the designed pattern width of 100 nm are shown in Fig. 3. These images were taken from different locations of a six-inch Si wafer. The range of the measured pattern width is distributed from 96 to 106 nm in Fig. 3. These results confirm the feasibility of the DP method for forming structures having dimension as small as 100 nm with an I-line stepper. However, we found the fluctuation in the measured line width of the patterned poly-Si structures becomes large as the nominal width is smaller than 100 nm. Such finding is reasonable when considering the overlay limit of the exposure system which is 45 nm. Since the dimension of the patterned lines is determined by the overlap region of the two gate masks, the

misalignment of the two masks would definitely affect the control of the critical dimension.

B: Device characteristics

Next we shift our attention to fundamental electrical characteristics of the fabricated devices. Typical transfer characteristics of a pMOSFET with channel length of 200 nm and channel width of 10 μm are illustrated in Fig. 4 with drain induced barrier lowering (DIBL) of 166 mV/V, subthreshold swing of 77 mV/dec. Cross-sectional SEM of the device is illustrated in Fig. 5. Figures 6 (a) and (b) show the threshold voltage (V_{TH}) and DIBL, respectively, of the devices as a function of the gate length. Overall the device performance is decent. Nonetheless, poor device characteristics featuring significant punchtrough are observed for devices with channel length of 100 nm or below. This is partly ascribed to the non-optimal implant conditions used in the device fabrication. During the course we've also found the occurrence of the necking phenomenon at the isolation edge as shown in Fig. 7. Such phenomenon is also responsible for the leaky characteristics of the short-channel devices. We are currently investigating the cause of the necking, trying to resolve the issue and pushing the channel length of the fabricated devices down below 100 nm.

The dependence of Id on channel length is quite different between conventional MOSFETs and TFETs. For the latter devices, the current is independent of channel length, although in a related simulation study [10], the results pointed out the conduction current would drop slightly due to the higher resistance of longer channel. Figure 8 shows channel-length dependences of TFETs. For all the measurements on the TFETs, we define the n^+ region as drain and the p^+ region as source. As can be seen, the characteristics of the TFET devices, essentially show little dependence on the channel length. The transfer curves of a TFET with gate length of 0.2 μm are shown in Fig. 9. In the figure Vds is fixed at -1.25 V, and the drain bias is increased from -0.25 V to 0.75 V with step of 0.25 V. We can see in the figure that these transfer curves are parallel and shift with respect to the adjacent ones by 0.25 V, consistent with the trend reported by Wang et al. [11]. The min SS denotes the minimum value of SS in the entire substhreshold region, the avg SS denotes the average value of SS in the range of drain current between 10^{-11} A and 10^{-9} A. In the figure the lowest min SS and ave SS are 231 mV/dec and 367 mV/dec, respectively.

四、結論與討論

In this work we present the results of developing an I-line DP technique for generating sub-100 nm patterns which are much finer than the resolution capability of the conventional I-line lithography. The feasibility of this approach is confirmed through the in-line and cross-sectional SEM characterization. Although an additional lithographic step and an additional etching step are required in the process, the overall throughput is still much higher than the e-beam lithography, while the process cost could be significantly lower than the DUV lithography. Finally, this approach has been applied for device fabrication. The fabricated pMOSFETs with 200 nm channel length have been characterized and confirmed with good characteristics and control over the short-channel effects. With suitable modification of layout

design, we believe the necking issue mentioned above will be settled completely for the sub-100 nm device fabrication. These results clearly evidence the usefulness of the proposed I-line DP technique for nano-scale device fabrication and study. In addition, TFETs with on/off ratio of around 4~5 orders in magnitude was achieved, and the minimum SS was about 230~260 mV/dec. The poor SS characteristics was ascribed to non-abrupt dopant profile.

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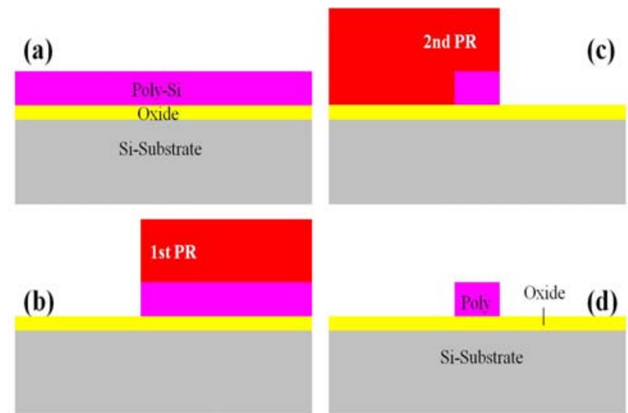
1. IEDMS, 2009, 303.
2. SNDT, 2009, NF20.
3. SNDT, 2010, NC06.
4. Microelectronics Reliability, 2010, p.584.



5. JVST B (under review), 2010.

Fig. 1 Schematic of the double patterning process. (a) Deposition of poly-Si on a Si wafer capped with thermal oxide. (b) Generation of the first PR patterns and etching of the poly-Si with subsequent etch step. (c) Generation of the second PR patterns and etching of the poly-Si with subsequent etch step. (d) Completed poly-Si structure after the DP process.

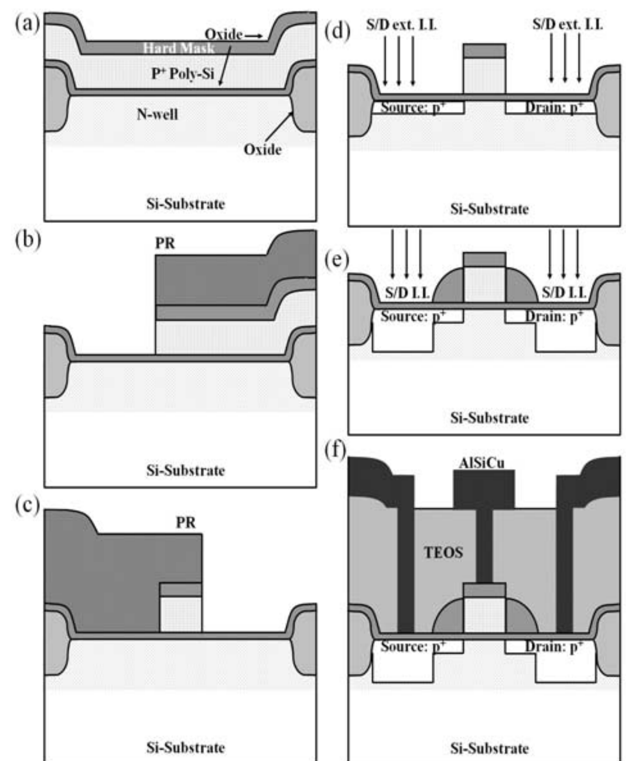


Fig. 2 Process flow of a pMOSFET with the DP method. (a) Deposition of TEOS and poly-Si layers onto the gate oxide (active region) and field oxide (isolation region). (b)

First gate pattern definition. (c) Second gate pattern definition. (d) S/D extension implantation. (e) Spacer formation and deep S/D implantation. (f) Formation of contact holes and test pads.

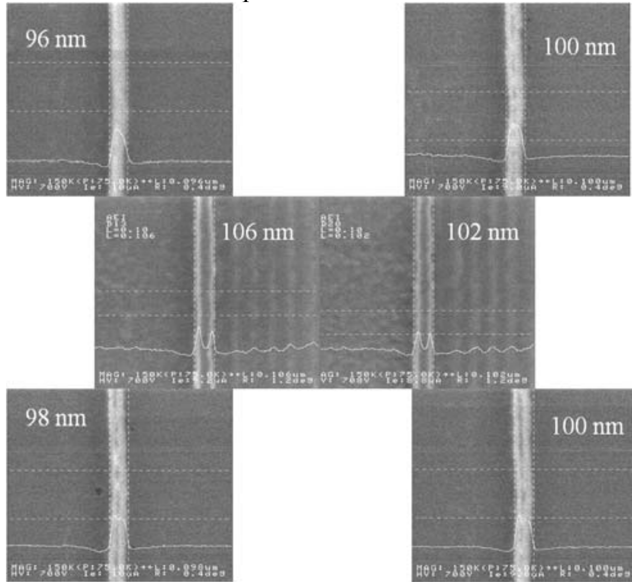


Fig. 3 In-line SEM images of poly-Si structures formed with the DP method with nominal width of 100 nm. The images were taken from different locations on a 6-in. Si wafer. The measured width is given in each picture.

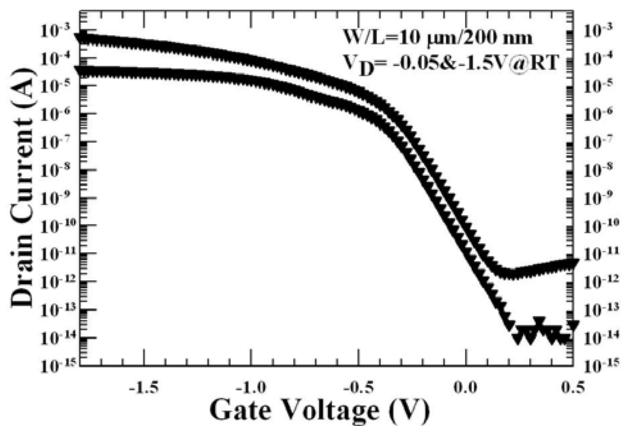


Fig. 4 Transfer characteristics of a pMOSFET with channel length of 200 nm and channel width of 10 μm, measured at V_D=-0.05 and -1.5 V.

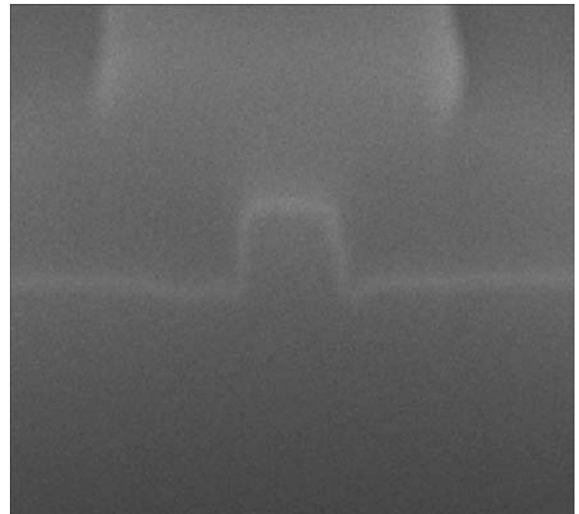


Fig. 5 Cross-sectional SEM image of a fabricated device with channel length of 200 nm.

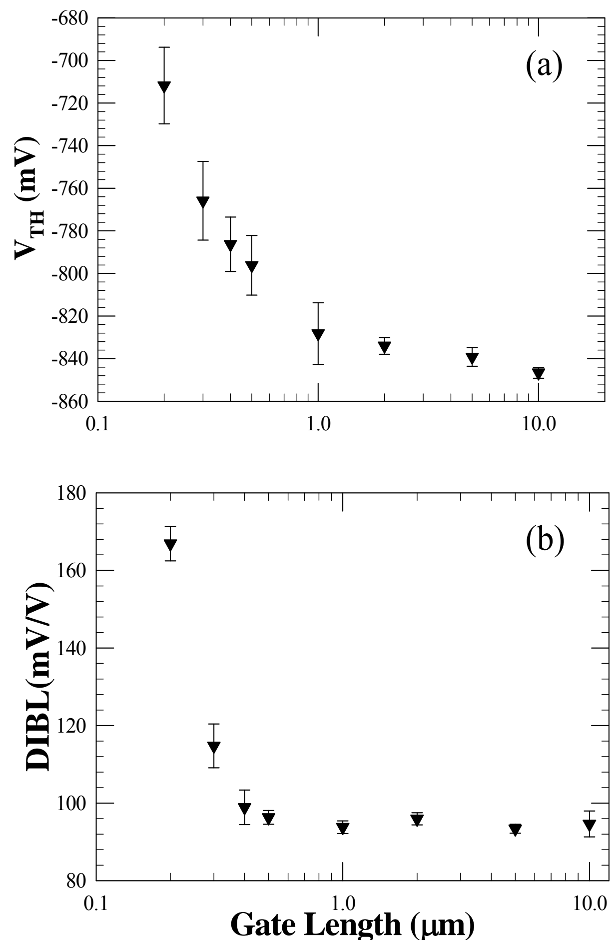


Fig. 6 (a) Threshold voltage (V_{TH}) and (b) drain induced barrier lowering (DIBL) of the fabricated devices as a function of gate length.

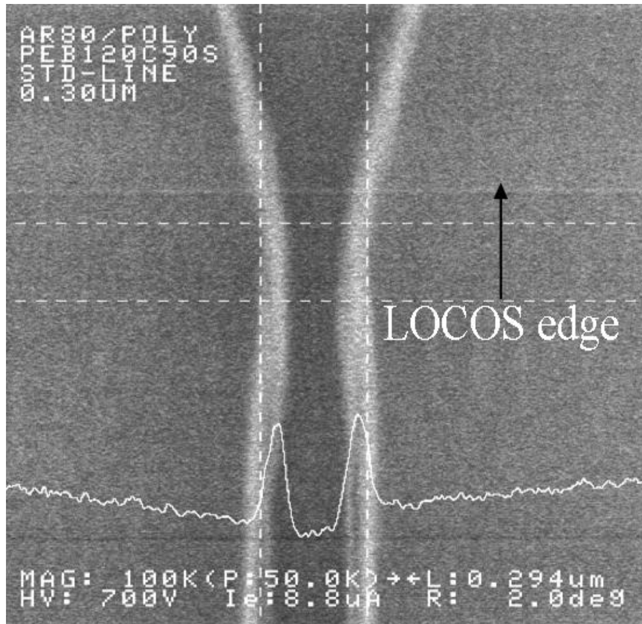


Fig. 7 In-line SEM view of a fabricated device showing the necking of the poly-Si gate at the isolation edge.

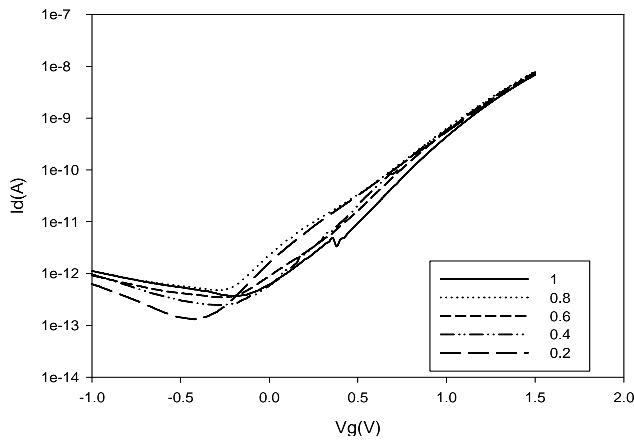


Fig. 8 Length dependence of transfer characteristics of TFETs devices with gate width of 10 µm. biased at Vd = 0.5V and Vs = -0.5V.

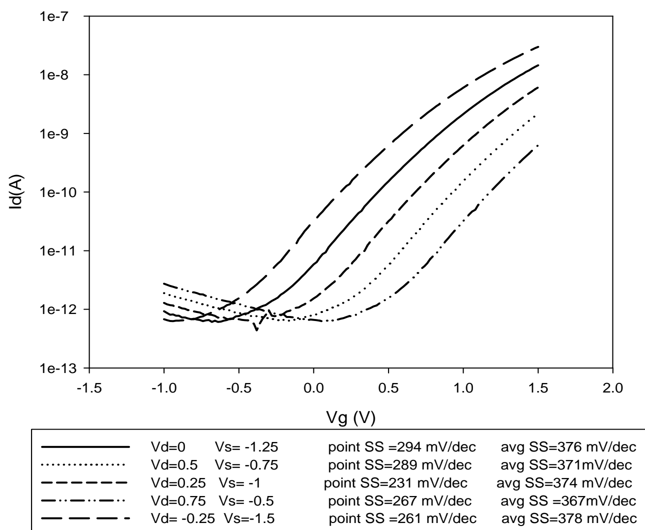


Fig. 9 Transfer characteristics of a TFET with constant Vds (1.25V) but different S/D bias. Channel length/ channel width =0.2 µm/10 µm.

無研發成果推廣資料

98 年度專題研究計畫研究成果彙整表

計畫主持人：黃調元	計畫編號：98-2221-E-009-160-
計畫名稱：以 I-line 雙重曝影技術研製次 100 奈米線寬穿隧式場效電晶體	

成果項目			量化			單位	備註（質化說明：如數個計畫共同成果、成果列為該期刊之封面故事...等）
			實際已達成數（被接受或已發表）	預期總達成數(含實際已達成數)	本計畫實際貢獻百分比		
國內	論文著作	期刊論文	0	0	100%	篇	
		研究報告/技術報告	0	0	100%		
		研討會論文	2	2	100%		SNDT, 2009, NF20. SNDT, 2010, NC06
		專書	0	0	100%		
	專利	申請中件數	0	0	100%	件	
		已獲得件數	0	0	100%		
	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（本國籍）	碩士生	0	0	100%	人次	
		博士生	0	0	100%		
		博士後研究員	0	0	100%		
		專任助理	0	0	100%		
國外	論文著作	期刊論文	2	2	100%	篇	Microelectronics Reliability, 2010, p.584. JVST B (under review), 2010.
		研究報告/技術報告	0	0	100%		
		研討會論文	1	1	100%		IEDMS, 2009, 303.
		專書	0	0	100%	章/本	
	專利	申請中件數	0	0	100%	件	
		已獲得件數	0	0	100%		
	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（外國籍）	碩士生	0	0	100%	人次	
		博士生	0	0	100%		
		博士後研究員	0	0	100%		
		專任助理	0	0	100%		

其他成果 (無法以量化表達之成果如辦理學術活動、獲得獎項、重要國際合作、研究成果國際影響力及其他協助產業技術發展之具體效益事項等，請以文字敘述填列。)	無

	成果項目	量化	名稱或內容性質簡述
科教處計畫加填項目	測驗工具(含質性與量性)	0	
	課程/模組	0	
	電腦及網路系統或工具	0	
	教材	0	
	舉辦之活動/競賽	0	
	研討會/工作坊	0	
	電子報、網站	0	
	計畫成果推廣之參與（閱聽）人數	0	

國科會補助專題研究計畫成果報告自評表

請就研究內容與原計畫相符程度、達成預期目標情況、研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）、是否適合在學術期刊發表或申請專利、主要發現或其他有關價值等，作一綜合評估。

1. 請就研究內容與原計畫相符程度、達成預期目標情況作一綜合評估

□達成目標

■未達成目標（請說明，以 100 字為限）

■實驗失敗

□因故實驗中斷

□其他原因

說明：

我們成功利用 I-line 雙重曝影技術製作出 100 奈米以下的閘極圖形,並且研製出非對稱式源汲極場效電晶體,然而由於源極端接面的摻雜濃度分布無法達到足以產生穿隧機制所需的陡直濃度分布的門檻,也因此無法達到 60mV/dec 次臨界擺幅的理想目標

2. 研究成果在學術期刊發表或申請專利等情形：

論文：■已發表 □未發表之文稿 □撰寫中 □無

專利：□已獲得 □申請中 ■無

技轉：□已技轉 □洽談中 ■無

其他：（以 100 字為限）

3. 請依學術成就、技術創新、社會影響等方面，評估研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）（以 500 字為限）

I-line 雙重曝影技術十分適合學術研究單位應用於奈米級元件製作,不僅微影速度較電子束系統快,而且同時具備製作非對稱式元件的能力,此外,就微影設備的維護方面考量下,I-line 步進機成本比電子束系統便宜的多,儀器維護方面也較方便,整體考量下對學術研究的價值不在言下