行政院國家科學委員會專題研究計畫 成果報告

前瞻矽奈米元件變異性及傳輸特性綜合研究(I)
研究成果報告(精簡版)

計 畫 類 別 ：個別型
計 畫 編 號 ：NSC 98-2221-E-009-178-
執 行 期 間 ：98 年 08 月 01 日至 99 年 07 月 31 日
執 行 單 位 ：國立交通大學電子工程學系及電子研究所

計 畫 主 持 人：蘇彬

計畫參與人員：博士班研究生-兼任助理人員：吳育昇
博士班研究生-兼任助理人員：郭俊延
博士班研究生-兼任助理人員：胡璧合
博士班研究生-兼任助理人員：范銘隆
博士班研究生-兼任助理人員：呂昆諺
博士班研究生-兼任助理人員：陳柏年

報 告 附 件 ：出席國際會議研究心得報告及發表論文

處 理 方 式 ：本計畫可公開查詢

中 華 民 國 99 年 10 月 29 日

前瞻矽奈米元件變異性及傳輸特性綜合研究(I)

計畫編號 : NSC 98-2221-E-009-178
執行期限 : 98 年 08 月 01 日　至　99 年 07 月 31 日
主持人 : 蘇彬　　國立交通大學電子工程學系

一、中文摘要

在本計畫中，我們對以矽為基底的前瞻奈米元件，針對其變異性及載子傳輸特性，進行綜合研究。在工作項目一中，我們探討使用應變矽(strained-Si)對元件匹配及變異特性的影響。這項研究不僅對使用先進 CMOS 元件的電路設計很重要，也有助於對奈米元件的本質參數變異的根本了解。在工作項目二中，我們針對不同應變程度的元件，藉由載子遷移率之溫度效應及低頻雜訊特性變化，探討應變對載子傳輸特性的影響。這項研究將有助於了解極微縮應變矽元件的載子傳輸機制，也對未來提昇載子遷移率的元件設計有所幫助。在工作項目三中，為提升鰭狀電晶體(FinFET)電路的效能，可改變通道表面方向以達到最佳化設計，本研究發展了一個包含量子侷限效應之解析理論模型，用以探討使用不同通道表面方向的矽及鍺材料鰭狀電晶體的變異性。我們的元件模型也將有助於未來極微縮鰭狀電晶體的設計。

關鍵詞：
應變矽，鰭狀電晶體，量子侷限，匹配，變異性，載子傳輸，遷移率，低頻雜訊

Abstract

In this project we conduct a comprehensive study of variability and carrier transport for advanced silicon-based nanodevices. In task I, we investigate and analyze the mismatching properties of nanoscale strained MOSFETs. This study is important not only for circuit designs using advanced CMOS devices, but also for the fundamental understanding of intrinsic parameter fluctuations in nanodevices. In task II, we conduct a comprehensive study of carrier transport for nanoscale strained MOSFETs. Our studies regarding the impact of uniaxial strain on the temperature dependence of carrier mobility and the carrier-mobility-fluctuation low-frequency noise have unveiled several puzzles regarding carrier transport in ultra-scaled strained devices, and provided insights for future mobility scaling. In task III, we investigate the impact of surface orientation on the threshold-voltage sensitivity to process variations for Si and Ge FinFETs using an analytical solution of Schrödinger equation. Our theoretical model considers the parabolic potential well due to short-channel effects and therefore can be used to assess the quantum-confinement effect in short-channel FinFETs. Our study has provided insights for device design and circuit optimization using advanced FinFET technologies.

Keywords :
strained-Si, FinFET, quantum confinement, mismatch, variability, carrier transport, mobility, low frequency noise

二、計畫目的及研究方法

In this project, we conduct a comprehensive study of variability and carrier transport for advanced silicon-based nanodevices [1]. This report describes our three main tasks:

Task I: Investigation and analysis of mismatching properties for nanoscale strained MOSFETs [2]

Task II: Impact of uniaxial strain on the temperature dependence of carrier mobility [3] and the carrier-mobility-fluctuation low-frequency noise [4] in nanoscale pMOSFETs

Task III: Impact of surface orientation on the threshold-voltage variability of ultra-scaled FinFETs [5]

Task I

With the scaling of device dimensions, the device mismatching that stems from stochastic fluctuations is becoming a concern for nanoscale MOSFETs [6]-[8]. Device mismatch may limit the achievable accuracy in analog applications such as multiplexed analog systems, digital-to-analog converters, reference source, and the SRAM. Since strained silicon is widely used in state-of-the-art CMOS technologies to enable the mobility scaling [9]-[10], a comprehensive study regarding the impact of strain on device mismatch is needed.

In this work, we conduct a systematic comparison of the mismatching properties of nanoscale strained MOSFETs between strained and unstrained devices.

Task II

Uniaxial strained-Si technology is crucial to transistor performance in state-of-the-art CMOS development [11]-[12]. The temperature effect on strain-enhanced mobility is of special importance because it may provide insights for the underlying mechanisms responsible for the performance enhancement. Although several studies have investigated the temperature effect on strain-enhanced mobility in the past [13]-[16], the temperature effect of process-induced uniaxial strain for nanoscale pMOSFETs is still not clear and merits investigation.

In addition, low frequency noise in nanoscale CMOS devices is becoming increasingly important because it may limit the functionality of analog and digital circuits [17]. Our pervious study showed that the carrier-number-fluctuations origin input-referred voltage noise of the uniaxial compressive strained pMOSFETs can be improved intrinsically by reducing the tunneling attenuation length through the strain-increased out-of-plane effective mass and tunneling barrier height [18]. Nevertheless, the carrier-number-fluctuations origin low frequency noise only dominates in the low gate voltage overdrive (V_{gst}) regime. Whether there exists an intrinsic strain effect on the low frequency noise characteristics in the high V_{gst} regime is still not clear and merits investigation.

In this work, we conduct an experimental assessment for the impact of the process-induced uniaxial strain on the temperature dependence of carrier mobility and the carrier-mobility-fluctuations origin low frequency noise in nanoscale pMOSFETs.

Task III

Because the carrier mobility of MOSFET depends on surface orientation, it has been proposed that the circuit performance of FinFET can be enhanced with the optimized surface orientation [19]-[21]. However, the immunity of FinFET structure with various surface orientations to process variations has rarely been examined. As the channel thickness (i.e., fin width) of FinFET scales down, the quantum confinement effect may become significant. This 1-D confinement effect may result in the threshold voltage (V_{th}) shift and impact the V_{th} variability. Moreover, the impact of quantum confinement may show surface-orientation dependence.

In this work, we investigate the V_{th} variability of Si- and Ge-channel FinFET with various surface orientations using analytical solution of Schrödinger equation. The theoretical model provides us a physical and efficient method to explore the impact of quantum-confinement effect. In addition, to validate the results predicted by the theoretical model, we also perform the 3-D atomistic simulation to assess the V_{th} dispersion due to fin line-edge-roughness (fin-LER) for FinFET with various surface orientations.

三、結果與討論

1. Investigation and analysis of mismatching properties for nanoscale strained MOSFETs [2]

Fig. 1 (a) and (b) show the V_g dependence of the extracted standard deviations of normalized drain current mismatch ($\sigma(\Delta I_d)/I_d$) for strained and control devices with L_{gate} = 54nm and gate width (W) = 0.3μm in the linear region ($|V_d|$=0.05V) and saturation region ($|V_d|$=1V), respectively. It can be seen that, for gate voltage overdrive ($|V_{gst}|=|V_g|-|V_{th}|$) below 0.4V, the $\sigma(\Delta I_d)/I_d$ of the strained device is larger than that of the unstrained one. On the other hand, for $|V_{gst}|$ above 0.4V, the $\sigma(\Delta I_d)/I_d$ of the strained device is smaller than that of the unstrained one.

The normalized drain current mismatch in the low $|V_{gst}|$ regime (e.g., $|V_{gst}|$<0.4V) is dominated by the threshold voltage mismatch, and can be expressed as:

$$\frac{\Delta I_d}{I_d} = -\frac{g_m}{I_d} \times (\Delta V_{th}) , \quad (1)$$

Fig. 2 shows that the g_m/I_d of the strained device is significantly larger than the control device. It is the enhanced g_m/I_d that increases the drain current mismatch in the low $|V_{gst}|$ regime (see Eq. (1)). The g_m/I_d for the strained device is higher than its control counterpart because of the higher V_g sensitivity of carrier mobility (μ_{eff}) present in the strained device, as shown in Fig. 3. It can be seen from Fig. 3 that μ_{eff} increases with V_g in the low $|V_{gst}|$ regime. This is because in the low $|V_{gst}|$ regime, the mobility is mainly determined by Coulombic scattering [22]. The mobile carrier screening makes μ_{eff} increases with V_g. The larger slope of the mobility for the strained device is responsible for the higher g_m/I_d observed in Fig. 2.

Nevertheless, for a given g_m/I_d, the $\sigma(\Delta I_d)/I_d$ for the strained and control devices are nearly identical. In other words, the V_{th} mismatch for the strained and control devices are nearly the same, as demonstrated in Fig. 4. Note that a linear dependence of $\sigma(\Delta V_{th})$ on $1/(WL_{gate})^{-1/2}$ in the Pelgrom plot indicates a random-dopant-fluctuations origin of V_{th} mismatch [23]. Moreover, the increase of $\sigma(\Delta V_{th})$ with increasing $|V_d|$ due to drain induced barrier lowering (DIBL) can also be observed in Fig. 4 [24].

In the high $|V_{gst}|$ regime (e.g., $|V_{gst}|$>0.4V), Fig. 1(a) and (b) show smaller $\sigma(\Delta I_d)/I_d$ for the strained device as compared with the unstrained one. In the high $|V_{gst}|$ regime, the variance of the $\sigma(\Delta I_d)/I_d$ can be expressed as:

$$\sigma^2\left(\frac{\Delta I_d}{I_d}\right) = \left(\frac{g_m}{I_d}\right)^2 \times \sigma^2(\Delta V_{th}) + \sigma^2\left(\frac{\Delta\beta}{\beta}\right), \quad (2)$$

where g_m and β are the transconductance and current factor, respectively. Fig. 5(a) and (b) show a comparison of the measured $\sigma^2(\Delta I_d)/I_d$ with Eq. (2) at $|V_d|$=0.05V and $|V_d|$=1V, respectively. It can be seen that the $\sigma^2(\Delta I_d)/I_d$ can be modeled well by considering the contribution from both ΔV_{th} and $\Delta\beta$.

Fig. 5(a) indicates that the $\Delta I_d/I_d$ in the high $|V_{gst}|$ linear regime is dominated by $\Delta\beta/\beta$. The Pelgrom plot of $\sigma(\Delta\beta)/\beta$ shown in Fig. 6(a) further demonstrates that it is the reduced $\sigma(\Delta\beta)/\beta$ that reduces the linear drain current mismatch in the high $|V_{gst}|$ regime. It should be noted that although the $\sigma(\Delta\beta)/\beta$ of the strained device is smaller than that of the unstrained one, the $\sigma(\Delta\beta)$ is actually larger for the strained device as shown in Fig. 6(b). It is plausible that the increased $\sigma(\Delta\beta)$ results from the strain enhanced mobility fluctuation. As compared with Fig. 1(a), Fig. 1(b) shows larger discrepancies in $\sigma(\Delta I_d)/I_d$ between strained and unstrained devices in saturation region. In other words, the improvement in $\sigma(\Delta I_d)/I_d$ for the strained device is further enhanced in saturation region. Fig. 5(b) indicates that the V_{th} mismatch is still relevant to the overall $\sigma(\Delta I_d)/I_d$ in the high $|V_{gst}|$ saturation region. In other words, the excess improvement of $\sigma(\Delta I_d)/I_d$ for the strained device in saturation region results from the reduced V_{th} mismatch. Since the V_{th} mismatch

for the strained and control devices are nearly the same, as demonstrated in Fig. 4, the reduced V_{th} mismatch can be explained by the strain-reduced g_m/I_d in the high $|V_{gst}|$ saturation region (e.g. $|V_d|$=1V) as shown in Fig. 7. The reduced g_m/I_d in the high $|V_{gst}|$ saturation region for the strained device can be attributed to the strain-reduced E_{sat}. The strain- reduced E_{sat} results from the enhanced mobility in the strained device. The enhancement in mobility corresponds to an increase in slope of the carrier velocity versus lateral field characteristic and a reduction in the critical field (E_{sat}) for velocity saturation.

In conclusion, we have investigated and analyzed the mismatching properties of nanoscale strained PMOSFETs under various bias conditions. In the low $|V_{gst}|$ regime, the $\sigma(\Delta I_d)/I_d$ for the strained device is enhanced while the threshold voltage mismatch of the strained device is nearly identical to that of the control one. The increased $\sigma(\Delta I_d)/I_d$ for the strained device can be attributed to the enhanced g_m/I_d. In other words, the $\sigma(\Delta I_d)/I_d$ of the strained device is almost the same as the unstrained one at a given g_m/I_d. In the high $|V_{gst}|$ linear region, the smaller $\sigma(\Delta I_d)/I_d$ for the strained device results from its smaller $\sigma(\Delta\beta)/\beta$, albeit the $\sigma(\Delta\beta)$ for the strained device is larger than that of the unstrained one. In the high $|V_{gst}|$ saturation regime, the improvement in $\sigma(\Delta I_d)/I_d$ for the strained device is further enhanced because of the strain-reduced E_{sat}.

2. Impact of uniaxial strain on the temperature dependence of carrier mobility [3] and the carrier-mobility-fluctuation low-frequency noise [4] in nanoscale pMOSFETs

Fig. 8 shows the drain current (I_D) versus gate voltage characteristics at various temperatures for the PMOS devices under test. The drain current shows strong correlation with stressor types and can be explained by the extracted carrier mobility, as shown in Fig. 9. It can be seen from Fig. 9 that the short channel mobility in PMOS (L_{EFF} = 95 nm) shows significant dependence on the uniaxial strain. The PMOS mobility prefers compressive stress because of the strain-reduced conductivity effective mass [9]. In addition, Fig. 9 shows that the mobility is degraded when temperature increases in the high vertical-field region, where phonon scattering is important [25]-[26]. Moreover, the temperature dependence of mobility shows strong sensitivity to strain. In other words, as the mobility is enhanced by compressive strain, its temperature dependence also increases. Fig. 10 shows the temperature sensitivity ($\log \mu / \log T$) of the hole mobility versus the vertical effective electric field (EEFF). For a given stressor, it can be seen that the temperature sensitivity increases (i.e., more negative) and then saturates as EEFF increases. More importantly, the $\log\mu/\log T$ for the PFET under compressive strain is the highest in absolute value among the three stressors. In other words, the scattering mechanism of the PMOS device becomes more phonon limited [25]-[26] under compressive strain. This also explains why the temperature sensitivity of drain current for the compressively strained PFET is the largest among the three stressors, as shown in Fig. 8. Fig. 11 shows the hole-mobility enhancement ($\Delta\mu/\mu$) versus temperature at EEFF = 1.5MV/cm. It shows that for both compressive and tensile stressors, the magnitude of $\Delta\mu/\mu$ decreases as temperature increases. Our result from the process-induced uniaxial stressors is consistent with the study in [16], in which an external compressive uniaxial mechanical stress was applied. Based on the model proposed in [16], it is plausible that as temperature increases, the compressively strained PFET has less holes to populate states near the band edge where the conductivity effective mass along the channel direction is smaller. Therefore, the observed mobility enhancement decreases with increasing temperature.

The drain current noise spectral densities (S_{Id}) for the strained and unstrained devices with L_{gate}=65nm biased at gate overdrive $|V_{gst}|$=0.8V are shown in Fig. 12. The spectra show typical $1/f^{\gamma}$ noise type with the frequency index γ close to one. Fig. 13 shows the normalized drain current noise spectral density (S_{Id}/I_d^2) versus $|V_{gst}|$ from the average of 10 devices. It can be seen that the strained device shows larger S_{Id}/I_d^2 than its control counterpart in this high gate-voltage overdrive regime.

Fig. 14 shows the input-referred noise spectral density for the strained and unstrained devices. The gate bias dependent S_{Vg} as $|V_{gst}|$ larger than ~0.2V for both the strained and unstrained devices indicates the carrier-mobility- fluctuations origin of low frequency noise. According to Hooge's carrier-mobility-fluctuations noise model [27], Hooge parameter α_H is a figure of merit for low frequency noise comparison. Fig. 15 shows the extracted Hooge parameter [27] versus $|V_{gst}|$ from the average of 10 devices. It can be seen that the α_H shows weak V_{gst} dependence, which is also a signature of the carrier-mobility- fluctuations origin 1/f noise. Moreover, the strained device shows larger α_H than the unstrained one. It indicates that the carrier mobility for the strained device, as compared with the unstrained one, is more phonon-scattering limited [27]. Through Monte-Carlo analysis, Fischetti *et al.* [28] has reported that the only scattering mechanism that is sufficiently sensitive to strain is the scattering from surface roughness [29]. It is plausible that the larger enhancement in the surface roughness mobility results in the more phonon- scattering limited carrier mobility for the strained device.

Fig. 16 compares the α_H of the strained and unstrained devices with various gate length at $|V_{gst}|$=0.8V. It can be seen that the impact of strain on α_H increases as gate length decreases. This is because the process-induced strain has a local nature, and the strain increases with decreasing gate length [9].

In conclusion, we have investigated the temperature dependence of carrier mobility and the low frequency noise characteristics, respectively, for advanced short-channel strained PMOS devices. By accurate split *C–V* mobility extraction under various temperatures, we examine the impact of process-induced uniaxial strain on the temperature dependence of mobility and mobility enhancement in nanoscale pMOSFETs. Our study indicates that the strain sensitivity of hole mobility becomes less with increasing temperature, and it is consistent with previous uniaxial mechanical-bending result. Furthermore, the carrier-scattering mechanism for the pMOSFET under uniaxial compressive strain tends to be more phonon limited at a given vertical electric field, which explains the larger drain current sensitivity to temperature present in the compressively strained PFET. Regarding the low frequency noise characteristics in nanoscale PMOSFETs, It is found that the normalized drain current noise of the strained device in the high gate overdrive (V_{gst}) regime is larger than its control counterpart. In addition, the enhanced carrier-mobility-fluctuations origin 1/f noise for the strained device in the high $|V_{gst}|$ regime indicates that the carrier mobility in the strained device is more phonon-limited, which represents an intrinsic strain effect on the low frequency noise.

3. Impact of surface orientation on the threshold-voltage variability of ultra-scaled FinFETs [5]

Fig. 17 shows a schematic sketch of a FinFET structure. For long-channel undoped FinFET, the conduction band edge $E_C(x)$ was treated as a flat well with potential energy β in the past [30]. However, to account for the source/drain coupling due to short-channel effects, the conduction band edge $E_C(x)$ in (1) should be treated as a parabolic well [31] with

potential energy $E_C(x) = \alpha \cdot x^2 + \beta$. α and β are length-dependent coefficients and can be obtained from the channel potential solution of Poisson's equation under subthreshold region [32]. Using the parabolic-well approximation, an analytical solution of (1) can be obtained.

Note that as α=0 (i.e., E_C is spatially constant), $\Psi_j(x)$ will return to the form of sinusoidal functions, which is the solution for the flat-well approximation [30]. The jth eigen-energy E_j can be determined by the boundary condition $\Psi_j (x = t_{ch}/2) = 0$. Thus, the eigen-energy and eigenfunction of short-channel FinFET under subthreshold region can be derived.

Fig. 18 shows that for a short-channel lightly-doped FinFET, the conduction band edge E_C is bended from a flat well to a parabolic-like well due to source/drain coupling, and the E_j calculated by our model considering the parabolic-well approximation agrees well with the TCAD simulation that numerically solves the self-consistent solution of Poisson and Schrödinger equations [33]. Fig. 19 shows the channel length (L_{eff}) dependence of the energy difference of E_0 and the bottom of well $E_C(x = 0)$. In contrast to the constant E_0 calculated from the flat-well approximation, both the TCAD simulation and our model show that the E_0 increases with decreasing L_{eff}.

To assess the impact of quantum confinement on V_{th}, the V_{th} is defined as the V_{GS} at which the average electron density of the cross-section at $y = L_{eff}/2$ (highest potential barrier for low V_{DS}) exceeds the channel doping concentration. Fig. 20 verifies the electron density distribution calculated from the classical (CL) model and the quantum-confinement (QC) model with the TCAD simulations.

Besides theoretical model, we also perform atomistic simulation to assess the problem. We employ the Fourier synthesis approach that generates the line edge patterns using the Gaussian autocorrelation function as the power spectrum [34], and then the Monte Carlo simulations. The parameters used for the fin-LER simulations in this study are the rms amplitude (Δ) = 1.5nm and the correlation length (Λ) = 20nm [35]. Fig. 21 shows the nominal 3-D FinFET structure and some of the 150 samples used in our atomistic simulation.

For FinFET structure, different surface orientations such as (100), (110), and (111) can be achieved by rotating the device layout in the wafer plane [20]. Fig. 22 shows that for Si-FinFET with a small t_{ch}, the V_{th} and its sensitivity to channel thickness (t_{ch}) variation considering the quantum-confinement effect is larger than that predicted by the CL model. Moreover, the V_{th} of (111)- and (110)-surface increases more rapidly than that of (100)-surface with decreasing t_{ch}. This is because the quantum-confinement effect depends on surface orientation, as indicated by the inset of Fig. 22. For high-mobility channel such as Ge-FinFET, the V_{th} dispersion due to quantum-confinement becomes more significant. Fig. 23 shows that the V_{th} of (100)-surface increases more rapidly than (110)- and (111)- surface with reducing t_{ch}. This is because the quantum-confinement effect of (100)-surface is larger than that of (110)- and (111)-surface, as indicated by the inset of Fig. 23.

Fig. 24 shows the V_{th} variability of (100)- and (110)- surface Si-FinFET derived from the atomistic simulation. It can be seen that the mean value as well as its spread of V_{th} for (110)-surface are larger than those of (100)-surface due to quantum confinement. The result is consistent with the V_{th} sensitivity to t_{ch} calculated by our theoretical model (Fig. 22). More results from atomistic simulation will be presented.

Besides the V_{th} sensitivity to t_{ch}, the quantum-confinement effect also affects the V_{th} sensitivity to the L_{eff} variation. Fig. 25 shows that for Ge-FinFET, the degree of V_{th} roll-off predicted by our QC model is (100) < (110) < (111) < CL, which is opposite to the V_{th} sensitivity to the t_{ch} variation (Fig. 23). In other words, while the quantum-confinement

effect enhances the V_{th} sensitivity to t_{ch}, it reduces the V_{th} sensitivity to the L_{eff} variation.

In conclusion, we have investigated the impact of surface orientation on the V_{th} variability of Si- and Ge-FinFET using both the analytical solution of Schrödinger equation and atomistic simulation. Our study indicates that, for ultra-scaled FinFET, the importance of t_{ch} variation increases due to the quantum-confinement effect. The Si-(100) and Ge-(111) surface show lower V_{th} sensitivity to t_{ch} variation as compared with other orientations. On the contrary, the quantum-confinement effect reduces the V_{th} sensitivity to L_{eff}, and Si-(111) and Ge-(100) surface show lower V_{th} sensitivity as compared with other orientations.

四、計畫成果自評

In this project we have conducted a comprehensive study of variability and carrier transport for advanced silicon-based nanodevices. We have investigated and analyzed the mismatching properties of nanoscale strained MOSFETs. This study is important not only for circuit designs using advanced CMOS devices, but also for the fundamental understanding of intrinsic parameter fluctuations in nanodevices. In addition, our studies regarding the impact of uniaxial strain on the temperature dependence of carrier mobility and the carrier-mobility-fluctuation low-frequency noise have unveiled several puzzles regarding carrier transport in ultra-scaled strained devices, and provided insights for future mobility scaling. Besides, we have investigated the impact of surface orientation on the threshold-voltage sensitivity to process variations for Si and Ge FinFETs using analytical solution of Schrödinger equation. Our theoretical model can provide insights for future device design and circuit optimization using advanced FinFET technologies.

Under the support of this NSC project, we have published 9 IEEE journal papers [2]-[5], [36]-[40]. These research works have also been crucial to the education of our graduate students to become leading researchers in the areas of silicon-based nanoelectronics, modeling and design for advanced CMOS devices, and device/circuit interaction and co-optimization in nano-CMOS.

五、參考文獻

[1] International Technology Roadmap for Semiconductors (http://www.itrs.net).

[2] J. J.-Y. Kuo, W. Chen, and P. Su, "Investigation and Analysis of Mismatching Properties for Nanoscale Strained MOSFETs," *IEEE Transactions on Nanotechnology*, vol. 9, no. 2, pp. 248-253, March 2010

[3] W. P.-N. Chen, J. J.-Y. Kuo, and P. Su, "Impact of Process-Induced Uniaxial Strain on the Temperature Dependence of Carrier Mobility in Nanoscale pMOSFETs," *IEEE EDL*, vol. 31, no. 5, May 2010, pp 414-416.

[4] J. J.-Y. Kuo, W. P.-N. Chen, and P. Su, "Enhanced Carrier-Mobility-Fluctuations Origin Low Frequency Noise in Uniaxial Strained PMOSFETs," *IEEE EDL*, vol. 31, no. 5, May 2010, pp. 497-499.

[5] Y.-S. Wu and P. Su, "Impact of Surface Orientation on the Sensitivity of FinFETs to Process Variations – An Assessment Based on Analytical Solution of Schrödinger Equation," *IEEE TED*, vol. 57, no. 12, Dec. 2010.

[6] C. Hu, "Device challenges and opportunities," *VLSI Symp. Tech. Dig.* 2004, pp. 4-5.

[7] F. Boeuf *et al.*, "An evaluation of the CMOS technology roadmap from the point of view of variability, interconnects, and power dissipation," *IEEE TED*, vol.55, no.6, pp.1433-1440, Jun. 2008.

[8] S. Saxena *et al.*, "Variation in transistor performance and leakage in nanometer-scale technologies," *IEEE TED*, vol.55, no.1, pp.131-144, Jan. 2008.

[9] S. Thompson *et al.*, "Uniaxial-process-induced strained-Si: extending the CMOS roadmap," *IEEE TED*, vol. 53, no. 5, pp.1010-1020, May 2006.

[10] X. Chen *et al.*, "Stress proximity technique for performance improvement with dual stress linear at 45nm Technology and beyond," *VLSI Symp. Tech. Dig.* 2006, pp. 74-75.

[11] F. Andrieu *et al.*, "Experimental and comparative investigation of low and high field transport in substrate- and process-induced strained nanoscaled MOSFETs," in *VLSI Symp. Tech. Dig.*, 2005, pp. 176–177.

[12] E. Wang *et al.*, "Physics of hole transport in strained silicon MOSFET inversion layers," *IEEE TED*, vol. 53, no. 8, pp. 1840–1851, Aug. 2006.

[13] F. Lime *et al.*, "Low temperature characterization of effective mobility in uniaxially and biaxially strained nMOSFETs," *Solid State Electron.*, vol. 50, no. 4, pp. 644–649, Apr. 2006.
[14] N. Sugii and K. Washio, "Low-temperature electrical characteristics of strained-Si MOSFETs," *Jpn. J. Appl. Phys.*, vol. 42, pt. 1, no. 4B, pp. 1924–1927, 2003.
[15] M. N. Tsai *et al.*, "Temperature effects of n-MOSFET devices with uniaxial mechanical strains," *Electrochem. Solid-State Lett.*, vol. 9, no. 8, pp. 276–278, Jun. 2006.
[16] X. Yang *et al.*, "Temperature dependence of enhanced hole mobility in uniaxial strained p-channel metal–oxide–semiconductor field-effect transistors and insight into the physical mechanisms," *Appl. Phys. Lett.*, vol. 93, no. 24, p. 243 503, Dec. 2008.
[17] N. Hakim *et al.*, "Superior hot carrier reliability of single halo (SH) silicon-on-insulator (SOI) nMOSFET in analog applications," *IEEE Trans. Device and Material Reliability*, vol. 5, no. 1, Mar. 2005.
[18] J. J.-Y. Kuo, W. Chen, and P. Su, "Impact of Uniaxial Strain on Low Frequency Noise in Nanoscale PMOSFETs," *IEEE EDL.*, vol. 30, no. 6, pp. 672-674, Jun. 2009.
[19] M. Yang *et al.*, "Performance Dependence of CMOS on Silicon Substrate Orientation for Ultrathin Oxynitride and HfO_2 Gate Dielectrics," *IEEE EDL*, vol. 24, pp. 339–341, May 2003.
[20] L. Chang, M. Ieong, and M. Yang, "CMOS Circuit Performance Enhancement by Surface Orientation Optimization," *IEEE TED*, vol. 51, No. 10, pp. 1621-1627, October 2004.
[21] S. Gangwal, S. Mukhopadhyay, and K. Roy, "Optimization of Surface Orientation for High-Performance, Low-Power and Robust FinFET SRAM," *IEEE CICC* 2006, pp. 433-436.
[22] W. Chen, P. Su, K. Goto, "Investigation of Coulomb Mobility in Nanoscale Strained PMOSFETs," *IEEE Trans. on Nanotechnology*, vol. 7, no. 5, pp. 538-543, Sep. 2008.
[23] M. Miyamura *et al.*, "SRAM critical field evaluation based on comprehensive physical/statistical modeling considering anomalous non-Gaussian intrinsic transistor fluctuations," *VLSI Symp. Tech. Dig.* 2007, pp.22-23.
[24] O. Weber *et al.*, "High immunity to threshold voltage variability in undoped ultra-thin FDSOI MOSFETs and its physical understanding," *IEDM Tech. Dig.*, 2008, pp. 245-248.
[25] K. Chain *et al.*, "A MOSFET electron mobility model of wide temperature range (77–400 K) for IC simulation," *Semicond. Sci. Technol.*, vol. 12, no. 4, pp. 355–358, Apr. 1997.
[26] S.-I. Takagi *et al.*, "On the universality of inversion layer mobility in Si MOSFETs: Part II—Effects of surface orientation," *IEEE TED*, vol. 41, no. 12, pp. 2363–2368, Dec. 1994.
[27] F.N. Hooge, *Physica*, vol. 83B, p. 14, 1976.
[28] M. V. Fischetti, F. Gamiz, and W. Hansch, "On the Enhanced Electron Mobility in Strained-Silicon Inversion Layers", *J. Appl. Phys.* vol. 92, pp.7320-7324, 2002.
[29] S. T. Pantelides *et al.*, "Performance, Reliability, Radiation Effects, and Aging Issues in Microelectronics From Atomic-Scale Physics to Engineering-Level Modeling," *Proc. ESSDERC* 2009, pp. 48-55.
[30] H. Ananthan and K. Roy, "A Compact Physical Model for Yield Under Gate Length and Body Thickness Variations in Nanoscale Double-Gate CMOS," *IEEE TED*, vol. 53, No. 9, pp. 2151-2159, Sep. 2006.
[31] Y.-S. Wu and P. Su, "Analytical Quantum-Confinement Model for Short-Channel Gate-All-Around MOSFETs Under Subthreshold Region," *IEEE TED*, vol. 56, No. 11, pp. 2720-2725, Nov. 2009.
[32] Y.-S. Wu and P. Su, "Sensitivity of Multigate MOSFETs to Process Variations - An Assessment Based on Analytical Solutions of 3-D Poisson's Equation," *IEEE Trans. Nanotechnology*, vol. 7, No. 3, pp. 299-304, May 2008.
[33] *ATLAS User's Manual*, SILVACO, Santa Clara, CA, 2008.
[34] A. Asenov, S. Kaya, and A. R. Brown, "Intrinsic parameter fluctuation in decananometer MOSFETs introduced by gate line edge roughness," *IEEE TED*, vol. 50, no. 5, pp. 1254–1260, May 2003.
[35] E. Baravelli *et al.*, "Impact of Line-Edge Roughness on FinFET Matching Performance," *IEEE TED*, vol. 54, No. 9, pp. 2466-2474, Sep. 2007.
[36] W. Lee and P. Su, "On the Experimental Determination of Channel Backscattering Characteristics - Limitation and Application for the Process Monitoring Purpose," *IEEE TED*, vol. 56, no. 10, pp. 2285-2290, October 2009.
[37] Y.-S. Wu and P. Su, "Analytical Quantum Confinement Model for Short-Channel Gate-All-Around MOSFETs Under Subthreshold Region," *IEEE TED*, vol. 56, no. 11, pp. 2720-2725, November 2009.
[38] Y.-S. Wu, M.-L. Fan, and P. Su, "Investigation of Switching Time Variations for Nanoscale MOSFETs Using the Effective Drive Current Approach," *IEEE EDL*, vol. 31, no. 2, pp. 162-164, February 2010.
[39] M.-L. Fan, Y.-S. Wu, V. P.-H. Hu, P. Su and C.-T. Chuang, "Investigation of Cell Stability and Write-ability of FinFET Subthreshold SRAM using Analytical SNM Model," *IEEE TED*, vol. 57, no. 6, pp. 1375-1381, June 2010.
[40] V. P.-H. Hu, Y.-S. Wu, and P. Su, "Investigation of Electrostatic Integrity for Ultra-Thin-Body Germanium-On-Nothing (GeON) MOSFET," *IEEE TNANO* (accepted) (First published online: 2010-02-02).

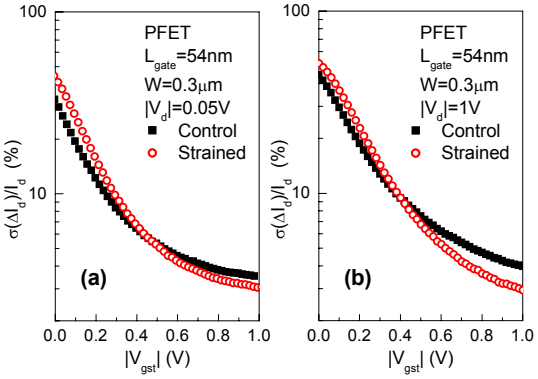


Fig. 1 Comparison of $\sigma(\Delta I_d)/I_d$ vs. $|V_{gst}|$ for strained and unstrained devices at (a) $|V_d|$=0.05V and (b) $|V_d|$=1V, respectively.

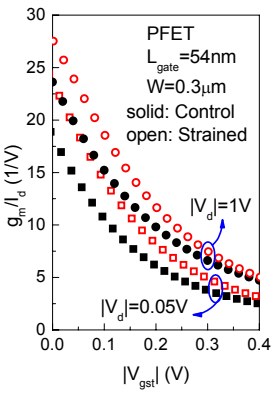


Fig. 2 The g_m/I_d for the strained device is enhanced in the low $|V_{gst}|$ regime at $|V_d|$=0.05V and 1V.

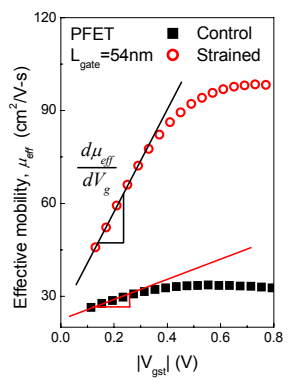


Fig. 3 Extracted carrier mobility versus $|V_{gst}|$ showing that the strained device has larger V_g sensitivity in the low $|V_{gst}|$ regime.

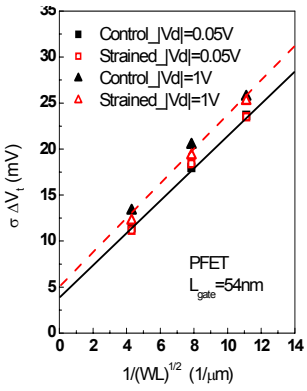


Fig. 4 Pelgrom plot of ΔV_{th} showing nearly identical ΔV_{th} for the strained and unstrained devices.

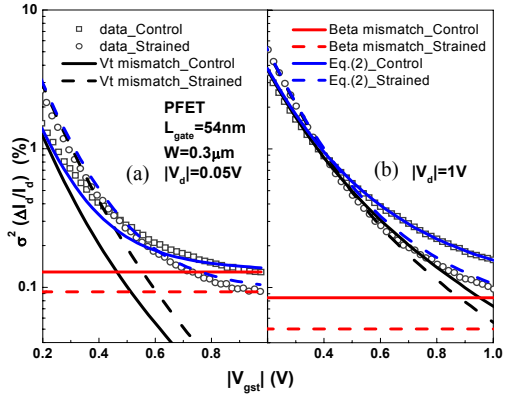
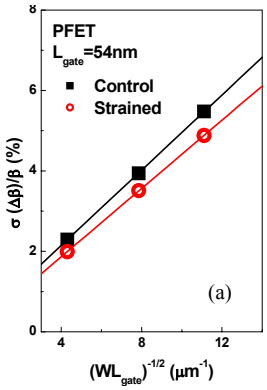


Fig. 5 The $\sigma^2(\Delta I_d)/I_d$ can be modeled well by Eq. (2) at $|V_d|$=0.05V and $|V_d|$=1V.



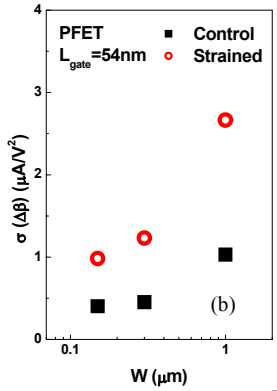


Fig. 6 (a)Pelgrom plot of $\sigma(\Delta\beta)/\beta$ showing smaller $\sigma(\Delta\beta)/\beta$ for the strained device. (b) $\sigma(\Delta\beta)$ versus gate-width showing larger $\sigma(\Delta\beta)$ for the strained device.

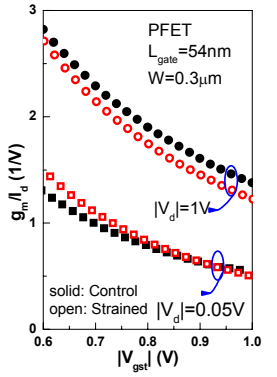


Fig. 7 The g_m/I_d for the strained device in the high $|V_{gst}|$ saturation regime ($|V_d|$=1V) is smaller than the control counterpart.

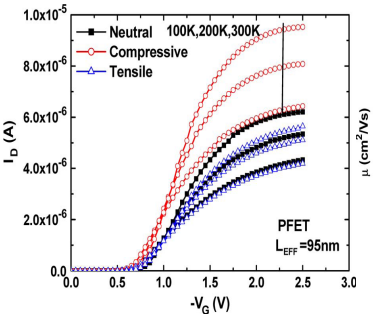


Fig. 8 Drain current versus gate voltage at various temperatures for PFETs with various stressors. The drain bias (V_{DS}) is −5 mV. The temperature dependence of the drain current shows strong correlation with stressor types.

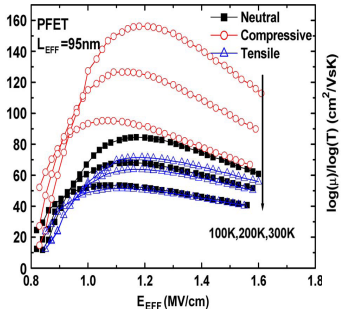


Fig. 9 Extracted carrier mobility shows significant dependence on the uniaxial stressor.

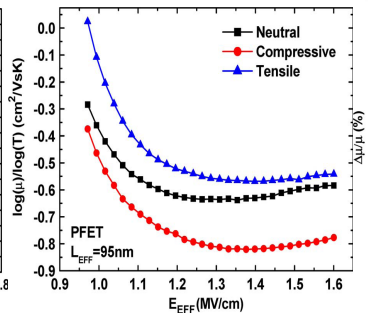


Fig. 10 Temperature sensitivity of hole mobility versus the vertical field for various uniaxial stressors.

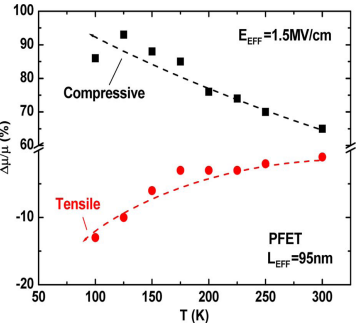


Fig. 11 Hole-mobility enhancement versus temperature at E_{EFF} = 1.5 MV/cm for PMOS devices with various stressors.

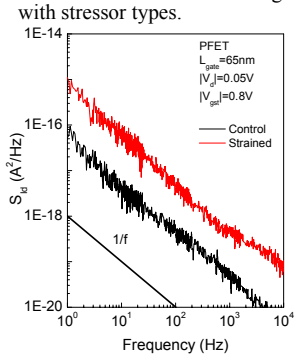


Fig. 12 Drain current noise spectral density S_{Id} for devices with L_{gate} =65nm at $|V_d|$ = 0.05V and $|V_{gst}|$=0.8V showing typical $1/f^{\gamma}$ noise type with γ close to 1.

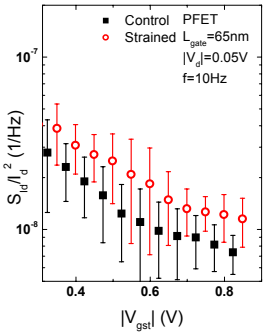


Fig. 13 Normalized drain current noise spectral density SI_d/I_d^2 versus $|V_{gst}|$ for devices with L_{gate} =65nm at f=10Hz and $|V_d|$=0.05V.

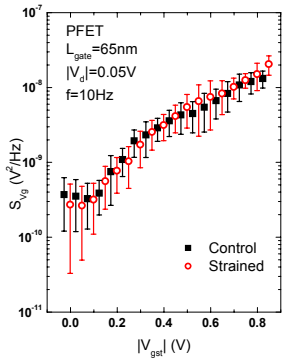


Fig. 14 Input-referred noise spectral density S_{Vg} versus $|V_{gst}|$ for devices with L_{gate} =65nm at f=10Hz and $|V_d|$=0.05V.

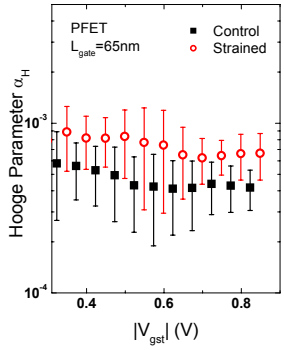


Fig. 15 Hooge parameter versus $|V_{gst}|$ showing larger mobility fluctuations for the strained devices.

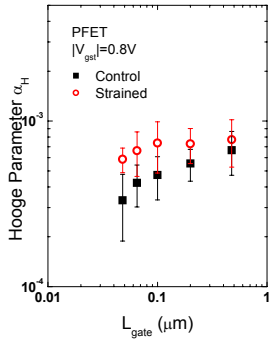


Fig. 16 Hooge parameter versus L_{gate} for strained and unstrained devices biased at $|V_{gst}|$=0.8V.

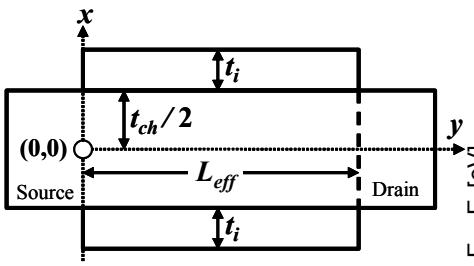


Fig. 17. Schematic sketch of FinFET structure investigated in this paper. L_{eff} is the channel length, t_{ch} is the channel thickness, and t_i is the gate insulator thickness.

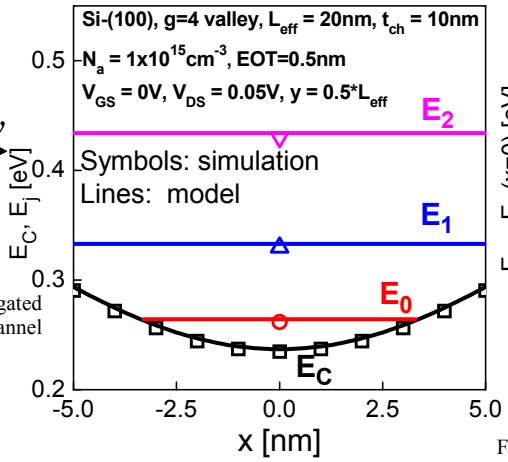


Fig. 18. Conduction band edge and quantized eigen-energies of a short-channel lightly-doped FinFET.

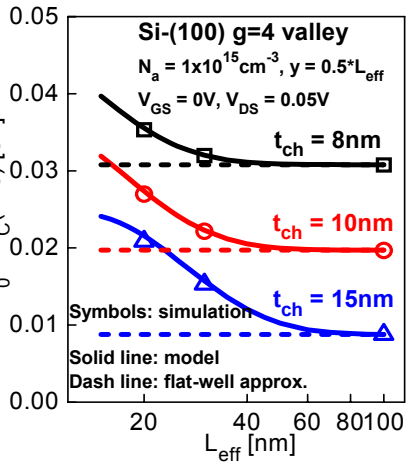


Fig. 19. Channel length dependence of the ground-state eigen-energy for lightly-doped FinFET with various t_{ch} showing the accuracy of our model.

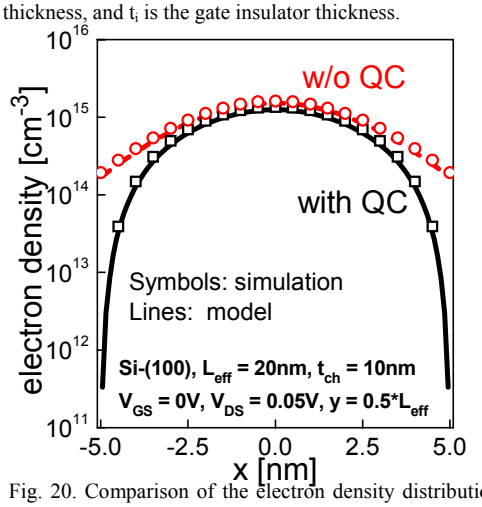


Fig. 20. Comparison of the electron density distribution with and without considering the quantum-confinement (QC) effect. The electron density is calculated from the 2-D DOS, eigen-energies, and wavefunctions

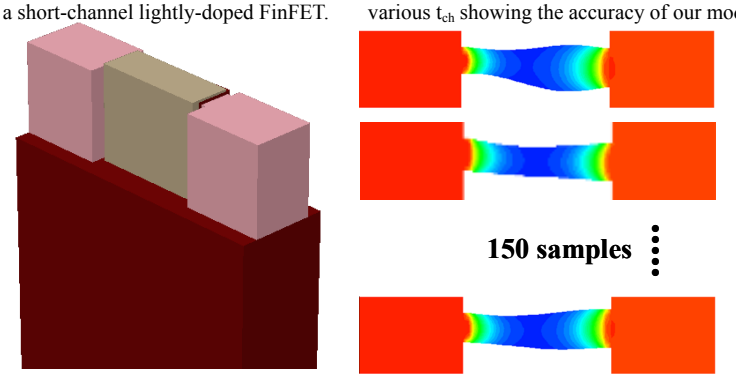


Fig. 21. The geometry of the nominal device used in our fin-LER simulation is W_{fin} = 7nm, H_{fin} = 20nm, L_{eff} = 25nm, EOT = 0.65nm. The sample number is 150.

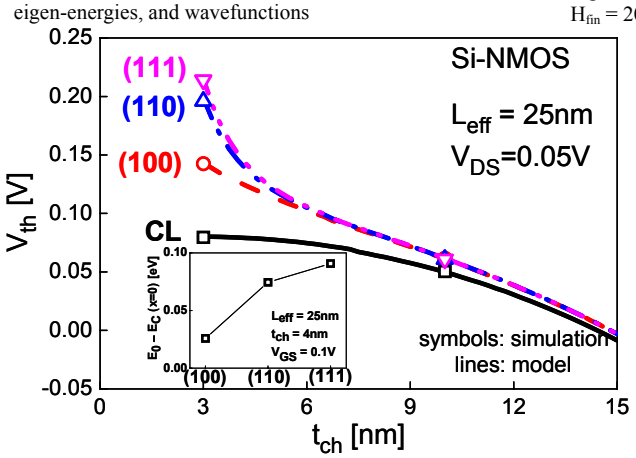


Fig. 22. Comparison of the t_{ch} dependence of V_{th} for Si-FinFET with various surface orientations and the classical model (CL). The V_{th} shift due to quantum confinement is mainly determined by the ground-state energy as indicated by the inset.

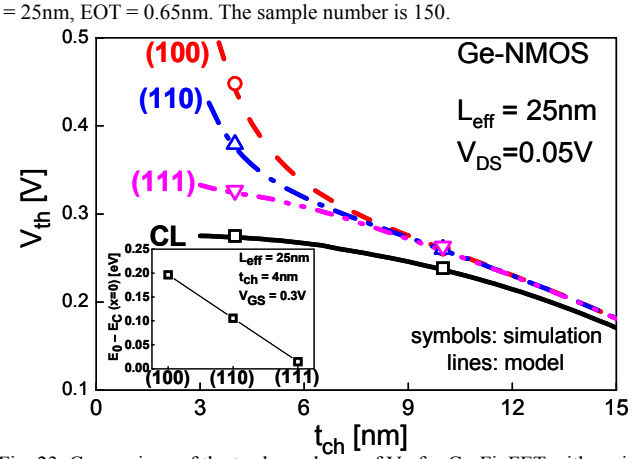


Fig. 23. Comparison of the t_{ch} dependence of V_{th} for Ge-FinFET with various surface orientations and the classical model (CL). The inset shows the comparison of the ground-state energy for various surface orientations.

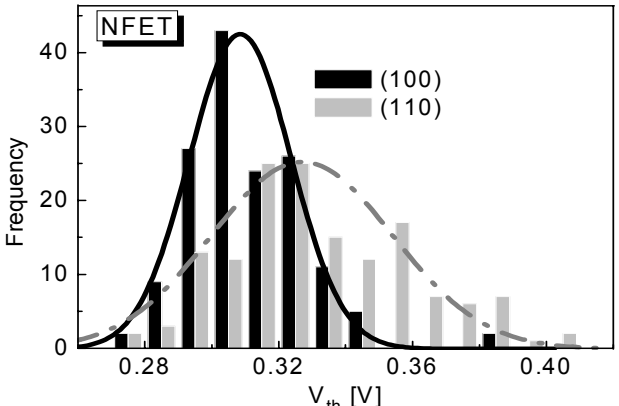


Fig. 24. The V_{th} of (110)-surface for Si-FinFET shows larger mean value and spread than those of (100)-surface.

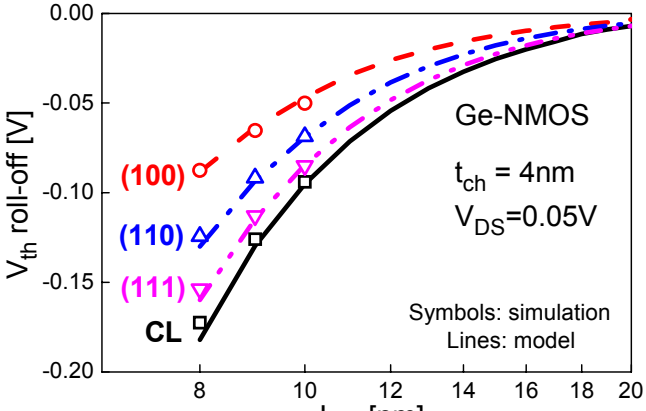


Fig. 25. Comparison of the L_{eff} dependence of V_{th} (V_{th} roll-off) for Ge-FinFET with various surface orientations and the classical model (CL).

附件四

國科會補助專題研究計畫項下出席國際學術會議心得報告

日期：99年7月27日

計畫編號	NSC98－2221－E－009－178		
計畫名稱	前瞻矽奈米元件變異性及傳輸特性綜合研究(I)		
出國人員姓名	吳育昇	服務機構及職稱	交通大學電子所博士生
會議時間	99年6月13日至 99年6月14日	會議地點	夏威夷 檀香山
會議名稱	（中文）2010 矽奈米電子研討會 （英文）2010 Silicon Nanoelectronics Workshop (SNW)		
發表論文題目	（中文）表面方向對 FinFET 臨界電壓變異的影響 （英文）Impact of Surface Orientation on V_{th} Variability of FinFET		

一、參加會議經過

今年的 SNW 地點輪到夏威夷檀香山的希爾頓飯店舉辦，由於同地點緊接著就是 VLSI symposium 這個重要會議，因此 SNW 每年也吸引不少知名學者和工業界的人士與會。今年的議程分為 7 個 session 和 2 個 poster session：

Session 1: Nanoscale FETs

Session 2: Alternative Semiconductor Materials

Session 3: Nanowire FETs

Session 4: Nanoscale Phenomena

Poster Session 1: Nanoscale Transistors, Quantum Dot Devices

Session 5: Nanoscale Memories

Session 6: Resistive RAM

Poster Session 2: Alternative Materials and Devices, Nanoscale Memories, and More

Session 7: More than Moore

其中 Session 1, 2, 3 比較偏近 MOSFET，也是我感興趣的 session。東京大學今年在 VLSI symposium 和 SNW 共有三篇 paper 講“current-onset voltage”，包括以實驗萃取以及用模擬分析，除了 V_{th} 和 g_m 之外，作者們提出造成電流變異的一個新的獨立成份。亞歷桑那州大學的 Ferry 有一篇 paper 是在講 graphene 作為 MOSFET 的通道材料的一些物理現象。Session 3 中有三篇 paper 都提到了 OMEN 這一套新的元件模擬軟體。NEMO 和 OMEN 是由 Purdue University 的研究機構所開發的數值模擬軟體，它的核心是使用 NEGF 的載子傳導模型，因此可用來模擬極小尺寸的元件如奈米線等。

我的 paper 是被分配到 poster session 1，雖然只需要 1 分鐘的口頭報告，不過隨後是 2 個小時在自己的 poster 前解說和回答問題。那 2 個小時的 poster 時間有好幾個人對於我的研究有興趣，互相交流之後讓我獲得了一些研究上可進行的方向，以及其他人對於我的研究方法有什麼不同的看法。在 2 個小時快結束時，我也到其他的人的 poster 前去看和自己研究有相關的 paper，詢問一下他們的研究內容。由於會場甚至有提供一些沙拉類的食物和啤酒類的飲料，因此 poster session 的氣氛感覺很輕鬆。有不少知名的學者也在場，可以看到期刊論文照片上的人物一個個出現在眼前，手中拿著啤酒和洋芋片，聚在一起聊天的情景。

除了 SNW 的會議本身之外，我還報名了 VLSI symposium 的 2 個 short course，包含 Technology 和 Circuit。每一個 short course 的講者都有約 1 個小時的時間，因此聽他們的演講可以廣泛而快速地瀏覽他們在自己領域的研究內容，是啟發自己研究想法的一個好機會。另外他們的投影片也已印成書面資料，帶回來後將來有需要時可以參考裡面的內容或是引用的 paper 等。

二、與會心得

雖然這個會議的名稱為“Silicon” Nanoelectronics Workshop，但是所收錄的 paper 中非 silicon 材料的主題佔了很大一部分。近幾年由於元件尺寸往往已小於 50 奈米，high-k / metal gate 的採用已變成主流技術，而其中一個對於元件的影響是 mobility 的降低，因此採用高 mobility 的通道材料便被認為是一種可能的解決方案，非 silicon 元件在國際會議上出現的比例每次都很高。在我的 paper 當中也有考慮 Germanium 做為通道材料的可能性，並研究其量子侷限效應對於元件電性變異的影響，未來對於非 silicon 通道材料的研究仍是熱門的主題，應該持續努力。

在 VLSI Technology 的 short course 部分，東京大學的 Prof. Toriumi 的演講“Technology Outlook for Group IV CMOS and Beond-CMOS Semiconductor Devices”中包含了許多先進的元件材料及架構如 carbon nanotube 和 graphene 等的介紹及引用文獻中代表性的 paper 等，這對未來想要進入這個領域的研究者是一個很好的參考資料。

在 VLSI Circuit 的 short course 中，IBM 的 Shahidi 和 Intel 的 Zhang 都有提到目前奈米製程上一定會面臨的製程變異的問題，他們的演講中皆有提到如何用各樣不同的電路設計使製程變異造成的影響降到最低。製程變異的問題不只是 Technology 領域的人要致力減輕，對於電路設計的人士也是要付出心力去解決的議題。

三、建議

這個會議的名字雖然是「矽」奈米電子研討會，但是近來以非傳統的矽材料作為 MOSFET 的研究方向漸趨熱門，高 mobility 的材料如鍺及其他 III-V 族的材料也受到

許多關注，因此許多研究主題不是矽元件的 paper 也都會投到這個會議來。而且這個會議之後接下來就是 VLSI Symposium 的舉行，因此與會者許多皆是來自大公司或學術界的知名人物。如果 paper 能在這個會議上被接受，在這個領域中曝光率比較高，也能讓較多人知道自己的研究內容。因此應該多加宣傳，讓在台灣做 III-V 族或是鍺元件的研究也能到這個會議上來發表，也可以增加台灣在半導體研究上的知名度。

四、攜回資料名稱及內容

2010 Silicon Nanoelectronics Workshop 論文集

VLSI Technology Short Course 書面投影片內容

VLSI Circuit Short Course 書面投影片內容

五、其他

Impact of Surface Orientation on V_{th} Variability of FinFET

Yu-Sheng Wu, Ming-Long Fan, and Pin Su
Department of Electronics Engineering & Institute of Electronics, National Chiao Tung University, Taiwan
Tel:+886-3-5712121 ext. 54142, Fax:+886-3-5724361, E-mail: pinsu@faculty.nctu.edu.tw

Introduction

Because the carrier mobility of MOSFET depends on surface orientation, it has been proposed that the circuit performance of FinFET can be enhanced with the optimized surface orientation [1]-[3]. However, the immunity of FinFET structure with various surface orientations to process variations has rarely been examined. As the channel thickness (i.e., fin width) of FinFET scales down, the quantum confinement effect may become significant. This 1-D confinement effect may result in the threshold voltage (V_{th}) shift and impact the V_{th} variability. Moreover, the impact of quantum confinement may show surface-orientation dependence.

In this work, we investigate the V_{th} variability of Si- and Ge-channel FinFET with various surface orientations using analytical solution of Schrödinger equation. The theoretical model provides us a physical and efficient method to explore the impact of quantum-confinement effect. In addition, to validate the results predicted by the theoretical model, we also perform the 3-D atomistic simulation to assess the V_{th} dispersion due to fin line-edge-roughness (fin-LER) for FinFET with various surface orientations.

Analytical Solution of Schrödinger Equation

Fig. 1 shows a schematic sketch of a FinFET structure. To consider the quantum-confinement effect along the fin-width (i.e., x) direction, the Schrödinger equation can be express as

$$-\frac{\hbar^2}{2m_x}\cdot\frac{d^2\Psi_j(x)}{dx^2}+E_C(x)\cdot\Psi_j(x)=E_j\cdot\Psi_j(x) \quad (1)$$

where E_j is the jth eigen-energy, $\Psi_j(x)$ is the corresponding wavefunction, and m_x is the carrier quantization effective mass. For long-channel undoped FinFET, the conduction band edge $E_C(x)$ was treated as a flat well with potential energy β in the past [4]. However, to account for the source/drain coupling due to short-channel effects, the conduction band edge $E_C(x)$ in (1) should be treated as a parabolic well [5] with potential energy $E_C(x) = \alpha x^2 + \beta$. α and β are length-dependent coefficients and can be obtained from the channel potential solution of Poisson's equation under subthreshold region [6].Using the parabolic-well approximation, an analytical solution of (1) can be obtained.

Note that as α=0 (i.e., E_C is spatially constant), $\Psi_j(x)$ will return to the form of sinusoidal functions, which is the solution for the flat-well approximation [4]. The jth eigen-energy E_j can be determined by the boundary condition $\Psi_j(x = t_{ch}/2) = 0$. Thus, the eigen-energy and eigenfunction of short-channel FinFET under subthreshold region can be derived.

Fig. 2 shows that for a short-channel lightly-doped FinFET, the conduction band edge E_C is bended from a flat well to a parabolic-like well due to source/drain coupling, and the E_j calculated by our model considering the parabolic-well approximation agrees well with the TCAD simulation that numerically solves the self-consistent solution of Poisson and Schrödinger equations [7]. Fig. 3 shows the channel length (L_{eff}) dependence of the energy difference of E_0 and the bottom of well $E_C(x = 0)$. In contrast to the constant E_0 calculated from the flat-well approximation, both the TCAD simulation and our model show that the E_0 increases with decreasing L_{eff}.

To assess the impact of quantum confinement on V_{th}, the V_{th} is defined as the V_{GS} at which the average electron density of the cross-section at $y = L_{eff}/2$ (highest potential barrier for low V_{DS}) exceeds the channel doping concentration. Fig. 4 verifies the electron density distribution calculated from the classical (CL) model and the quantum-confinement (QC) model with the TCAD simulations.

Atomistic Monte Carlo Simulation

Besides theoretical model, we also perform atomistic simulation to assess the problem. We employ the Fourier synthesis approach that generates the line edge patterns using the Gaussian autocorrelation function as the power spectrum [8], and then the Monte Carlo simulations. The parameters used for the fin-LER simulations in this study are the rms amplitude (Δ) = 1.5nm and the correlation length (Λ) = 20nm [9]. Fig. 5 shows the nominal 3-D FinFET structure and some of the 150 samples used in our atomistic simulation.

Impact of Surface Orientation on V_{th} Variability

For FinFET structure, different surface orientations such as (100), (110), and (111) can be achieved by rotating the device layout in the wafer plane [2]. Fig. 6 shows that for Si-FinFET with a small t_{ch}, the V_{th} and its sensitivity to channel thickness (t_{ch}) variation considering the quantum-confinement effect is larger than that predicted by the CL model. Moreover, the V_{th} of (111)- and (110)-surface increases more rapidly than that of (100)-surface with decreasing t_{ch}. This is because the quantum-confinement effect depends on surface orientation, as indicated by the inset of Fig. 6. For high-mobility channel such as Ge-FinFET, the V_{th} dispersion due to quantum-confinement becomes more significant. Fig. 7 shows that the V_{th} of (100)-surface increases more rapidly than (110)- and (111)-surface with reducing t_{ch}. This is because the quantum-confinement effect of (100)-surface is larger than that of (110)- and (111)-surface, as indicated by the inset of Fig. 7.

Fig. 8 shows the V_{th} variability of (100)- and (110)-surface Si-FinFET derived from the atomistic simulation. It can be seen that the mean value as well as its spread of V_{th} for (110)-surface are larger than those of (100)-surface due to quantum confinement. The result is consistent with the V_{th} sensitivity to t_{ch} calculated by our theoretical model (Fig. 6). More results from atomistic simulation will be presented.

Besides the V_{th} sensitivity to t_{ch}, the quantum-confinement effect also affects the V_{th} sensitivity to the L_{eff} variation. Fig. 9 shows that for Ge-FinFET, the degree of V_{th} roll-off predicted by our QC model is (100) < (110) < (111) < CL, which is opposite to the V_{th} sensitivity to the t_{ch} variation (Fig. 7). In other words, while the quantum-confinement effect enhances the V_{th} sensitivity to t_{ch}, it reduces the V_{th} sensitivity to the L_{eff} variation.

Conclusions

We have investigated the impact of surface orientation on the V_{th} variability of Si- and Ge-FinFET using both the analytical solution of Schrödinger equation and atomistic simulation. Our study indicates that, for ultra-scaled FinFET, the importance of t_{ch} variation increases due to the quantum-confinement effect. The Si-(100) and Ge-(111) surface show lower V_{th} sensitivity to t_{ch} variation as compared with other orientations. On the contrary, the quantum-confinement effect reduces the V_{th} sensitivity to L_{eff}, and Si-(111) and Ge-(100) surface show lower V_{th} sensitivity as compared with other orientations. Our study may provide insights for device design and circuit optimization using advanced FinFET technologies.

Acknowledgement

This work was supported in part by the National Science Council of Taiwan under contract NSC 98-2221-E-009-178 and in part by the Ministry of Education in Taiwan under ATU Program.

References

[1] M. Yang *et al.*, *IEEE EDL*, vol. 24, No. 5, p.339, 2003.
[2] L. Chang *et al.*, *IEEE TED*, vol. 51, No. 10, p.1621, 2004.
[3] S. Gangwal *et al.*, *CICC* 2006, p. 433.
[4] H. Ananthan and K. Roy, *IEEE TED*, vol. 53, No. 9, p.2151, 2006.
[5] Y.-S. Wu and P. Su, *IEEE TED*, vol. 56, No. 11, p. 2720, 2009.
[6] Y.-S. Wu and P. Su, *IEEE TNANO*, vol. 7, No. 3, p.299, 2008.
[7] *ATLAS User's Manual*, SILVACO, Santa Clara, CA, 2008.
[8] A. Asenov *et al.*, *IEEE TED*, vol. 50, No. 5, p.1254, 2003.
[9] E. Baravelli *et al.*, *IEEE TED*, Vol. 54, No. 9, pp. 2466, 2007.

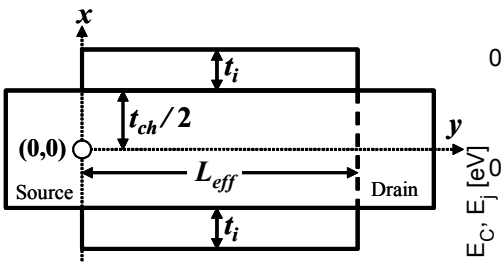


Fig. 1. Schematic sketch of FinFET structure investigated in this paper. L_{eff} is the channel length, t_{ch} is the channel thickness, and t_i is the gate insulator thickness.

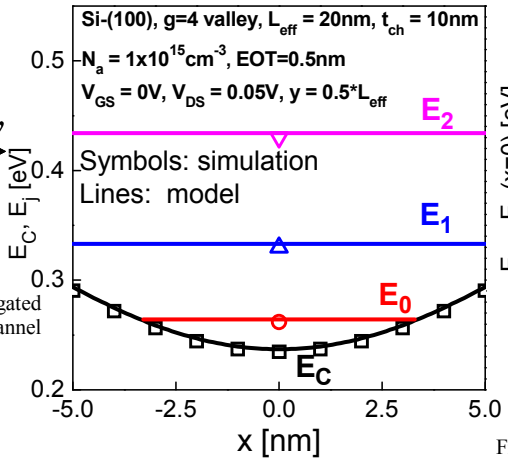


Fig. 2. Conduction band edge and quantized eigen-energies of a short-channel lightly-doped FinFET.

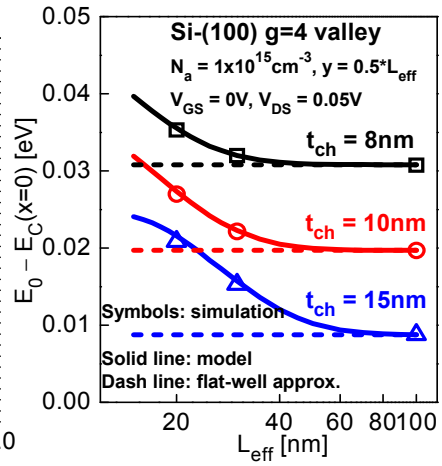


Fig. 3. Channel length dependence of the ground-state eigen-energy for lightly-doped FinFET with various t_{ch} showing the accuracy of our model.

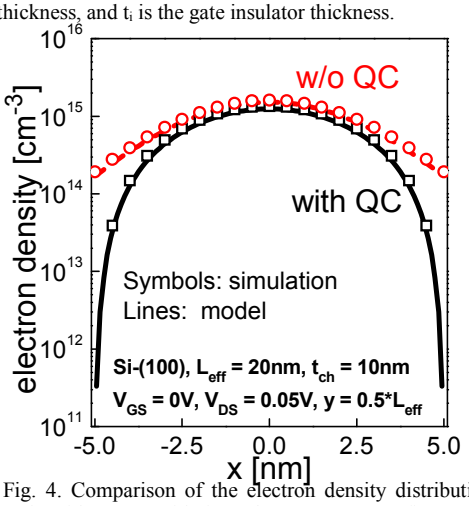


Fig. 4. Comparison of the electron density distribution with and without considering the quantum-confinement (QC) effect. The electron density is calculated from the 2-D DOS, eigen-energies, and wavefunctions

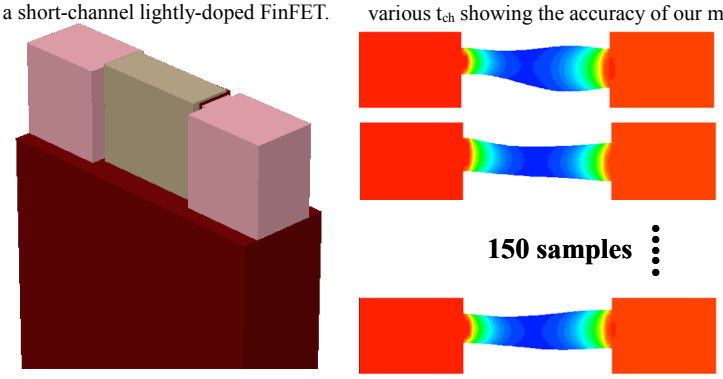


Fig. 5 The geometry of the nominal device used in our fin-LER simulation is W_{fin} = 7nm, H_{fin} = 20nm, L_{eff} = 25nm, EOT = 0.65nm. The sample number is 150.

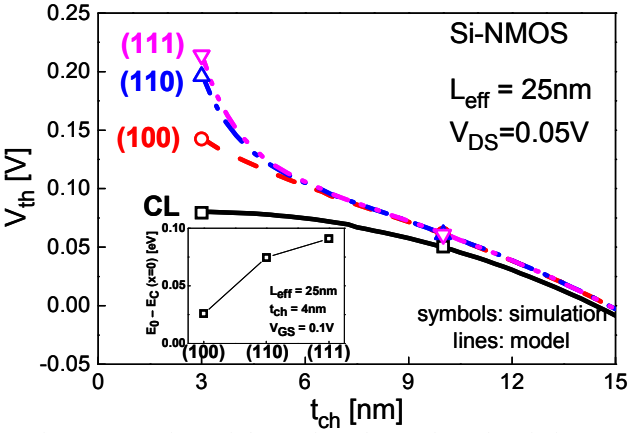


Fig. 6. Comparison of the t_{ch} dependence of V_{th} for Si-FinFET with various surface orientations and the classical model (CL). The V_{th} shift due to quantum confinement is mainly determined by the ground-state energy as indicated by the inset.

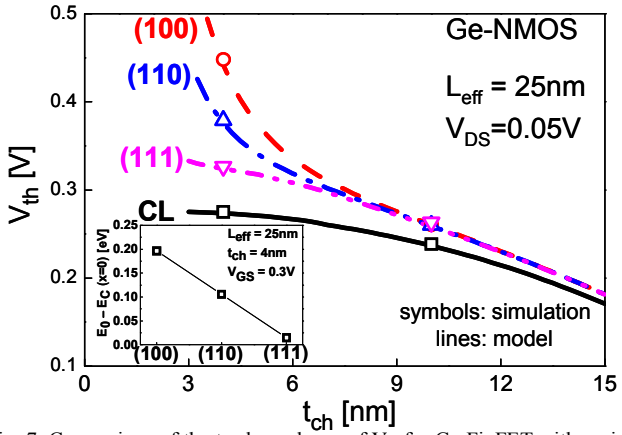


Fig. 7. Comparison of the t_{ch} dependence of V_{th} for Ge-FinFET with various surface orientations and the classical model (CL). The inset shows the comparison of the ground-state energy for various surface orientations.

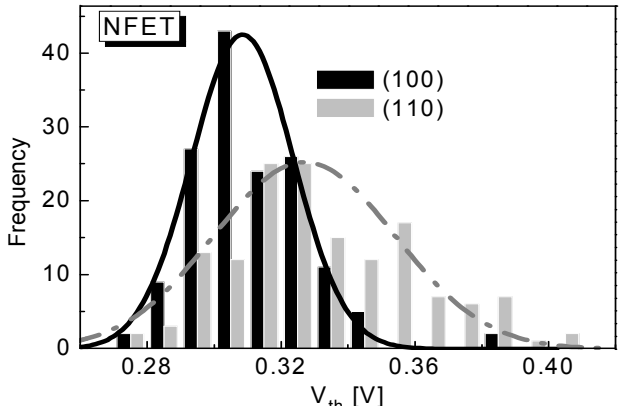


Fig. 8. The V_{th} of (110)-surface for Si-FinFET shows larger mean value and spread than those of (100)-surface.

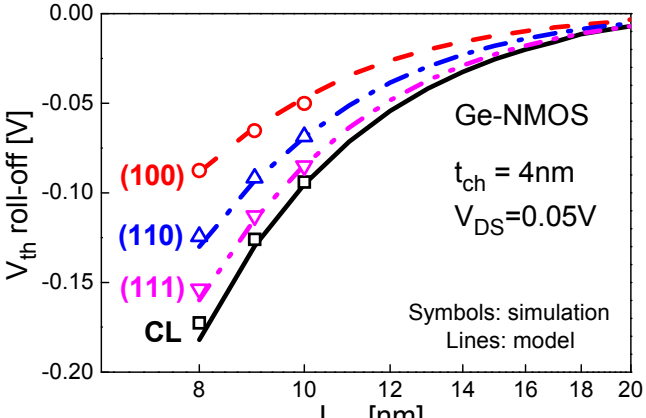


Fig. 9. Comparison of the L_{eff} dependence of V_{th} (V_{th} roll-off) for Ge-FinFET with various surface orientations and the classical model (CL).

無衍生研發成果推廣資料

98 年度專題研究計畫研究成果彙整表

計畫主持人：蘇彬	計畫編號：98-2221-E-009-178-
計畫名稱：前瞻矽奈米元件變異性及傳輸特性綜合研究(I)	

成果項目			量化			單位	備註（質化說明：如數個計畫共同成果、成果列為該期刊之封面故事...等）
			實際已達成數（被接受或已發表）	預期總達成數(含實際已達成數)	本計畫實際貢獻百分比		
國內	論文著作	期刊論文	0	0	100%	篇	
		研究報告/技術報告	0	0	100%		
		研討會論文	0	0	100%		
		專書	0	0	100%		
	專利	申請中件數	0	0	100%	件	
		已獲得件數	0	0	100%		
	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（本國籍）	碩士生	2	2	100%	人次	
		博士生	6	6	100%		
		博士後研究員	0	0	100%		
		專任助理	0	0	100%		
國外	論文著作	期刊論文	9	9	90%	篇	The 9 published journal papers supported by the NSC98-2221-E-009-178 project are all IEEE papers: (4 IEEE TED, 3 IEEE EDL, 2 IEEE TNANO).
		研究報告/技術報告	0	0	100%		
		研討會論文	7	7	70%		
		專書	0	0	100%	章/本	
	專利	申請中件數	0	0	100%	件	
		已獲得件數	0	0	100%		
	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（外國籍）	碩士生	2	2	100%	人次	
		博士生	6	6	100%		
		博士後研究員	0	0	100%		
		專任助理	0	0	100%		

其他成果 (無法以量化表達之成果如辦理學術活動、獲得獎項、重要國際合作、研究成果國際影響力及其他協助產業技術發展之具體效益事項等，請以文字敘述填列。)	獲 2010 年國立交通大學傑出人士榮譽獎勵.（考量過去五年（2005～2009）之綜合學術表現）

	成果項目	量化	名稱或內容性質簡述
科教處計畫加填項目	測驗工具(含質性與量性)	0	
	課程/模組	0	
	電腦及網路系統或工具	0	
	教材	0	
	舉辦之活動/競賽	0	
	研討會/工作坊	0	
	電子報、網站	0	
	計畫成果推廣之參與（閱聽）人數	0	

國科會補助專題研究計畫成果報告自評表

請就研究內容與原計畫相符程度、達成預期目標情況、研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）、是否適合在學術期刊發表或申請專利、主要發現或其他有關價值等，作一綜合評估。

1. 請就研究內容與原計畫相符程度、達成預期目標情況作一綜合評估

■達成目標

□未達成目標（請說明，以 100 字為限）

□實驗失敗

□因故實驗中斷

□其他原因

說明：

2. 研究成果在學術期刊發表或申請專利等情形：

論文：■已發表 □未發表之文稿 □撰寫中 □無

專利：□已獲得 □申請中 ■無

技轉：□已技轉 □洽談中 ■無

其他：(以 100 字為限)

在本計畫的 support 之下，我們的研究成果已發表在 9 篇 IEEE 期刊論文(4 篇 IEEE TED，3 篇 IEEE EDL，2 篇 IEEE TNANO)。

3. 請依學術成就、技術創新、社會影響等方面，評估研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）（以 500 字為限）

在本計畫中，我們對以矽為基底的前瞻奈米元件，針對其變異性及載子傳輸特性，進行綜合研究。在工作項目一中，我們探討使用應變矽(strained-Si)對元件匹配及變異特性的影響。這項研究不僅對使用先進 CMOS 元件的電路設計很重要，也有助於對奈米元件的本質參數變異的根本了解。在工作項目二中，我們針對不同應變程度的元件，藉由載子遷移率之溫度效應及低頻雜訊特性變化，探討應變對載子傳輸特性的影響。這項研究將有助於了解極微縮應變矽元件的戴子傳輸機制，也對未來提昇戴子遷移率的元件設計有所幫助。在工作項目三中，為提升鰭狀電晶體(FinFET)電路的效能，可改變通道表面方向以達到最佳化設計，本研究發展了一個包含量子侷限效應之解析理論模型，用以探討使用不同通道表面方向的矽及鍺材料鰭狀電晶體的變異性。我們的元件模型也將有助於未來極微縮鰭狀電晶體的設計。

在本計畫的 support 之下，我們的研究成果已發表在 9 篇 IEEE 期刊論文(4 篇 IEEE TED，3 篇 IEEE EDL，2 篇 IEEE TNANO)，可見本計畫的學術價值與績效是相當優異的。