A Simple Spacer Technique to Fabricate Poly-Si TFTs With 50-nm Nanowire Channels

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***Abstract*—In this letter, polycrystalline-silicon thin-film transistors (poly-Si TFTs) with 50-nm nanowire (NW) channels, which are fabricated without advanced photolithography by using a sidewall spacer-formation technique, are proposed for the first time. Because the polygate electrode is perpendicularly across poly-Si NW channels to form a trigatelike structure, the proposed poly-Si NW TFT owns outstanding gate controllability. In summary, a simple and low-cost scheme is proposed to fabricate high-performance poly-Si NW TFT suitable for future display manufacturing and practical applications.**

***Index Terms*—Nanowire (NW), polycrystalline silicon (poly-Si), sidewall spacer, thin-film transistors (TFTs), trigatelike structure.**

I. Introduction

POLYCRYSTALLINE-SILICON thin-film transistors (poly-Si TFTs) have attracted much considerable attention because they could be integrated with peripheral driving circuits on a low-cost glass substrate in active-matrix liquid-crystal displays [1], [2]. In addition, poly-Si TFTs have the potential to be used in 3-D circuits, including vertically integrated SRAMs [3] and DRAMs [4]. Recently, a lot of effort have been given to improve the gate controllability and device performance by changing device structure of poly-Si TFTs with complicated steps, such as the gate-overlapped lightly doped drain TFT [5], the double-gate TFT [6], and the gate-all-around TFT [7]. Moreover, poly-Si TFTs with nanoscale feature sizes have also been proposed to reduce the influence of the grain-boundary defects [8]–[12]. In these studies, the electrical performance of TFT could be remarkably improved by decreasing the channel dimensions to be comparable to, or still smaller than, the grain size. However, the poly-Si TFTs with narrow-width channels are directly defined by using costly electron-beam-lithography technology [8]–[10], which could not be practicable in flat-panel displays. On the other hand, for the poly-Si TFTs with nanowire (NW) channels and multiple-gate configuration reported in [11] and [12], the gate-induced drain-leakage (GIDL) current that resulted from large gate-to-drain overlapping area is high and must be addressed by additional processes. Furthermore, in order to form a trigate structure with NW channels, the extra top metal gate and bottom Si-substrate gate accompanied with high-temperature thermal-oxide and rapid-thermal processing are used [10], [11], which are difficult to process in liquid-crystal display (LCD) production line.

In this letter, we proposed a simple spacer technique to fabricate high-performance poly-Si TFTs. The self-aligned formation of twin poly-Si NWs with 50-nm linewidth is directly defined to serve as the channel regions without any expensive photolithography process. All processes are compatible with modern LCD production line and suitable for system-on-panel (SOP) applications in the future.

II. Device Fabrication

The major processes to fabricate the proposed poly-Si NW TFT by a sidewall spacer-formation technique are depicted in Fig. 1(a)–(e) shows the device top view. First, a 150-nm-thick SiN_X and a 100-nm-thick tetraethooxysilane (TEOS) SiO_X were consecutively deposited by plasma-enhanced chemical-vapor-deposition (PECVD) system to serve as the starting substrate and the dummy oxide layer, respectively. After patterning the dummy oxide stripe [Fig. 1(a)], a 100-nm-thick amorphous-silicon (α-Si) film was deposited by low-pressure CVD (LPCVD) [Fig. 1(b)] and, then, anisotropically etched to form α-Si spacer (namely, α-Si NW) in a self-aligned manner without extra mask or advanced photolithography system [Fig. 1(c)]. The feature size of the α-Si NWs could be well controlled by the thickness of α-Si film and the dry-etching condition. Next, a solid-phase-crystallization annealing was executed at 600 °C for 24 h in N_2 ambient to transform the α-Si into poly-Si. Then, the dummy oxide stripe was removed by buffered-oxide-etchant solution, and then, the square-coil poly-Si NW was reserved [Fig. 1(e)].

Afterwards, a 34-nm-thick TEOS gate oxide was deposited by PECVD system, and a 250-nm-thick phosphorus-doped poly-Si was then deposited by LPCVD system to serve as the gate electrode [Fig. 1(d)]. Subsequently, a self-aligned phosphorus-ion implantation was performed at the dosage and the ion energy of 5×10^{15} cm^{-2} and 15 keV, respectively, and then, the source/drain dopants were activated by an annealing treatment at 600 °C for 12 h in N_2 ambient. After depositing the passivation layer and defining the contact holes, the 500-nm-thick Al electrodes were deposited and then patterned

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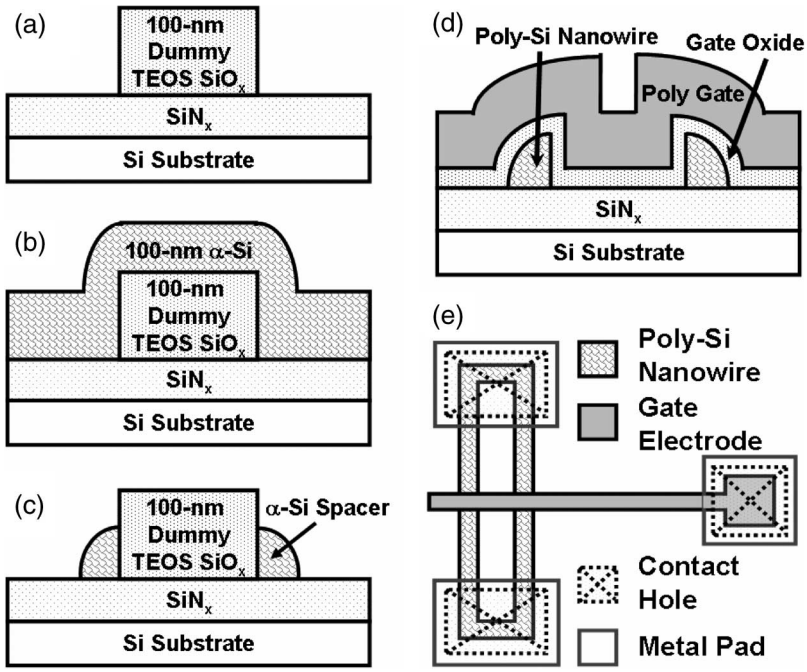

Fig. 1. (a)–(d) Cross-sectional views of the major processes to fabricate the poly-Si NW TFT. (e) Schematic top view of the proposed poly-Si NW TFT.

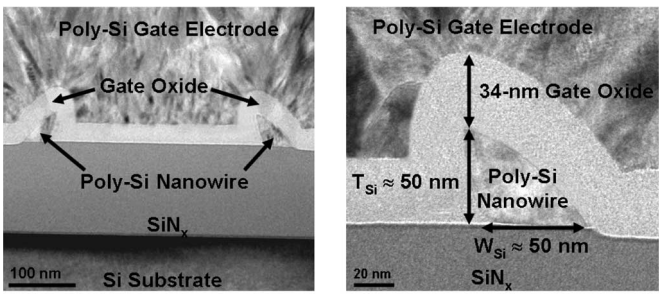

Fig. 2. (a) Cross-sectional TEM micrograph of the test structure of the proposed poly-Si TFT having a couple of NW channels with a 300-nm distance. (b) Fractional enlarging plot in (a).

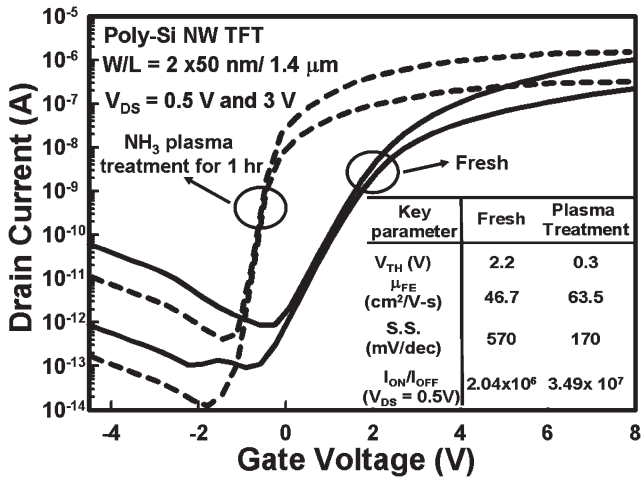

Fig. 3. Typical transfer characteristics of the proposed poly-Si NW TFT, with and without NH_3 plasma treatment for 1 h. The inset table is the electrical characteristics comparison of the poly-Si NW TFT, with and without NH_3 plasma treatment for 1 h.

[Fig. 1(e)]. Finally, a NH_3 plasma treatment was performed at 300 °C for 1 h to improve the device performance.

III. Results and Discussion

Fig. 2(a) shows the cross-sectional transmission-electron-microscopy (TEM) micrographs of the test structure of the proposed poly-Si TFT with NW channels. Here, such test structure with a small dimension of 300-nm distance is used to make the illustration clearer. The fractional enlarging plot of poly-Si NW channel is shown in Fig. 2(b). Because the polygate pattern is perpendicularly across poly-Si NW, a couple of active channels would be formed after removing the dummy oxide stripe in the proposed poly-Si NW TFT. From the cross-sectional TEM micrograph, the vertical sidewall thickness $(T_{\rm Si})$ and horizontal width $(W_{\rm Si})$ are approximately 50 nm. The aspect ratio $T_{\rm Si}/W_{\rm Si}$ of the active channel in the poly-Si NW TFT (approximately equals to one) is larger than that in the traditional planar TFT (much smaller than one). Such high aspect ratio means that the gate electrode forms in a trigatelike structure with well electrostatic controllability on channel potential due to sidewall and corner contribution effects [13], [14].

Typical transfer characteristics $(I_{\rm DS}-V_{\rm GS})$ of poly-Si NW TFTs, with and without NH_3 plasma treatment, are compared and shown in Fig. 3. The effective channel width of the poly-Si NW TFTs is defined as twice the horizontal width $(2 \times W_{\rm Si})$ of 100 nm parallel on the starting substrate, which is the same definition in other reports on TFT field [8]–[10]. The ON/OFF current $(I_{\rm ON}/I_{\rm OFF})$ ratio is the ratio of the maximum ON-state current to the minimum OFF-state current at

$V_{\rm DS} = 0.5$ V. The threshold voltage ($V_{\rm TH}$) is defined as the gate voltage required to achieve a normalized drain current of $I_{\rm DS} = (W/L) \times 100$ nA at $V_{\rm DS} = 0.5$ V. After NH_3 plasma passivation for 1 h, the threshold voltage is scaled down from 2.2 to 0.3 V, the field-effective mobility ($\mu_{\rm FE}$) can be improved from 46.7 to 63.5 $\rm cm^2/V \cdot s$, the subthreshold swing is also decreased from 570 to 170 mV/dec, and the ON/OFF current ratio could be increased one order of magnitude. In addition, the GIDL current could be suppressed near half order of magnitude at $V_{\rm DS} = 3$ V and $V_{\rm GS} = -4$ V. All of these devices' parameters are summarized in the inset of Fig. 3.

Besides excellent gate controllability due to 3-D trigate feature, the effect of grain boundaries in poly-Si NW film also plays an important role. As the poly-Si TFTs are scaled down, the number of grain boundaries is decreased to dominate on the $V_{\rm TH}$ decreasing [15], [16]. Therefore, in the poly-Si NW channel, the fewer grain boundaries make lower $V_{\rm TH}$ for ploy-Si TFT, which obtains higher driving current under the same operational condition. On the other hand, according to the poly-Si model [17], the effective mobility ($\mu_{\rm FE}$) could be given as

$$\mu_{\rm EF} = \frac{1}{1 + (\mu_G/\mu_{\rm GB})[nL_{\rm GB}/L]\exp[qV_b/kT]} \qquad (1)$$

where $\mu_{\rm FE}$ is the effective field-effect mobility, $L_{\rm GB}$ is the average grain-boundary length, $n = L/LG$ is the average grain-boundary number, and L_G is the average intragrain length. If the active channel is shrunk down to nanoscale dimension, the n value would be decreased to improved $\mu_{\rm FE}$ [15], [17]. Finally, fewer grain boundaries in poly-Si NW channel also make effectively passivated deep-states by NH_3 plasma treatment. Therefore, the high-performance poly-Si NW TFT with NH_3 plasma treatment could be achieved by utilizing a simple spacer-formation technology and suitable for LCD practical manufacturing.

IV. Conclusion

We have introduced a simple, low-cost, and self-aligned spacer technique to fabricate the poly-Si TFTs with NW channels in this letter. The 50-nm NW channel could be easily realized by anisotropically etched without extra mask or advanced photolithography system. The proposed poly-Si NW TFT has excellent gate controllability due to the trigatelike structure with the sidewall and corner contribution effects. Besides, the fewer grain boundaries in poly-Si NW channel also improve the electrical characteristics of TFT, even including the effectively passivated deep-states by plasma treatment. Therefore, the proposed poly-Si NW TFT is highly suitable for realizing SOP applications.

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