行政院國家科學委員會專題研究計畫 成果報告

奈米點記憶體元件之製作與物理機制研究(2/2)
研究成果報告(完整版)

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中 華 民 國 99 年 09 月 06 日

行政院國家科學委員會補助專題研究計畫 ■成果報告 □期中進度報告

奈米點記憶體元件之製作與物理機制研究(2/2)

計畫類別：■個別型計畫　□整合型計畫

計畫編號：NSC 98-2221-E-009-001

執行期間：2009/08/01 ~ 2010/07/31

執行機構及系所：交通大學

計畫主持人：施敏

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中　華　民　國　99 年　8 月　1

行政院國家科學委員會補助專題研究計畫期中報告

奈米點記憶體元件之製作與物理機制研究(2/2)

執行期限：2009/08/01 ~ 2010/07/31

計劃編號: NSC 98-2221-E-009-151-

計劃主持人: 交通大學電子工程學系及電子研究所 施敏 教授

1、中文摘要

傳統非揮發性記憶體的基本構成單元主要是由多晶矽(poly-Si)浮閘(floating gate)元件所構成，為了使得非揮發性記憶體元件有更高操作速度，包覆多晶矽的氧化層需要向下微縮。然而，這使得多晶矽層內所儲存的電子更容易遺失，導致記憶特性的消失。為了同時達到高速操作以及長久記憶特性的要求，具有分離式與高密度儲存中心的奈米點記憶體被提出為解決的方法。奈米點記憶體除了能同時達到非揮發性與高速及低能損操作的要求之外，同時奈米點記憶體的製程與現有之半導體製程完全相容，而被視為下世代非揮發性記憶體。

透過金屬奈米點本身具的高度儲存狀態(density of state)以及強耦合能力，可使得奈米點記憶體能在小電壓操作下即可獲得能夠邏輯電路辨別之記憶準位，而達到高速操作的特性。

本計畫主要的目標是非揮發性奈米點記憶體之製作與物理機制研究。第一年將針對金屬、金屬矽化物與磁性材料物奈米點結合高介電常數絕緣層之製作研究，此外，並建立DLTS 以及記憶體元件之模擬與量測分析技術。計畫的第一年將利用各種不同的金屬、金屬矽化物與磁性材料物質結合高介電常數之絕緣物質以製作出金屬性奈米點(W、Mo、Co 與 Ni 等)於高介電常數絕緣層中可有效的增加元件的操作效率。金屬性奈米點本身因具有高功函數以及強耦合能力，結合高介電常數物質絕緣層所具有之高介電常數特性進而改善電荷儲存的效率與分析奈米點儲存之物理特性。我們將利用半導體相關的低溫製程以形成奈米點，以期能應用於薄膜電晶體顯示器產品。後處理製程如氫電漿、氨電漿與超臨界處理等將研究以改善奈米點本身的穩定度與可靠度。第二年將針對元件結構改進之製作研究，並將驗證奈米點記憶體的技術於場效應電晶體以及薄膜電晶體。我們將利用第一年的研究成果，對記憶體元件結構改進，如多層奈米點等之研究以提升奈米點記憶體元件的儲存能力並瞭解奈米點儲存之物理機制。最後，將奈米點與場效應電晶體以及薄膜電晶體整合，並針對各種寫入機制與記憶體特性作探討。本計

畫著重於兩部分，一為奈米點記憶體結合高介電常數物質之元件的製作與後處理製程的影響，另一為奈米點記憶體之物理特性探討。利用量測電流電壓特性(IV)與電容電壓特性(CV)並搭配X-Ray光電子能譜圖(XPS)、二次離子質量頻譜

(SIMS)與穿透式電子顯微鏡(TEM)等對所形成之奈米點做物性的探討。最後歸納奈米點記憶體元件的電特性與材料之間的關係，建立完整的奈米點記憶體元件資料庫與其物理機制。

關鍵詞：非揮發性記憶體；奈米點記憶體；高介電係數材料

Abstract

Recently, nanocrystals (NCs) memory has received much attention due to its discrete charge storage centers and physics originate from nano scale. It is well know that the unit cell of non-volatile memories (NVMs) is constructed with continuous floating gate (FG) embedded in silicon oxide. In order to gain high operation speed and low power consumption, the oxide layer has to be scaled down. The nanocrystal memory was proposed as the solution for these conflict requirements due to its properties of discrete charge storage centers and high density of storage states. The recent researches indicate that the metal NCs have advantages of high density of states and stronger coupling with conduction channel, which enable the device operation in low voltage and high speed.

This project focuses on the fabrication of nanocrystals memory device and investigation on their relevant physical characteristics for application on the novel nonvolatile memory devices. In the first year, we will fabricate NCs composed of several metal materials like W, Pt, as well as metal silicide materials like Ni_2Si, NiSi, $NiSi_2$, Co_2Si, CoSi, $CoSi_2$ or magnetic metals like Co, Ni, etc. Various high-k materials will be combined with NCs to further enhance the device performance. Post treatment process including H_2 plasma, NH_3 plasma and supercritical fluid will be investigation to improve reliability of NCs memory device. The project is mainly divided into two parts, one is fabrication and formation of NCs device and the other is investigation of physics of NCs device。The IV and CV measurement is employed for investigation of electrical properties. XPS, SIMS and TEM are utilized for material analyses. Finally, we will summary the results of electrical and material analyses into complete database for fabrication and physics of NCs memory.

Keywords: nonvolatile memory, nanocrystal memory, high-K dielectric materials

2 、Introduction

Flash memory (Flash memory) of the invention on behalf of the origin in the year 1960. At that time, the electronic information stored on magnetic core memory (magnetic-core memory)-based, nuclear magnetic memory as a result of the high cost of large volume and high power, in order to replace nuclear magnetic memory, I and Dr. Kahng co-invented the first stop floating (floating-gate) non-volatile memory at Bell Labs in 1967.

Today, flash memory (Flash memory) has a non-volatile memory structure of the main flow, its extensive use in personal computers, as well as two aspects of embedded memory. In recent years, with consumer electronics products pandemic and portable electronic products can quickly universal in all families, one of the most important factor is the use of convenient flash memory high-provincial electricity, high-density and lightweight characteristics of earthquake. Traditional non-volatile memory for the main structure of floating gate polysilicon (poly-Si float gate), as shown in Figure 1.

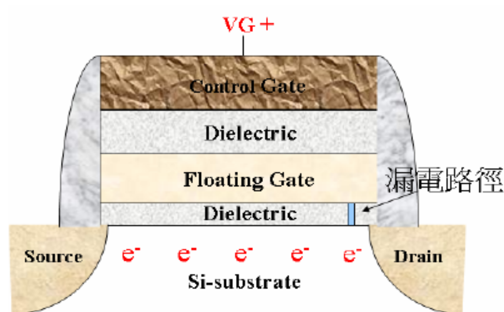

Figure 1.Floating ate memory device

Plus the gate bias, the carrier of silicon plate can be gained large enough kinetic energy to tunnel tunneling oxide by FN and storage in the poly-crystal floating gate (floating gate). Removing the power supply in addition, the carrier in the floating gate don’t have enough kinetic energy to tunnel to substrate and cause limited sub-set of the floating gate, and then have a flat-band voltage of the translation, so that threshold voltage changes. There are different bits of the power flow for the detection of quasi-circuit judge to the effect of memory.

With non-volatile memory in the large capacity, high-speed and low energy loss of the request, the floating gate memory and between the silica substrate (Tunneling oxide layer) need to microfilm down. However, scaling down the tunneling oxide layer made floating gate non-volatile memory components to face the inevitable clinical challenge. That is, in a number of components after the operation, making leaks easily track circuit was produced in the tunneling oxide layer, once formed by the leakage of electrical path connected floating gate and substrate, stored in the floating gate of the carrier will then be through this path and all is lost, lead to the loss of memory effect. In recent years, nanocrystals have been applied to non-volatile memory (Figure 2), to solve the traditional poly-crystal silicon floating gate memory (eg, flash memory) scaling down problem. Different from

the continuous conduction of the floating gate, the charge storage center (nanocrystals) was separate. After several rounds of the components read data from and after the write process, the tunneling oxide layer caused by leakage circuit track, even with some linked nanocrystals, it will only result in the storage part of the loss of the carrier. It is still non-volatile memory the characteristics of

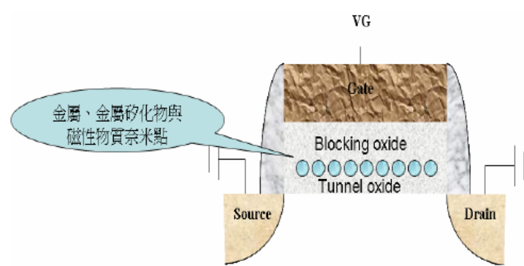

Figure 2.Structure of nanocrystal memory

The purpose of this research lies in the production and research components nanocrystals memory. In addition to nanocrystals process to do, the relevant simulation and physical components will also be a plan to carry out.

The program will target metal and magnetic materials nanocrystals combined with the high-K dielectric isolation layer improve the characteristics of memory. Using common variety of semiconductor processing process, such as hydrogen and supercritical fluid application improve the reliability of nanocrystals memory as retention and endurance. Low-temperature process to form nanocrystals will be the plan to study. It is helpful to develop and apply on thin film transistor displays. With continuing scaling down, in order to increase the reliability and stability, multi-layered structure of the storage layer will also be in this research program was to increase the density of nanocrystals. Finally, we will be formed by the integration of nanocrystals to the MOSFET and TFT to verify the actual nanocrystals memory components as a non-volatile memory components feasibility.

3、Result and Discussion

(3.1 Charge storage characteristics of Mo nanocrystal)

3-1-1 (Experiment)

The memory cells were fabricated on 6 in. *p*-type Si substrate. After the substrate was cleaned with standard Radio Corporation of America process, a 5-nm-thick dry oxide was thermally grown at 950 °C on the substrate in a horizontal furnace. An 8-nm-thick Mo silicate layer was subsequently deposited on the oxide layer by cosputtering Mo and Si in Ar (24 SCCM)/O (2 SCCM) (SCCM denotes cubic centimeter per minute at STP) ambience. A 30-nm-thick Si oxide as the control oxide was deposited on the Mo silicate layer by plasma enhanced chemical vapor deposition (PECVD) at 300 °C. Thermal annealing process was performed in N_2 ambience at 900 °C at 60 s to form Mo nanocrystals embedded in SiO_x. Cells were then treated with NH3 plasma in PECVD chamber for 30 min with a NH_3 gas flow rate of 20 SCCM and the chamber pressure of 67

torr at power of 50 W. To measure the electric characteristics, a 500-nm-thick Al was thermally evaporated through a shadow mask on the control oxide to form the metal-oxidesemiconductor (MOS) structure. The x-ray photoemission spectroscopy (XPS) was adopted to analyze the chemical bonding and composition of the charge storage layer. Electrical characteristics were measured using Keithley4200 and HP4284 Precision *LCR* meter.

3-1-2 (Discussions)

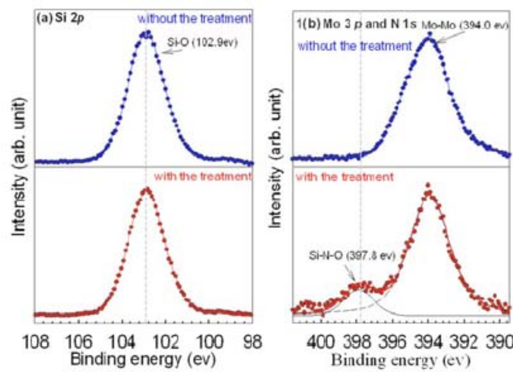

FIG. 3. (Color online) (a) Si 2*p*, (b) Mo 3*p*, and N 1*s* core-level spectra of the charge storage layer composed of Mo nanocrystals embedded in SiO*x* with and without the plasma treatment.

Figure 3 shows the XPS spectra of the charge storage layer with and without the plasma treatment, which was performed

by using a monochromatic Al *K*α(1486.6 eV) x-ray. Figure 3(a) shows the XPS Si 2*p* spectra of the charge storage for the sample with and without the plasma treatment.

For the sample without the treatment in Fig. 3(a), the peak position of XPS Si 2*p* situated at 102.9 eV indicates that the surrounding oxide of nanocrystals is SiO*x*.[1] There is no obvious difference in the peak positions between the samples with and without the treatment. However, it was found that an additional XPS peak (397.8 eV) appears in the Mo 3*p* and N 1*s* spectra of the charge storage layer after the plasma treatment, which indicates that the incomplete bonds in SiO*x* bonded with nitrogen after the plasma treatment, as shown in Fig. 3(b).[2]

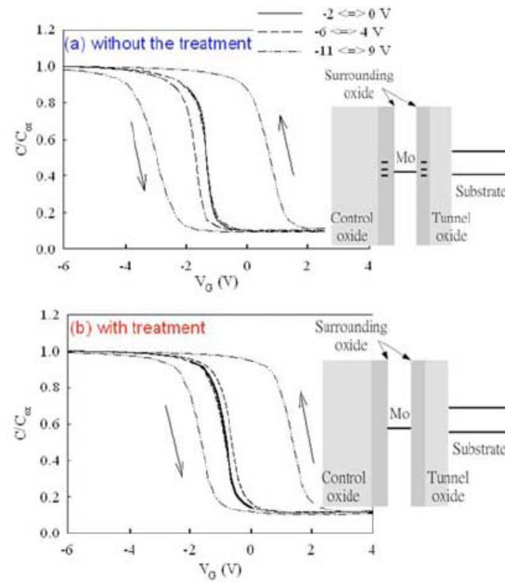

FIG. 4. (Color online) *C-V* curves of the MOS structure with and without the plasma treatment. The inset of the is the simple band diagram of the structure in the flat-band state.

Figures 4(a) and 4(b) show the *C-V* curves of MOS structure embedded with Mo nanocrystals for the sample with and without the plasma treatment, respectively. At the smaller sweeping voltage of 2 V, there is a negligible memory window in Figs. 4(a) and 4(b) corresponding to the quasineutral state (i.e., no charge is stored in the charge

storage layer under this sweeping range). At the larger sweeping voltages, there are counterclockwise memory hystereses in Fig. 4. The counterclockwise hystereses are due to carrier transport through tunnel oxide between the charge storage layer and the Si substrate. We note that the memory windows of the sample with the plasma treatment are smaller than that without the treatment. For the smaller memory window after the treatment, we speculate the nitrogen passivation in the charge storage layer. It has been suggested that the traps in the oxide around nanocrystals can capture carriers and contribute to the memory window.[3-4] According XPS results, the nitrogen was incorporated into the oxide around the Mo nanocrystals after the treatment. The incorporated nitrogen can passivate the traps in the oxide, which reduces the charge storage centers and leads to the smaller memory window, as indicated in the insets of Fig. 4.

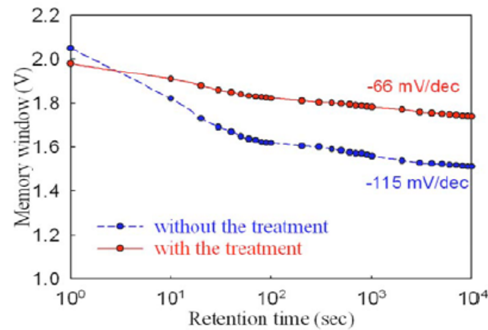

FIG. 5. (Color online) The retention behavior of the MOS structures with and without the plasma treatment.

Figure 5 is the comparison of the retention behavior for the samples with and without the plasma treatment. The retention was measured by a stress voltage of 10 V on Al gate electrode for 5 s. The memory window was obtained by comparing the *C-V* curves after the programming to the quasineutral state. It can be found in Fig. 5 that, after the 103 s retention time, the decay rate (-66 mV/decade) of the memory window for the sample with the plasma treatment is slower than that without the treatment (-115 mV/decade).

The superior retention of the sample with the treatment can be explained by the nitrogen passivation of the traps in the oxide around Mo nanocrystals. When charges are stored in the nanocrystals, the stored charges can escape with the assistance of traps _traps assist tunneling_ in the surrounding oxide. Because the traps in the oxide were reduced after the plasma treatment, the retention was improved by suppressing the trap assisted tunneling process.

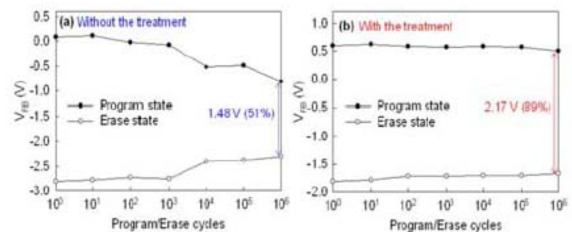

FIG. 6. (Color online) Endurance characteristic of the MOS structures (a) with and (b) without the plasma treatment.

Figures 6(a) and 6(b) presents the endurance characteristics of the samples with and without plasma treatment under the pulse conditions of V_G=-15 V for 1 ms, respectively. In Fig. 6(a), the $\triangle V_{FB}$ (the difference in V_{FB} between

programming and erase states) reduced significantly, and the $\triangle V_{FB}$ remained 51% after 106 program/erase cycles. However, the plasma treated sample exhibits robust endurance characteristic ($\triangle V_{FB}$ of 89% after 106 program/erase cycles). It is known that the $\triangle V_{FB}$ reduction during the endurance test is due to the degradation of the gate oxide.[5]

The better endurance characteristics of the sample with the plasma treatment can be attributed to the improvement of quality of the surrounding oxide. During the endurance test, the carriers transport between nanocrystals and the substrate can damage the surrounding oxide, which produces more traps. Because the surrounding oxide was strengthened by the nitrogen incorporation after the treatment, the generation rate of traps reduced, resulting in the better endurance characteristic.

3-1-3 (Conclusion)

The nonvolatile memory characteristics of the Mo nanocrystals were influenced by the ammonia plasma treatment. The *C*-*V* hysteresis reduced to 3.0 V and retention characteristic improved with decay rate of -66 mV/decade after the plasma treatment due to the nitrogen passivation of the traps in the oxide around the nanocrystals. The incorporation of nitrogen into the charge storage layer through the NH_3 plasma treatment can strengthen the endurance characteristic of Mo nanocrystals memory.

(3.2 $NiSi_2/SiN_X$ nanocrystals for nonvolatile memory devices)

3-2-1 (Experiment)

This memory-cell structure was fabricated on a 6 inch p-type silicon (100) wafer. After a standard RCA process which removed native oxide and micro-particles, a 4.5-nm-thick tunnel oxide (SiO2) was thermally grown by a dry oxidation process in an atmospheric pressure chemical vapor deposition furnace. Subsequently, three type structure of $NiSi_2$ charge-storage layer was fabricated to compare. About 5~7 nm thick NiSi2 layer was deposited for single-layer (sample A) and double-layer (sample B) nanocrystal storage structure with only Ar 50 sccm. The sample A was also used to be control sample and the two nanocrystal storage layer of sample B was separated by about 3 nm PVD oxide (SiO_2). The other structure is also about 5 nm thick nanocrystal storage layer sputtering in the mixture gas of Ar (50sccm) and NH3 (10 sccm) at room temperature to induce the nitride based trap (sample C). After that, about 30nm SiO_2 was deposited as control oxide. Nanocrystals can be isolated well and the oxide quality can be improved by rapid thermal anneal in O_2 ambiance. Finally, the bottom and top Al electrode was patterned to form the MOS transistors.

3-2-2 (Discussions)

To confirm the formation of nanocrystal, the cross-sectional transmission electron microscope images of the single-layer

(sample A) and double-layer (sample B) structure nanocrystal without reaction gas are shown in Fig. 1(a) and Fig. 1(b), respectively. Obviously, NiSi2 atoms are activated and self-assembled into separate and granular NCs after 700℃ RTA process in O2 ambient. The densities of nanocrystal for sample A and B are estimated to be 2.73×10^{12} cm-2 and 1.43×10^{12} cm-2, and the nanocrystal diameters are about 5 nm and 7 nm. The low resolution TEM images are shown in the inset of Fig. 1(a) and Fig. 1(b).

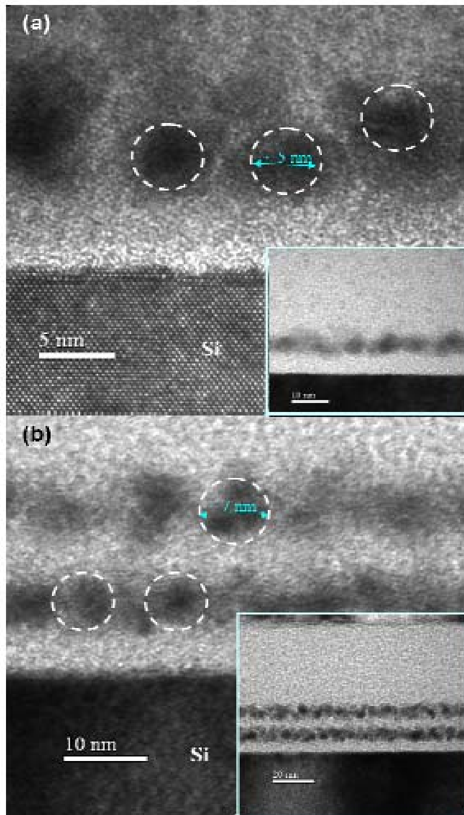

Fig. 1 Cross-sectional transmission electron microscope of (a) single-layer NiSi NCs , and (b) double-layer NiSi NCs embedded in the SiO2. The insert pictures are the low resolution TEM images.

Fig. 2(a) and Fig. 2(b) show the C-V hysteresis of sample A and sample B, and indicate the memory windows under ±4MV/cm operation are 2.5V and 8.6V, respectively. The memory window of device with double-layer structure is larger than that with single-layer structure due to the fact that more charge storage traps in double-layer structure. Although 0.5V memory window is large enough to identify logic “1” or “0” state, memory device with a larger memory window can stand more electrons loss from the nanocrystal charge storage layer and avoid misidentification.

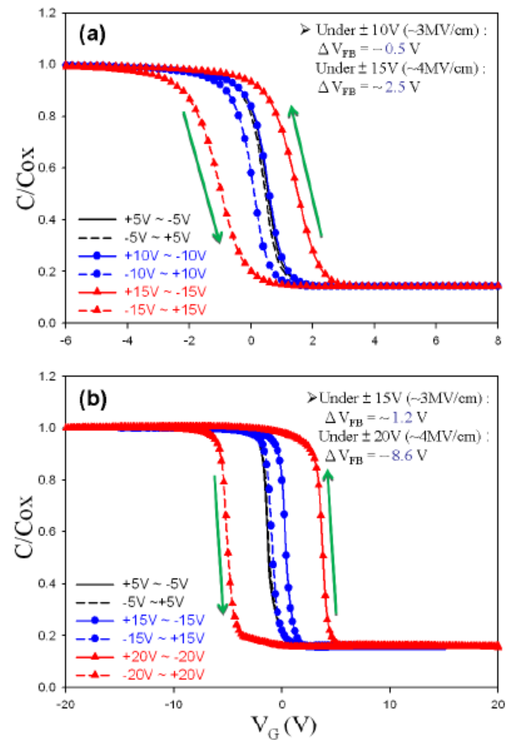

Fig. 2 Capacitance-voltage (*C-V)* hysteresis characteristics of memories with (a) single-layer and (b) multi-layer NCs. The memory windows of (a) 2.5 V and (b) 8.6 V can be obtained under about ± 4MV/cm operation, respectively

Figure 3(a) and Figure 3(b) show the threshold voltage shifts (ΔV_T) from flat

band with pulse time for samples A and B. Comparing with sample A, sample B still has an equal memory window even it is operated with a smaller effective electric field.

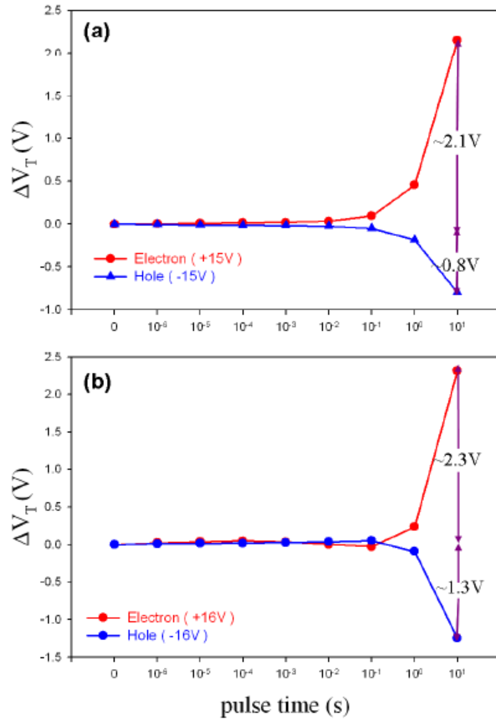

Fig. 3 Electron and hole injection induced threshold voltage shift (ΔV_T) from flat band with pulse time for devices with (a) single-layer and (b) double-layer nanocrystal structures.

Figure 4(a) and Figure 4(b) show the retention characteristics of the samples A and B, respectively. It can be seen that the decay ratio of sample B is large than that of sample A. Because the coulomb blockade effect induced by the electrons stored in the first layer (the closer layer from Si substrate) can exclude the electrons stored in the second layer (the further layer from Si substrate) from leaking back to the substrate, the stored carrier can be improved from 49.9% (sample A) to 58.7% (sample B) until 10^4 sec in room temperature.

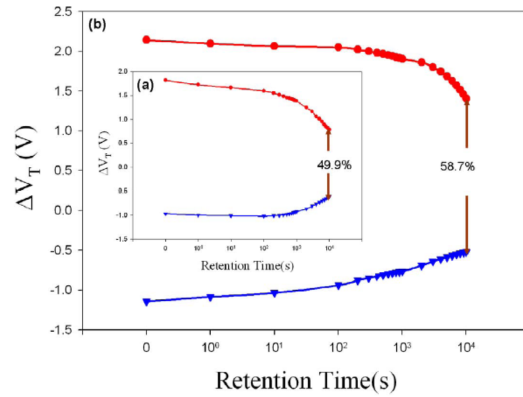

Fig. 4 Retention characteristics of (a) single-layer and (b) double-layer nanocrystal structure at room temperature. The device with double-layer structure has better retention characteristic, 58.7%, at 104 sec than that for single-layer device because of coulomb blockade effect.

In order to combine the advantages of nonvolatile nanocrystal memory (NVM) and metal/oxide/nitride/oxide/silicon (SONOS) memory, we integrate the nitride traps with $NiSi_2$ nanocrystal by simply reactive sputtering $NiSi_2$ in the mixture gas of argon (Ar) and ammonia (NH_3) at room temperature (sample C). The C-V curves of sample C are shown in Fig.5(a), and the memory window under ±15V operation is about 2V, which is not much different from sample A. The cross-sectional transmission electron microscope images are also shown in Fig. 5(b), and the density and diameter of nanocrystals are estimated to be $1.23\times10^{12}cm^{-2}$ and 5nm, respectively.

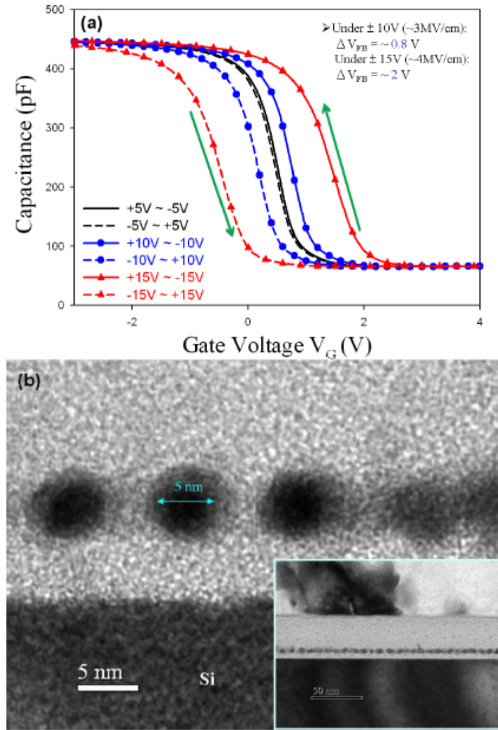

Fig. 5 (a) *C-V* hysteresis characteristics and (b) TEM photographs of memory with NiSi2/SiNX compound nanocrystals (CNCs) structure. The memory window under ± 4MV/cm operation is about 2V , and the nanocrystal diameter is identified about 5nm.

As shown in Fig. 6(a), the photoelectron spectra of Ni 2p3/2 of sample C can be separated to two peaks with center at 853.1eV and 855.6eV by fitting with Lorenzian-Gaussian functions. Due to the fact that the bond dissociation energy of Ni-Si (318 kJ·mol-1) is much less than that of N-Si (437.1 kJ·mol-1) , the Ni-Si bond tends to dissociate and react with nitrogen to form the bond of Ni-Si-N and Si-N during sputtering. Hence, the peak with center at 855.6 eV is attributed to the bond Ni-Si-N. As shown in Fig. 6(b), the photoelectron spectra of N 1*s* of sample C also verified the nanocrystals were composited of N-Si bonding (397.9 eV) and N-Si-Ni (396.8) again. According to the X-ray photoelectron spectra analyses above, it could be judged that the nanocrystals components of sample C are composed of $NiSi_2$ and SiNX with minor inclusion of NiSiN ternary alloy.

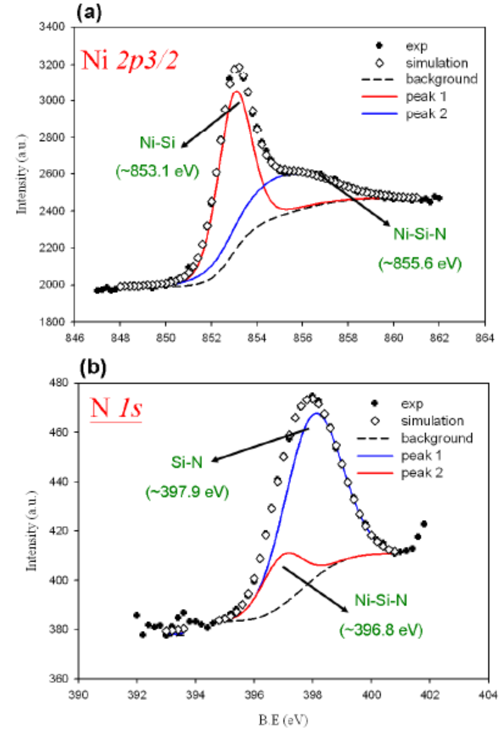

Fig. 6 Peak analyses of XPS spectrum of (a) Ni 2*p*3/2 and (b) N 1*s* for sample C with NiSi2/SiNX CNCs structure.

The threshold voltage shifts (△V_T) from flat band with pulse time for sample C were also shown in Fig. 7(a). The threshold voltage shifts caused by electrons and holes injecting under ± 15V for 10 seconds are about 2.0V and 0.9V, respectively. It is noteworthy that the marked electrons and holes injection happened as the pulse time increases 10-3~10-2 seconds, indicating that the programming and erasing efficiencies of sample C is higher than that of sample A and sample B.

To investigate the storage ability of

memory device of sample C, the retention characteristic is shown in Fig. 7(b). Since the structure of $NiSi_2/SiN_x$ CNCs is formed in sample C, the additional potential barrier of nitride can reduce the tunnel probability significantly and the traps contributed by nitride can be used as memory storing centers. Furthermore, the hydrogen atoms which were dissociated from NH_3 during depositing nanocrystal charge storage layer could passivate the shallow traps of nitride. On account of the deep traps being well below 0.7 eV, the carriers trapped in deep traps were hard to escape during retention test. Hence, in spite of the endurance test has been implemented before the retention test, the decay ratio of memory window for 10^4 seconds is still better than sample A and B in room temperature. According to the retention results, the proposed device with $NiSi_2/SiN_x$ CNCs structure indeed exhibits superior reliability than traditional single-layer or even double-layer nanocrystals device.

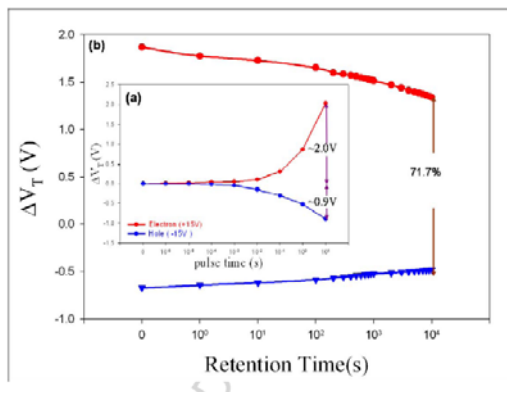

Fig. 7 (a) Electron and hole injection induced threshold voltage shift with pulse time, and (b) Retention characteristic after endurance test at room temperature. The retention characteristic is still better than double-layer structure (sample B) even undergoing endurance test.

3-2-3 (Conclusion)

We have fabricated double-layer (sample B) NCs and $NiSi_2/SiN_X$ CNCs (sample C) as comparison samples with single-layer (sample A) to investigate the improvement of reliability based MOS memory capacitor. Since the coulomb blockade effect, the nanocrystal device with double-layer structure improves the charge retention performance indeed. This study also incorporates nitrogen into $NiSi_2$ layer by sputtering in NH_3 ambience, and the $NiSi2/SiN_X$ CNCs can be easily formed after rapid thermal annealing. Comparing with double-layer device, the nitride layer surrounding NiSi nanocrystals can provide the additional tunnel barrier and deep traps to further improve the charge retention characteristic. The combination of nitride based traps with nanocrystal by simple process indeed can provide superior memory reliability for next generation and high-integrated NVM applications.

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5. 計畫成果自評

本計劃今年度延續去年奈米點元件記憶體特性及可靠度，以解決傳統浮停夾微縮問題, 已經完成了Mo奈米點之製作及電漿處理對於增加其非揮發性記憶體之可靠度特性有明顯有效的成果, 且我們成功發展奈米點及高介電常數材料之整合與多層奈米點之發展及不同處理方式如超臨界流體處理對奈米點非揮發性記憶體之影響，相關成果已整理並逐步發表於國際期刊上。

無研發成果推廣資料

98 年度專題研究計畫研究成果彙整表

計畫主持人：施敏　　計畫編號：98-2221-E-009-001-

計畫名稱：奈米點記憶體元件之製作與物理機制研究(2/2)

成果項目			量化：實際已達成數（被接受或已發表）	量化：預期總達成數(含實際已達成數)	量化：本計畫實際貢獻百分比	單位	備註（質化說明：如數個計畫共同成果、成果列為該期刊之封面故事...等）
國內	論文著作	期刊論文	0	0	100%	篇	
		研究報告/技術報告	0	0	100%		
		研討會論文	0	0	100%		
		專書	0	0	100%		
	專利	申請中件數	0	0	100%	件	
		已獲得件數	0	0	100%		
	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（本國籍）	碩士生	0	0	100%	人次	
		博士生	0	0	100%		
		博士後研究員	0	0	100%		
		專任助理	0	0	100%		
國外	論文著作	期刊論文	0	0	100%	篇	
		研究報告/技術報告	0	0	100%		
		研討會論文	0	0	100%		
		專書	0	0	100%	章/本	
	專利	申請中件數	0	0	100%	件	
		已獲得件數	0	0	100%		
	技術移轉	件數	0	0	100%	件	
		權利金	0	0	100%	千元	
	參與計畫人力（外國籍）	碩士生	0	0	100%	人次	
		博士生	0	0	100%		
		博士後研究員	0	0	100%		
		專任助理	0	0	100%		

其他成果 (無法以量化表達之成果如辦理學術活動、獲得獎項、重要國際合作、研究成果國際影響力及其他協助產業技術發展之具體效益事項等，請以文字敘述填列。)	無

	成果項目	量化	名稱或內容性質簡述
科教處計畫加填項目	測驗工具(含質性與量性)	0	
	課程/模組	0	
	電腦及網路系統或工具	0	
	教材	0	
	舉辦之活動/競賽	0	
	研討會/工作坊	0	
	電子報、網站	0	
	計畫成果推廣之參與（閱聽）人數	0	

國科會補助專題研究計畫成果報告自評表

請就研究內容與原計畫相符程度、達成預期目標情況、研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）、是否適合在學術期刊發表或申請專利、主要發現或其他有關價值等，作一綜合評估。

1. 請就研究內容與原計畫相符程度、達成預期目標情況作一綜合評估

■達成目標

□未達成目標（請說明，以 100 字為限）

□實驗失敗

□因故實驗中斷

□其他原因

說明：

2. 研究成果在學術期刊發表或申請專利等情形：

論文：□已發表 □未發表之文稿 □撰寫中 ■無

專利：□已獲得 □申請中 ■無

技轉：□已技轉 □洽談中 ■無

其他：（以 100 字為限）

3. 請依學術成就、技術創新、社會影響等方面，評估研究成果之學術或應用價值（簡要敘述成果所代表之意義、價值、影響或進一步發展之可能性）（以 500 字為限）

堣耵杞傳肆郥磎擊吣肆晇皕濼�van唏梅積鐎灢儌蕠咨靠瓔ㄛ鳺刋抻闇巘摵憤唫瘎纋菏藺,䲧柃駍僁瑦 Mo 晇皕濼巃罸簋蕠赽斸蠺黖厬槲嚦吤剢猼漽蕍儌梅積鐎巃咨靠瓔灢儌膧晱皻膧湘鍌僁咥,韓鋳滑僁佞蕍霶晇皕濼蕠邴佪赽堇稃謏儚巃曚╪瑮竘鹠晇皕濼巃蕍霶蕠楙婞蠺黖菾蔙濆廲櫸衻蕓鐎蠺黖厬晇皕濼猼漽蕍儌梅積鐎巃蝭匯ㄛ葯巹僁咥䲧曚逘並穖勑蕍礲槲玿藫悢巠葞〔