

Three-dimensional simulation studies on electrostatic predictions for carbon nanotube field effect transistors

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Abstract

Analysis of the electrostatic characteristics and the gate capacitance of typical nanostructured carbon nanotube field effect transistors (CNT-FETs) were performed numerically. A previously developed parallelized electrostatic Poisson's equation solver (PPES) is employed, coupled with a parallel adaptive mesh refinement (PAMR) to improve the numerical accuracy near the region where variation of potentials are significant. CNT-FETs with four typical configurations of the gate electrode, the bottom gate (BG), the double gate (DG), the top gate (TG), and the surrounding gate (SG) were simulated. Effects of the nanotube arrangement and the gate length on the gate capacitance are presented and discussed. The simulation results show that SG-CNTFET possesses the largest gate capacitance among various structures. However, TG-CNTFET is recommended for practical applications by taking into account both the device performance and the difficulty of fabrication. According to the simulated gate capacitance, estimation of the on-state current of CNTFETs is possible.

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1. Introduction

Since carbon nanotubes (CNTs) were first discovered by S. Iijima in 1991 [1], there has been increasing interest in the study of its superior material and electrical properties [2,3]. Due to their unique electrical properties, CNTs represent a promising alternative to conventional silicon technology for future nanoelectronics. The first realization of CNT field effect transistors (CNTFETs) originated from S. Tan's pioneering work in 1998 [4], and since then various new CNTFETs with different device structures and gate configurations have been proposed [5–8]. Until now, several gate configurations were proposed for CNTFETs, such as the bottom gate (BG) [5,6], the double gate (DG) [7], the top gate (TG) [8,9], and the surrounding gate (SG) [10]. For the bottom gate structure, the CNT array is placed on a silicon substrate covered by a high-quality, ultra-

thin silicon dioxide (SiO_2) layer that serves as the gate dielectric with a planar bottom gate electrode located under silicon dioxide layer, as shown in Fig. 1(a). This architecture provides an easier way for the device fabrication in practice. Generally speaking, larger thickness and lower dielectric constant of the gate oxide results in a smaller gate-to-nanotube capacitance, which further leads to a smaller on-state current. Thus, a device of this kind with large gate capacitance is desired. For the double gate structure, another gate is placed on the top of the CNT array, as shown in Fig. 1(b), in addition to the BG-like structure. For the top gate structure, the CNT array is covered with the gate dielectric and then a top gate electrode, as shown in Fig. 1(c). For the surrounding gate structure, the CNT is surrounded by the cylindrical gate dielectric and coaxially gated, as shown in Fig. 1(d). Each gate configuration has its own advantages. However, which one is most suitable for field effect transistor applications is still an open question to answer. Thus, the central objective of this study is, through numerical simulation, to provide the possible optimized geometrical parameters

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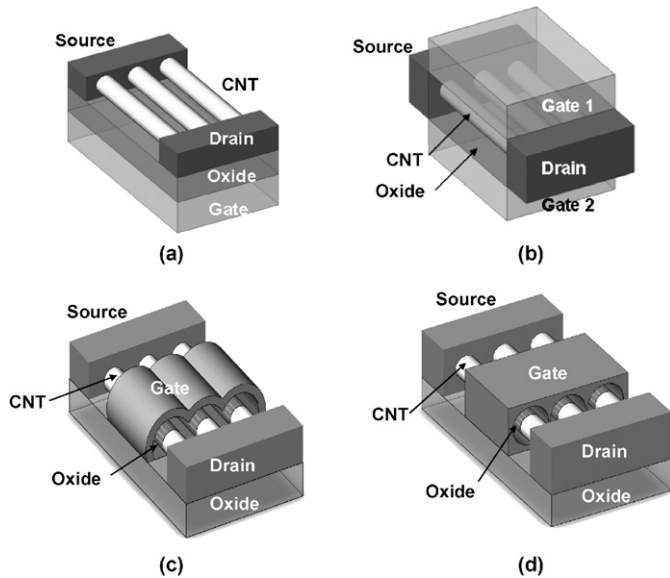


Fig. 1. Sketch of different types of CNTFET: (a) bottom gate (BG), (b) double gate (DG), (c) top gate (TG), and (d) surrounding gate (SG).

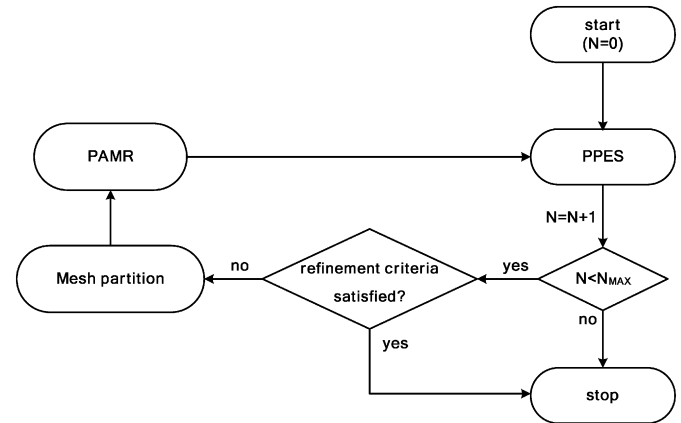
for obtaining the largest gate capacitance among various structures.

Since a single CNT can only provide small amount of driving current, arranging CNTs in arrays is generally required to improve the driving capability of CNTFETs. Thus, electric screening effects can no longer be neglected, provided that the distance between CNTs is small. Four CNTFETs (BG-, DG-, TG-, and SG-CNTFET) with different pitch distance of CNT array and gate lengths were simulated to study the influence of the electric screening effect. In this study we intend to perform parametric studies of CNTFETs based on typical model systems with parameters close to the realistic arrangement.

In this paper, we applied a computer code [11] for the electrostatic predictions of CNTFET with arbitrary and realistic three-dimensional geometries. Details of geometry were fully taken into account without any oversimplification (e.g., a 2D or coaxial symmetric simulation [12]). It has been demonstrated that there are 30% difference between 2D and 3D models in the magnitude of computed gate capacitance [13]. In our numerical simulation, a parallel Poisson's equation solver (PPES) was first used to obtain the potential and electric field distribution of structures. A solution-based parallel adaptive mesh refinement (PAMR) module based on the error-estimator technique was then applied iteratively to refine where higher electric fields exist. Finally, the capacitance was calculated by the modified charge integration method. This code enables us to estimate the electrostatic characteristics of CNTFETs with various nanostructures. A more detailed procedure of the implementation of PPES-PAMR is described in the following section.

2. Numerical method

In previous studies [11,14], we have presented a parallelized 3-D Poisson's equation solver using the Galerkin finite-element method, coupled with a ray-tracing module, to predict field-emission properties of the gated CNT field-emission device. In



PPES : Parallel Poisson's Equation Solver

Fig. 2. Flowchart of the coupled PPES-PAMR method [15].

this study, the simulation procedures for the electrostatic distribution consist of those in [11], except for the procedure of applying the modified charge integration method to obtain the capacitance.

In order to perform the electrostatic analysis, we first need to calculate the electrostatic distribution by solving the Poisson's equation. Without considering the space-charged effect, the Poisson's equation reduces to a Laplacian equation. An unstructured tetrahedral mesh has been used throughout the study for the flexibility of modeling objects with complex geometry. In the current study, eight processors are used for simulation throughout the study and the convergence criterion of the relative residual in parallel Conjugate Gradient is 10^{-7} , unless otherwise specified. A parallelized adaptive mesh refinement (PAMR) module [15] is automatically coupled to increase the accuracy of the predicted electric field near the region where electric fields are large. In brief, PAMR is implemented using an *a posteriori* error estimator proposed by Zienkiewicz and Chu [16]. A prescribed global relative error ε_{pre} of 0.0005 is used to control the level of accuracy throughout the study, unless otherwise specified. The absolute error in each element is then compared with a current mean absolute error at each level, based on ε_{pre} , to decide if refinement is required. In this case, an element is refined into eight child elements if required. Procedures of this coupled PPES-PAMR method are summarized as shown in Fig. 2. Details of the implementation and study of the parallel performance can be found in our previous work [11].

To compute the gate capacitance, a modified charge integration method was used to compute the accumulated charges of a conductor pair [13]. Since the distribution of the electric field at the surface of the nanotube is obtained by PPES-PAMR, charges can be retrieved by an integration approach. Charges are then divided by the potential difference to evaluate the capacitance. It is assumed that the constant potential prevails at each electrode and then the gate-to-tube capacitance can be readily obtained as described in the above. Note that quantum mechanical effects for the device with ultra-thin insulators [17, 18] are not considered in the present simulation models. The classical approach used here may overestimate the capacitance as compared with the results of quantum corrected approaches.

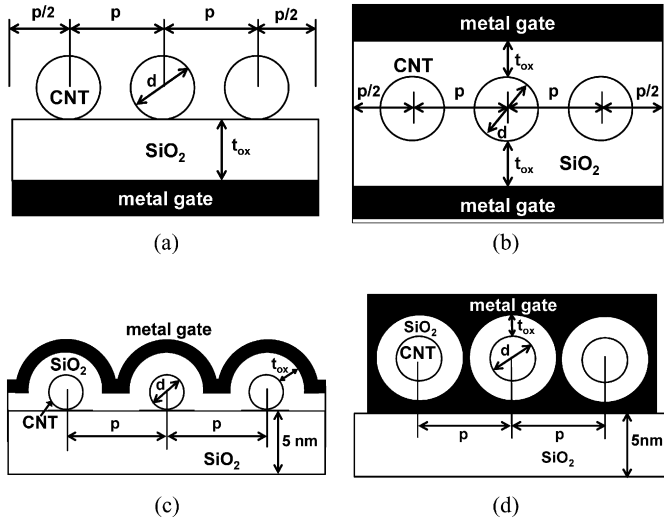


Fig. 3. Transversal cross-section of CNTFETs with different gate configuration: (a) BG, (b) DG, (c) TG, and (d) SG.

It is believed that the consideration of quantum capacitance shall result in more proper quantitative calculation [19], which is currently under investigation in our group. Nevertheless, the major physical trends obtained in this study will remain valid even when the quantum mechanical effects are included. Moreover, the difference between the classical and quantum mechanical simulation is quite small and decreased with the increasing of pitch distance.

3. Results and discussions

In our simulation models, the length of CNT, l , was 25 nm and its diameter, d , was 1.7 nm, which was the typical mean diameter of single wall CNT [20]. To investigate how the screen effect affects device performance, an array of CNT, consisting of the three nanotubes were considered in our modeling for simplicity. CNTs were pitched in a periodic arrangement with uniform pitch distance, p , defined as the central distance between two neighboring CNTs. Gate capacitance is calculated as a function of pitch distance that is varied from 2 to 11 nm. The thickness of silicon dioxide, t_{ox} , as gate dielectric was fixed to 2 nm. The dielectric constant of silicon dioxide, ϵ_{ox} , was 3.9. The CNTFET was embedded inside the background (board) material with dielectric constant $\epsilon_0 = 1$ (vacuum). The extent of the background material was set at least five times larger than the CNTFET. Figs. 3 (a)–(d) show the schematic arrangement of BG-, DG-, TG-, and SG-CNTFET, respectively. Here CNT was treated as classical metal (perfect conductor) and the applied voltage over the whole CNT was 1 volt. The gate electrode was grounded. The gate-to-middle tube (C_{gm}) capacitance was defined as the capacitance between the gate and middle tube, while the gate-to-edge tube capacitance (C_{ge}) was defined as the capacitance between the gate and “edge” tube (tube next to the middle tube). Note that C_{ge} represents the capacitance between gate and either of left or right tube. C_{gm} and C_{ge} of CNTFETs with BG, DG, TG, and SG gate electrode configurations were simulated for comparison.

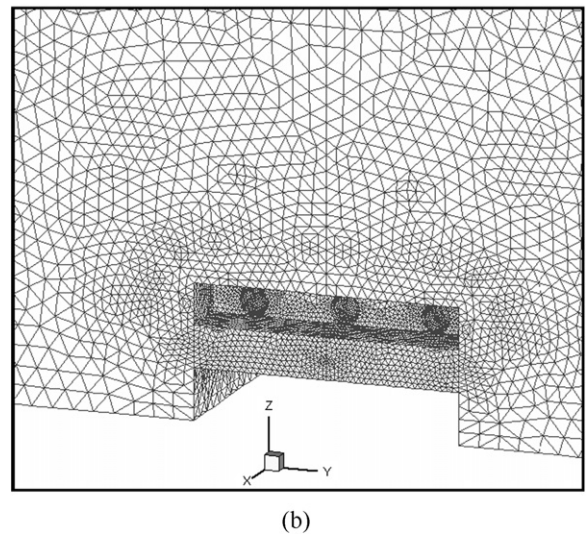
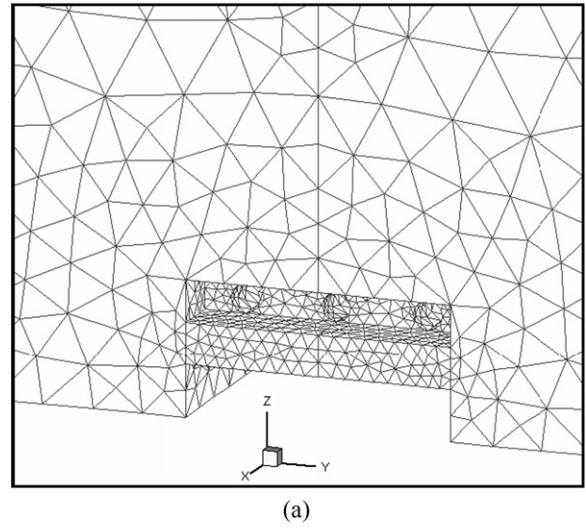


Fig. 4. Surface mesh distributions of the BG-CNTFET at (a) initial (Level-0; 7845 nodes) and (b) after Level-4 PAMR (79842 nodes).

Fig. 4 shows the surface mesh distributions of a typical BG configuration with the gate length of 15 nm and the pitch distance of 6 nm after a series of applying PPES-PAMR procedure. Fig. 4 (a) and (b), respectively, shows the initial and level-4 surface mesh around the tubes, where the number of nodes increases from 7845 to 79,842. Most refined nodes are clustered near the surface of the tubes, which in turn improves the accuracy of the potential distribution in those regions. After 4 levels of mesh refinement, the value of the gate-to-middle tube capacitance and gate-to-edge tube capacitance near the tip approaches approximately a constant value of 0.082 and 0.0835 fp/um, respectively. All the cases shown later apply this mesh refinement module for better solution.

Figs. 5 (a)–(d) show the cross-section plots of potential contour for (a) BG-, (b) DG-, (c) TG-, and (d) SG-CNTFET, respectively. For all results in Fig. 5, the pitch distance was fixed as 6 nm and the gate length was fixed as 15 nm. The electric field was calculated as the negative value of the potential gradient at all nodes. As a result, the dense spread of equipotential lines located over the surface of the nanotubes indicates

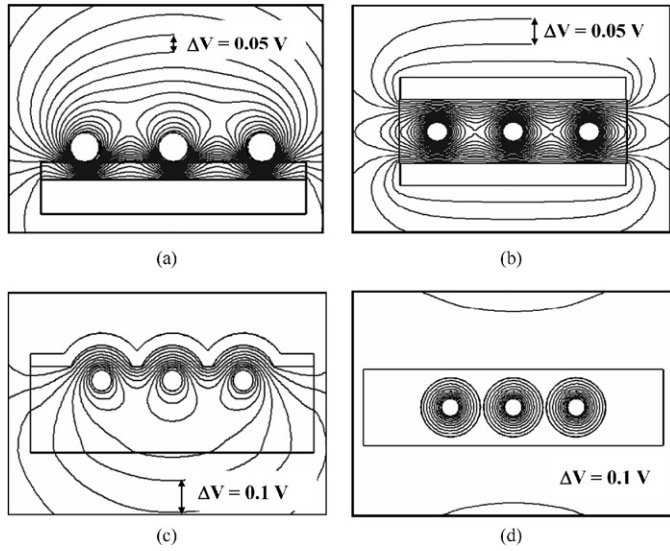


Fig. 5. Transversal potential distributions for CNTFETs with different gate configuration: (a) BG, (b) DG, (c) TG, and (d) SG.

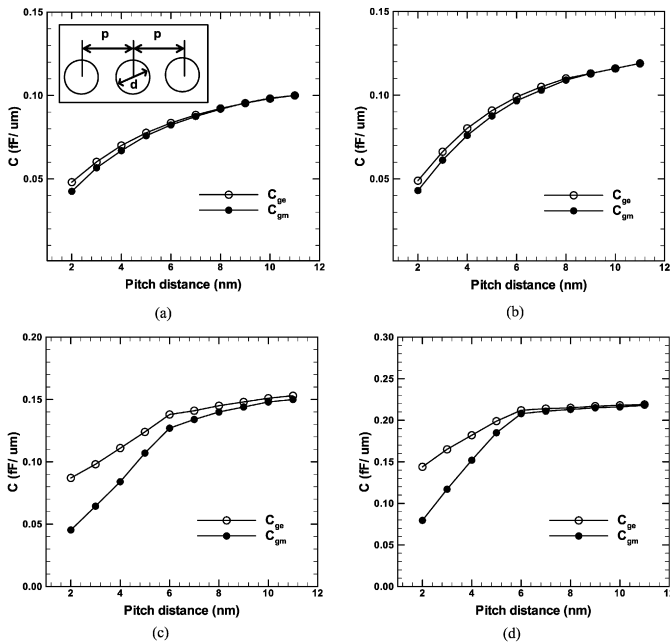


Fig. 6. Dependence of the gate-to-middle tube capacitance (●) and gate-to-edge tube capacitance (○) on the pitched distance for (a) BG-, (b) DG-, (c) TG-, and (d) SG-CNTFET.

the presence of the stronger electric field, which leads to higher accumulated charges enclosed within the surface of nanotube. Induced charges of the middle tube and edge tubes were then computed by applying the charge accumulation method through integration of the local electric field over the surface of nanotube. Then, capacitance can be extracted by means of dividing the charges by the potential difference between gate and tube. The dependence of gate capacitances (C_{gm} and C_{ge}) on pitch distance for different CNTFETs is presented in Fig. 6. Here, the gate length was fixed as 15 nm, in which we are interested in demonstrating the effects of screening effects due to the variation of pitch distance. As shown from the results, SG-CNTFET

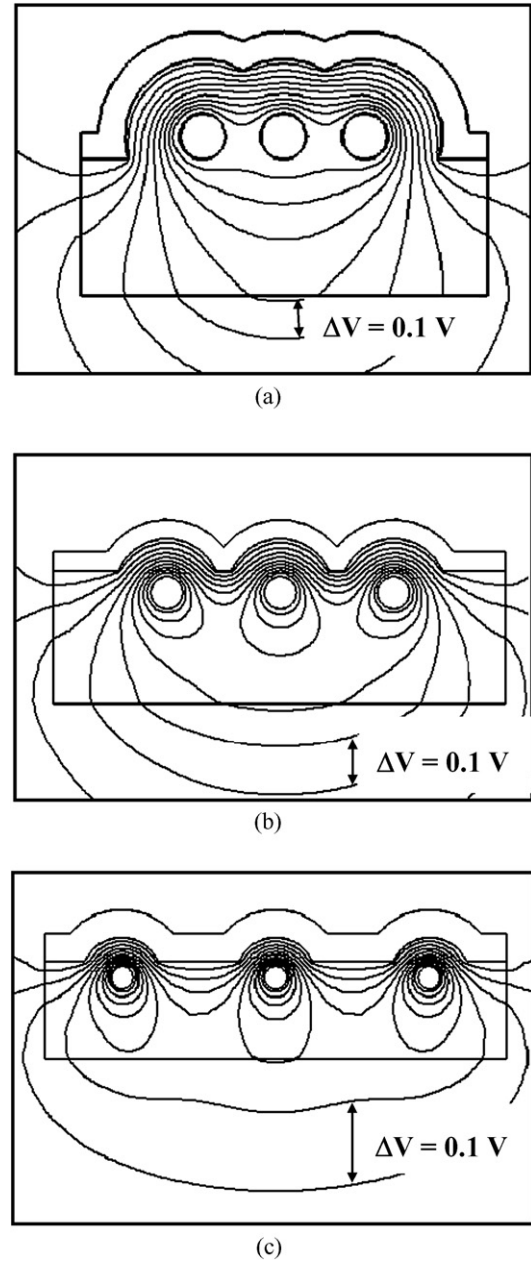


Fig. 7. Transversal potential distributions for TG-CNTFET with three pitched distance: (a) 3 nm, (b) 6 nm, and (c) 9 nm.

is found to possessing the largest capacitance among various structures, while, BG-CNTFET shows the lowest gate capacitance. For the optimized condition, $p = 11$ nm, the magnitude of C_{gm} for BG, TG, and DG is 54%, 45% and 30% smaller than that of SG, respectively. It is clear that the screening effect can seriously affect the magnitude of the capacitance if the tubes were pitched too close. As a result, both C_{gm} and C_{ge} increase as the increasing of pitch distance and finally saturate at a constant value at large pitch distance.

The screening effect becomes most serious in TG configuration. To understand the electric screening effect, we focus our attention on TG structure. The potential distribution of TG-CNTFETs with pitch distance of 3, 6, and 9 nm are shown in Figs. 7 (a)–(c), respectively. We can find that the middle tube is

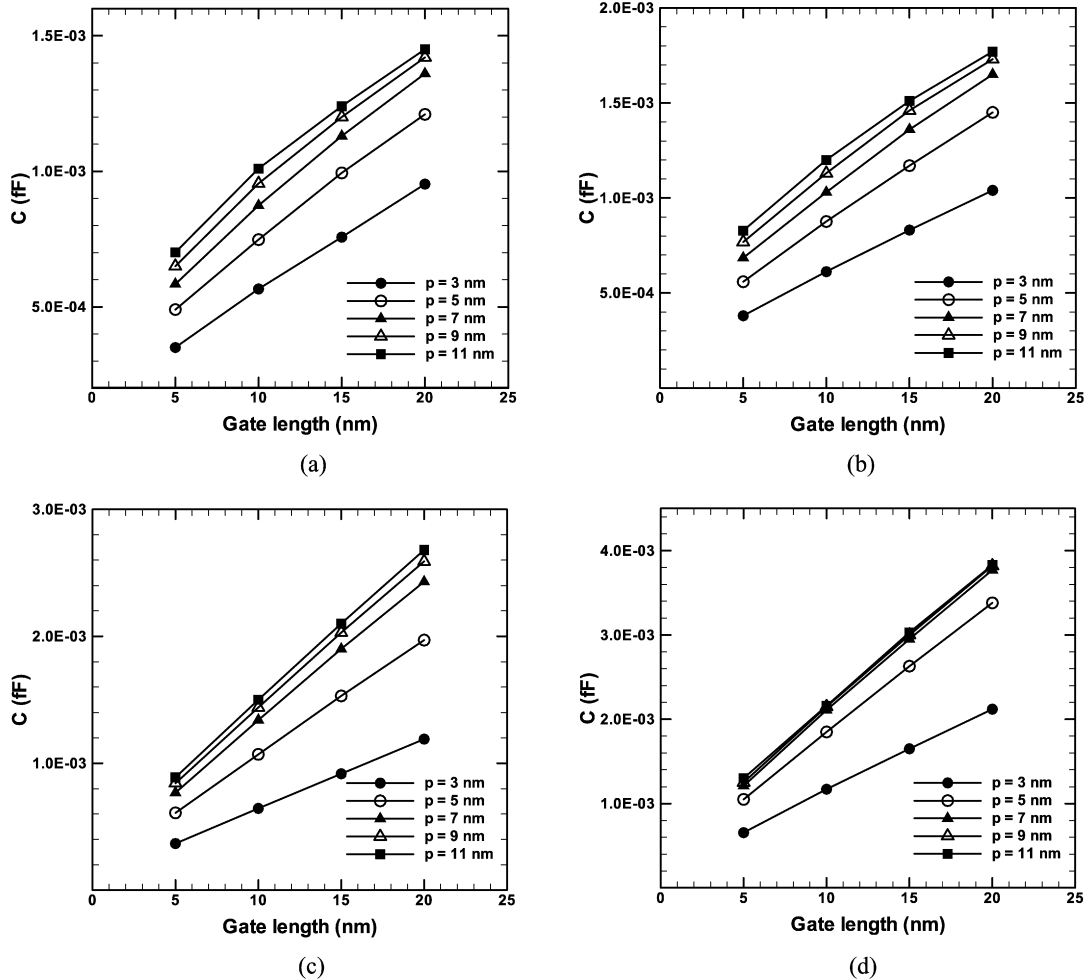


Fig. 8. Dependence of the gate-to-middle tube capacitance on the gate length for (a) BG-, (b) DG-, (c) TG-, and (d) SG-CNTFET.

seriously screened at the shortest pitch distance (Fig. 7(a)) and it shows an improved potential coverage at large pitch distance (Fig. 7(c)). It clearly explains that the value of gate-to-middle tube capacitance is much lower than the gate-to-edge tube capacitance at small pitch distance as shown in Fig. 6. Taking into account the form of the potential distribution as well as the strong influence of electric field on induced charges, it is not difficult to figure out the difference of the C_{gm} and C_{ge} is mainly due to the stronger electric screening for the middle tube. As the pitch distance becomes larger (e.g., p is larger than 8 nm), the electric screening becomes weak; thus, the difference between C_{gm} and C_{ge} is tiny and the total capacitance is larger. This is particularly apparent for configurations with stronger gate control such as TG and SG. It seems that the electric screening between tubes is insignificant provided that the pitch distance of the CNTFET is a few times larger than the diameter of CNT. To sum up our simulation results, the pitch distance of larger than 8 nm is recommended for BG and DG structures for eliminating the screening effects. In contrast, the pitch distance of larger than 10 nm and 6 nm is recommended for TG and SG structures, respectively.

Effects of gate length to the C_{gm} and C_{ge} with different pitch distances are presented in Figs. 8 and 9, respectively. Different

gate lengths with the pitch distance of 3, 5, 7, 9 and 11 nm were simulated. Results indicate that both C_{gm} and C_{ge} linearly increase with increasing of the gate length at a fixed pitch distance. In addition, the slopes of C_{gm} and C_{ge} increase with increasing pitch distance. At the larger pitch distance, the gate capacitance and the slope eventually converge, as observed in Figs. 8 and 9.

4. Conclusions

So far, we have developed a 3D adaptive finite element simulation code, which is capable of computing the electrostatic characteristics and the gate capacitance of CNTFETs with different configurations. Electrostatic properties and gate capacitances of BG-, DG-, TG-, and SG-CNTFET have been investigated. Different pitch distance and gate length has been taken into account to understand the influence of the screening effect on device performance. Finally, optimized geometric parameters are suggested. Pitch distance of 8 nm for BG and DG, 10 nm for TG and 6 nm for SG CNTFET are recommended to eliminate the electric screening effect. Although screening effect becomes most serious for TG design, under the well controlled pitch distance, it is recommended that the top gate design is the most appropriate structure for CNTFET applica-

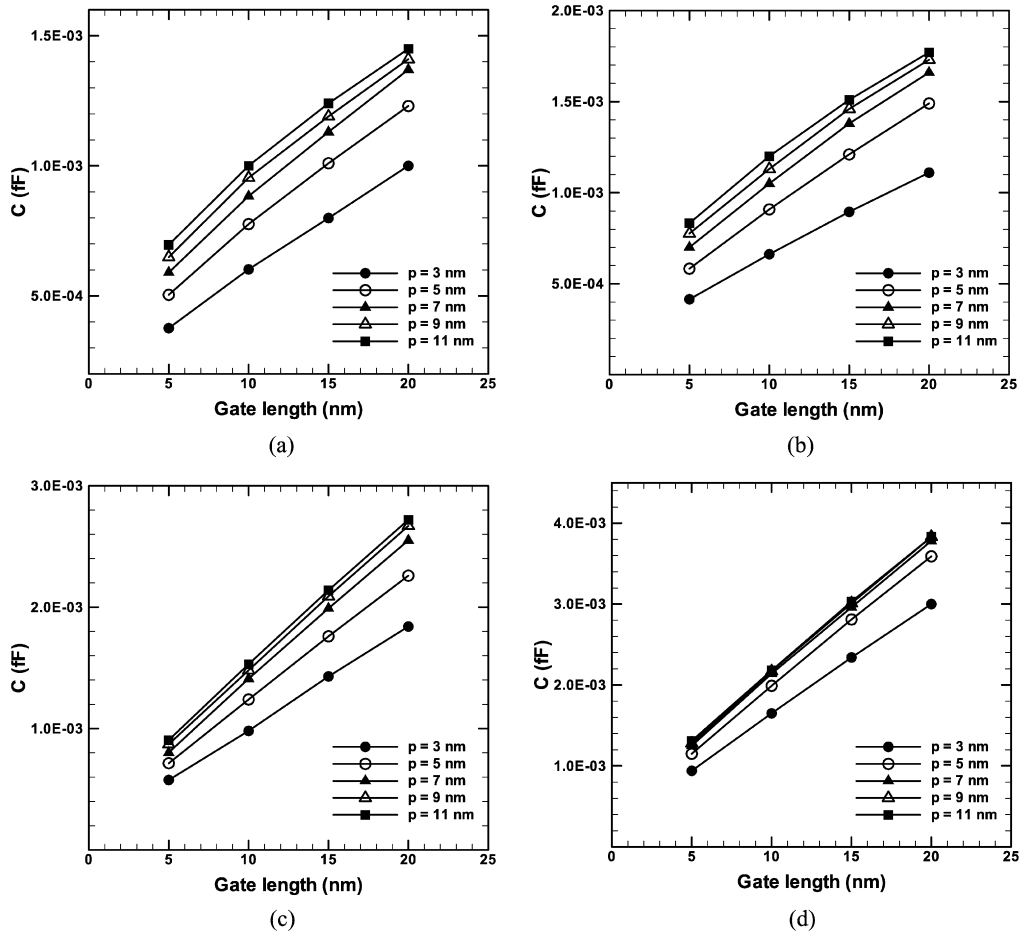


Fig. 9. Dependence of the gate-to-edge tube capacitance on the gate length for (a) BG-, (b) DG-, (c) TG-, and (d) SG-CNTFET.

tions, which may provide a compromise between device performance and manufacturability. This modeling can also help us investigate and compare the performance among many metal-oxide-semiconductor FETs (MOSFETs) in the nanoelectronic engineering design.

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