行政院國家科學委員會補助專題研究計畫成果報告

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※ **電漿製程對 N-型及 P-型金氧半場效電晶體** ※

※ **之損傷機制研究** ※

※ Mechanism of Plasma Process Induced Damage ※

※ On N-type and P-type MOSFET ※

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計畫類別：■個別型計畫　□整合型計畫

計畫編號：NSC 89－2215－E－009－074－

執行期間： 88 **年** 11 **月** 01 **日至** 89 **年** 07 **月** 31 **日**

計畫主持人：崔秉鉞

共同主持人：無

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行政院國家科學委員會專題研究計畫成果報告

電漿製程對 N-型及 P-型金氧半場效電晶體之損傷機制研究

Mechanism of Plasma Process Induced Damage on N-type and P-type MOSFET

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執行期限：88 年 11 月 01 日至 89 年 07 月 31 日

主持人：崔秉鉞　交通大學電子工程學系

共同主持人：無

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一、中文摘要

本計畫著重在接觸窗 之介電層蝕刻之電漿製程損傷機制研究・P-型電晶體所受損傷比 N-型電晶體嚴重，且損傷程度與接觸窗之總面積成正比・大部份損傷經後段製程後轉為隱性缺陷，對元件基本性質影響不大，但在熱載子可靠度測試時會產生影響・介電層蝕刻的安全天線比例低於導體蝕刻，此為未來嵌入式製程所必需慎重面對的課題・

關鍵詞：電漿製程損傷、天線比例、介電層蝕刻

Abstract

Plasma process induced damage from high-density plasma dielectric etcher was studied. It was observed that PMOS devices were damaged more readily than NMOS devices. Some permanent damages become hidden defects after backend of line processes. These latent damages in the form of gate oxide traps result in poor oxide integrity during Fowler-Nordheim stress or hot carrier stress. The damage shows good correlation with the total exposed contact area. The safe antenna ratio is much lower than that at conductor etch. Thus, plasma damage during dielectric etch in high-density plasma system must be considered carefully.

Keywords: plasma process induced damage, antenna ratio, dielectric etch

二、緣由與目的

電漿製程已廣泛應用於積體電路(IC)製造上・由於電漿系統中充滿加速的帶電粒子，會對製造中的元件造成許多種損傷[1]・ 這之中最中要的是電荷堆積(charge build-up)・由於電荷堆積會被曝露在電漿中的導體面積放大，又稱為天線效應(antenna effect) [2-26]・在過去十餘年中，大部份的研究均著重在導體的電漿蝕刻製程上 [2-17]，也就是複晶矽層及金屬層・

近年來，因為接觸窗(contact hole)及通孔(via hole)的深寬比逐漸增加 [27]，介電層蝕刻在深次微米製程所扮演的角色也愈來愈受重視・但是針對介電層蝕刻的電漿損商所進行的研究卻不多[28-32]，對損傷機制的了解更是有限・本專題計畫即針對以高密度電漿系統執行介電層蝕刻所造成的天線效應進行研究・包括完整的測試結構設計、多項元件參數的測量、可靠度的評估等等・希望對介電層蝕刻造成的損傷機制有更多的認識，了解對元件的影響，並評估其嚴重程度・

三、結果與討論

I. 實驗設計

本計畫採用 0.25 微米 CMOS 製程, 閘氧化層厚度為 5nm，通道長度及寬度分別為 0.24um 及 5.0um・NMOS 的閘極為 N 型複晶矽，PMOS 閘極為 P 型複晶矽・複晶矽對閘氧化層的天線比例是 2000・接觸窗的數量分別是 125、625、1275 及 2875，相對應的天線比例是 7、37、75 及 170・接觸

窗直徑及間距都是 0.3um，有些元件用不同的接觸窗大小及間距，以了解對損傷的影響．接觸窗蝕刻是在電感耦合式的高密度電漿系統中進行．所有元件的閘極都從第一層金屬開始並聯到保護二極體以避免金屬蝕刻及後續製程的影響．圖一是測試結構的示意圖．

II. 實驗結果

我們首先測量複晶矽天線比為 10,000 而接觸窗只有一個的元件，所有參數均顯示元件沒有受到損傷，因此 2,000 的天線比例是安全的設計．如果不同的接觸窗設計有元件受損的跡象，必然是因為接觸窗製程所造成．

接下來測量不同接觸窗數量的 NMOS 及 PMOS 元件的基本直流參數包括低電場閘極電流(Ig)、臨界電壓(Vt)、互導(gm)及次臨界斜率(S)．NMOS 的所有參數都看不出與接觸窗數量的關係，只有 PMOS 的 Ig 顯示出接觸窗數量愈多則高漏電流的元件愈多，如圖二所示．這顯示 Ig 是最敏感的直流參數．PMOS 比 NMOS 易受到製程損傷可能與損傷發生時的電壓極性有關．

其次，我們選擇另一組元件施加電應力(FN stress)使流過閘氧化層的電量達到 10 mC/cm^2 以偵測是否有電中性的損傷存在． PMOS 的 I_g 及 V_{th} 都顯示出接觸窗數量愈多分佈愈廣，如圖三(左)及(右)所示．這表示有些損傷在後段製程轉變為電中性的隱性缺陷 (hidden defect)．又因為施加應力後 V_{th} 的改變受接觸窗數量影響，但 g_m and S 的變化則無，隱性缺陷應是以氧化層中的陷阱(oxide trap)型態存在．

NMOS 經 FN stress 後，只有接觸窗最多的元件的 Ig 從 2 pA 增加到 10 pA，其它元件及參數都未顯示出製程損傷的跡象．這也佐證 NMOS 比 PMOS 不易受到製程損商．

我們也嘗試用熱載子應力測試 (hot carrier stress) 來評估製程損傷．PMOS 用最大閘電流條件，NMOS 用最大基板電流條件．PMOS 的 Vth 劣化率隨接觸窗數量增加而增加，如圖四(左)，g_m 和 S 的劣化則和接觸窗數量無關．這是因為 PMOS 的劣化機制是電子被捕捉在氧化層中 [30-32]，既然隱性缺陷是氧化層中的陷阱，注入的熱電子可以被隱性缺陷所捕捉，不需要自行產生陷阱，分佈較無隱性缺陷的元件廣，所以 Vth 的劣化率隨接觸窗數量增加而增加，g_m 和 S 的劣化則和接觸窗數量無關．

NMOS 也顯示出 Vth 的劣化率隨接觸窗數量增加而增加的現象，如圖四(右)，這再一次支持隱性缺陷是氧化層中的陷阱的推論．也同時表示 hot carrier stress 比 FN stress 容易看出隱性缺陷的存在與否．

不同接觸窗大小 (0.3 um, 0.25 um, 0.2 um) 或間距 (0.3 um, 0.6 um, 1.2 um)的元件的直流特性都幾乎一樣 (接觸窗數目為 625)．為提高對製程損傷的鑑別能力，進一步對這些 PMOS 施加 hot carrier stress．

圖五(左)是不同接觸窗大小的 PMOS 經 hot carrier stress 後的 Vth 劣化情形．似乎接觸窗愈小劣化就愈輕，但幅度差別不大．這可能是因為數量不變的情況下，接觸窗愈小，天線比例愈低，所以損傷較輕．這樣的結果顯示接觸窗蝕刻在 0.2um 時，仍不會有電子遮避效應．圖五(右)是不同接觸窗間距的 PMOS 經 hot carrier stress 後的 Vth 劣化情形．間距愈大則劣化愈嚴重，這可能可以用局部電場分佈來解釋 [15]，但詳細的原因在本計畫中尚未能確認．值得慶幸的是在真實的電路中，多個接觸窗通常會用最小間距，所以問題應不嚴重．

三、計畫成果自評

本計畫對介電層蝕刻製程的電漿製程損傷進行了深入的探討．N-型電晶體及 P-型電晶體的基本電性參數及可靠度均已列入評估項目，符合計畫原設定希望綜合比較各種參數的變化以偵測損傷的發生的構想．

本計畫共達成下列結論：

1. 確認低電場閘級電流在介電層蝕刻製程下仍是最能反應奠漿損傷的直流參數．
2. 經過後段製程，多數損傷轉為隱性缺陷，缺陷以氧化層中之陷阱型態存在．此類隱性缺陷必須以電應力測試才能偵測到．

3. **在熱載子測試時，因為** PMOS **的熱載子損傷機制與電漿製程的隱性缺陷同為氧化層中的陷阱，故顯示與天線比例相吻合的趨勢・**
4. **損傷程度與接觸窗總面積成正比關係，與接觸窗大小無關・可知在實驗範圍內並無電子遮蔽效應發生・**
5. **介電層蝕刻的安全天線比例低於** 100**，遠低於導體蝕刻的安全天線比例 (約** 10K) **・**

上述結果提供對介電層蝕刻步驟的電漿製程損傷機制深入的了解，也顯示出介電層蝕刻可能造成比導體蝕刻更嚴重的製程傷害・對發展中的嵌入式製程提供預警・

本計畫之部份研究成果已整理為學術論文，並通過 Microelectronics Reliability **期刊之審查，正排版待刊中・原稿請見附件・**

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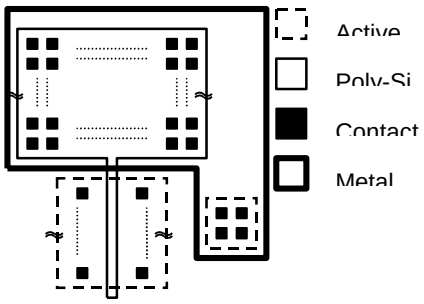
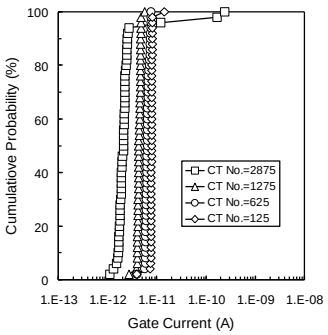
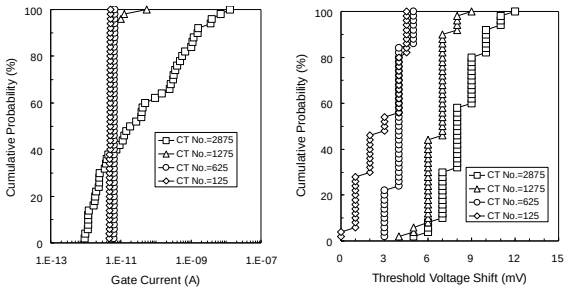


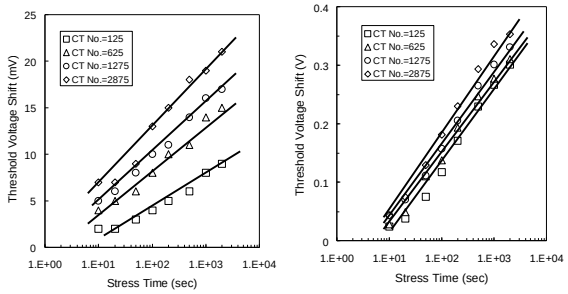


圖一．本計畫使用之測試結構示意圖．

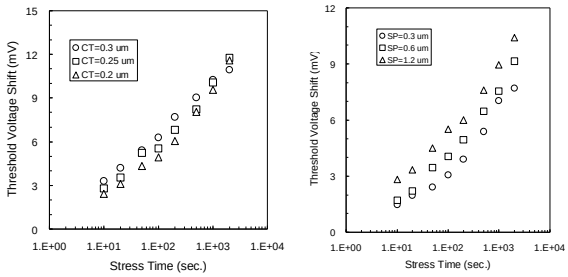
圖二．不同接觸窗數目的 NMOS 元件低電場閘極電流累積分佈．



圖三. PMOS **經** FN stress **後的(左)閘極電流及(右)臨界電壓漂移累積分佈**．FN stress **條件是**-1mA/cm^2，10 second.



圖四. (**左**)NMOS **及(右)**PMOS **經熱載子應力測試後的臨界電壓漂移累積分佈**•PMOS **應力測試條件是** V_{ds}=-5V **及** V_{gs}=-0.8V • NMOS **應力測試條件是** V_{ds}=4.5V **及** V_{gs}=1.6V.



圖五. (**左**)**不同接觸窗大小及(右)不同接觸窗間距的** PMOS **經熱載子應力測試後的臨界電壓漂移累積分佈．應力測試條件是** V_{ds}=-5V **及** V_{gs}=-0.8V •

附　件

Plasma Charging Damage during Contact Hole Etch In High-Density Plasma Etcher

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Abstract

Plasma process induced damage from high-density plasma dielectric etcher was studied comprehensively. It was observed that PMOS devices were damaged more readily than NMOS devices. Low field gate current is the most sensitive parameter to reflect the permanent damages. Some permanent damages become hidden defects after backend of line processes. These latent damages in the form of gate oxide traps result in poor oxide integrity during Fowler-Nordheim stress or hot carrier stress. The damage shows good correlation with the total exposed contact area. The safe antenna ratio is much lower than that at conductor etch. although no electron shading effect was observed. Thus, plasma damage during contact or via hole etch in high-density plasma system must be considered carefully.

Keywords : plasma process induced damage; dielectric etch; high-density plasma; latent damage

I. Introduction

Plasma process had been widely used in integrated circuit (IC) manufacturing. Since plasma system has charged and accelerated particles, several kind of damage may be induced during plasma process. The damages can be divided into four categories : (a) physical damage due to ion bombardment; (b) metal contamination from chamber and gas piping; (c) radiation damage due to glow discharge and ion bombardment; (d) charging damage due to unbalanced charge in plasma [1]. Among these damages, charging damage attracts much more attention in the past ten years because the damage may be magnified by the total exposed conducting area. It is the so-called antenna effect [2-26].

In the past, much work has been devoted to antenna effect during conducting layer etch, e.g. poly-Si layer and metal layer [2-17]. Basic mechanisms, damage modes, impacts on device and circuit, test structures, and measurement techniques have been discussed widely. From these fundamental understandings, low damage process, protection strategy, and new plasma reactor were proposed [18-26]. It is also well accepted that PPID (Plasma Process Induced Damage) can be withstood after optimizing process and circuit design.

Dielectric etch becomes more and more important in deep sub-micron era, because the aspect ratio of contact and via hole become larger and larger for DRAM process [27]. On the other hand, dual damascene process becomes main stream for metal patterning as Cu interconnect is used instead of Al interconnect [28]. Conventional metal etch is replaced by dielectric etch in damascene process. Therefore, dielectric etch is more and more important in IC manufacture, especially at backend of line (BEOL) processes. Unfortunately, less work has been done in the field of PPID of dielectric etch [29-33]. In ref.[29], the authors reported that only gate current was degraded by PPID. But only fresh device characteristics were measured and only area antenna effect was discussed. In ref.[30-32], the authors discussed the contact etch damage on various thickness oxides. But the contact size is as large as 4 μm^2. In ref.[33], the authors studied the PPID of damascene process, but the etcher used is not a high-density

plasma system.

In this paper, we reported a comprehensive assessment of the PPID during dielectric etch in a high-density plasma (HDP) etcher. A set of test structures with various contact number, contact size, and contact space was designed. Various device parameters were measured before and after stress to separate latent damages from permanent defects. Hot carrier resistance was also evaluated. It is observed that under the same area antenna ratio, dielectric etch induces more severe damage to gate oxide than conductor etch does. Thus, PPID during dielectric etch must be considered carefully.

II. Experiments

Both NMOS and PMOS devices were fabricated by a standard 0.25 μm single-poly-triple-metal CMOS technology using shallow trench isolation structure. Gate oxide was thermally grown to 5 nm thick. N^+ and P+ doped-Si was used as gate electrode for NMOS and PMOS devices, respectively. All devices used to monitor damage are identical and channel length and channel width is 0.24 μm and 5 μm, respectively. In order to place more contacts to poly-Si gate, and to exclude the effect of different antenna ratio during poly-Si etch, the antenna ratio of poly-Si pad area to gate oxide area was set to 2K for all devices. Devices with contact number of 125, 625, 1275, and 2875 corresponding to area antenna ratio (AAR) of 7, 37, 75, and 170, respectively, were designed. The typical contact size is 0.3 x 0.3μm^2 and the contact space is 0.3 μm. For some test structures the contact size and contact space are changed to study the effect of contact size and contact density, respectively. Contact etch was performed in a high density plasma system with inductively coupled plasma (ICP) source. The plasma density at wafer surface is about 10^{11} ions/cm^2. All devices were protected by p-n diode and connected by the first layer metal to avoid damages from other plasma processes. Fig.1 shows the schematic diagram of the test structure used in this work.

Low field leakage current of gate oxide (Ig) at 2.5V, linear region threshold voltage (V_{th}),

transconductance (g_m), sub-threshold swing (S) were all measured before and after Fowler-Nordheim (F-N) stress to separate the latent damages from permanent defects. The specification of I_g is 10 pA which is typical limitation of the noise and leakage current of the automatic measurement system. The F-N stress was performed in inversion polarity at the current density of 1 mA/cm^2 for 10 sec. Channel hot carrier stress was performed on NMOSFET devices at maximum substrate current and PMOSFET devices at maximum gate current to evaluate the impact of damages on device integrity.

III. Results and Discussion

Since the poly-Si area must be large enough to contain more contact holes, the damage level at poly-Si etch step must be examined at first. Four device parameters, Ig, V_{th}, g_m, and S, were all measured on NMOS and PMOS devices with various AAR at poly-Si layer. The contact number is one and the metal pad is connected to a protection diode. It is observed that even if the AAR of poly-Si is as high as 10K, no degradation of any parameters were observed. These results imply that the poly-Si AAR of 2K used for contact hole etch experiments will not introduce damage during poly-Si etch. Furthermore, the protection diode at metal-1 level is effective to avoid damage at metal etch step. All damages observed for higher contact hole AAR must be attributed to the contact hole etch step.

1. Damage Observation

Fig.2(a), (b), and (c) show the cumulative probability plots of I_g, V_{th}, and g_m of NMOS devices with various contact number before F-N stress, respectively. Although slight difference of mean value of I_g is observed, all of them are within specification. The slight difference of I_g may be arisen from the different surface leakage current since various structures are placed at various position of the test chip. Neither yield nor deviation degrades

with the increase of contact number for all parameters. Fig.3(a), (b), and (c) show the cumulative probability plots of I_g, V_{th}, and g_m of PMOS devices with various contact number before F-N stress, respectively. PMOS devices with large contact number show wider spread of I_g. Although the distribution of V_{th} and g_m of PMOS devices do not show any contact number dependence, the obvious correlation between I_g distribution and contact number reflects that PPID occurred and resulted in permanent damage to PMOS devices during contact etch. Sub-threshold swing was also measured, but no contact number dependence was observed for both NMOS and PMOS devices.

From the direct measurement results, two important phenomena were observed. At first, I_g is the most sensitive parameter to reveal damage among the measured DC parameters of devices. This can be easily understood. Oxide charges induced by PPID can be neutralized after BEOL processes. However, most of the trap sites can not be removed at the relatively low process temperature (around 400 ^oC). Low field I_g is related to oxide trap sites while the other device parameters are related to the trapped charges. Therefore, I_g can reflect PPID more sensitive. The current-voltage characteristics of high Ig devices show stress induced leakage current (SILC). This confirms the existence of oxide trap sites. This result is similar to that reported in ref.[30-32, 34]. Second, PMOS device is damaged easier than NMOS device. This may be due to the polarity of charging during plasma process or due to the difference of poly-Si doping type and is still under investigation.

2. Latent Damages

To determine if any defects were passivated during BEOL processes, another device populations were F-N stressed to 10 mC/cm^2, and I_g, V_{th}, g_m, and S were measured. Fig.4(a) is the cumulative probability plot of I_g of PMOS devices with various contact numbers after stress. It shows that devices with more contact holes have much wider I_g distribution after stress than those with less contact holes. The V_{th} shift after stress, defined as V_{th} (after

stress) $-V_{th}$ (before stress), is larger for devices with more contact holes as shown in Fig.4(b). However, no apparent g_m and S shift difference was observed on PMOS devices with different antenna ratio after stress (not shown). These phenomena indicate that most of the plasma process induced defects were passivated during BEOL processes. Since these defects only results in V_{th} shift but not g_m and S shift after stress, these passivated defects were located in gate oxide but not at oxide/silicon interface.

NMOS devices were also F-N stressed to reveal latent damages. However, except the mean value of NMOS devices with 2875 contact holes (AAR=170) increased from 2 pA to 10 pA, the other parameters did not show contact number dependence. The latent damages in NMOS devices are much less than that in PMOS devices. This confirms that NMOS device shows less PPID than PMOS device in this experiment.

It should be noted that the F-N stress used is not strong. The only purpose is to re-generate hidden damages. So, if device was not damaged by PPID, I_g will not increase after F-N stress. The results indicate that the device with largest AAR is damaged seriously during contact etch. Since the sensitivity of F-N test is lower than hot carrier test, hot carrier stress was performed in the next step. It was shown that hot carrier stress can resolve latent damages even if the contact number is only several hundreds.

3. Impact on Hot Carrier Resistance

Fig.5(a) shows the V_{th} shift of PMOS devices with various contact numbers after hot carrier stress at V_{ds}=-5V and V_{gs}=-0.8V. Higher contact number structure shows higher V_{th} degradation rate. The other parameters such as g_m and S do not show contact number dependence. There are two possible explanations. First, no significant interface states were generated during hot carrier stress. It is reasonable because it is well accepted that the major degradation mechanism of PMOS devices under hot carrier stress is oxide trap but not interface state [35-37]. Second, the injected electrons were trapped at those trap sites

generated during plasma process in major. Since the plasma process induced defects are uniformly distributed in channel region, the trapped electrons distributed broader. The V_{th} shift of NMOS devices stressed at V_{ds}=4.5V and V_{gs}=1.6V also show contact number dependence similar to that of PMOS devices as shown in Fig.5(b). These results confirm that defects located in gate oxide were passivated during BEOL processes and can be re-generated during electrical stress. Although the amount V_{th} degradation of NMOS devices is higher than that of PMOS devices, the difference between various contact number of NMOS devices is less apparent than that of PMOS devices. This is consistent with the conclusion in previous sections that NMOS device show less PPID than PMOS device. Furthermore, the major degradation mechanism of NMOS and PMOS devices under hot carrier stress is interface traps and oxide traps, respectively. The observed phenomenon also supports the argument that the latent damages are in the form of oxide traps.

4. *Effect of Contact Hole Size and Contact Hole Density*

At first, cumulative probability of I_g of NMOS and PMOS devices with various contact hole size of 0.2, 0.25 and 0.3 μm (aspect ratio of 3.75, 3.0, and 2.5) and various contact hole of 0.3, 0.6, and 1.2 μm) are measured. Since the contact number is 600 and 625 for devices with various contact hole size and various contact hole space, respectively. No difference of Ig distribution was observed. This is not surprising according to the results shown in section 3.1. To improve the resolution, hot carrier stress was performed on PMOS devices. The stress condition is the same as that used in previous section.

Fig.6(a) shows the V_{th} shift of PMOS devices with various contact hole size after hot carrier stress. It seems smaller contact hole results in smaller V_{th} shift. This may be due to the reduction of antenna ratio by a factor of 2.25 as contact hole size is reduced from 0.3 μm to 0.2 μm. No electron shading enhanced effect was observed.

Fig.7 shows the V_{th} shift of PMOS devices with various contact hole space after hot

carrier stress. It is surprising that the larger the contact hole space, the larger the V_{th} shift. This may be due to the local field disturbing effect [38]. To deeply understand the mechanism required additional works on the local field distribution which is beyond the scope of this paper. Fortunately, the contact hole space will be pushed to technology limitation to improve the circuit density. This wide space layout does not occur at real circuit.

IV. Conclusion

In this work, the PPID during contact hole etch in a HDP system was investigated comprehensively. Among the devices DC parameters, I_g is the most sensitive parameter to reveal the permanent defects. Some permanent defects were hidden during the BEOL process. These latent damages in the form of oxide trap exist in gate oxide. They can be re-generated after F-N stress or hot carrier stress. NMOS devices show less PPID than NMOS devices in this work.

The PPID shows good correlation with the number of contact, i.e. the total area of contact holes. The hot carrier degradation decreases with the decrease of contact hole size due to the reduction of antenna ratio. The PPID is enhanced by the wide contact hole space. Fortunately, it will not be issues in real circuit. It is also observed that the safe antenna ratio of contact hole etch is much less than that of conductor. Therefore, PPID during contact hole or via hole etch must be considered carefully.

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Figure Captions

Fig.1. Schematic diagram of the test structure used to study the plasma process induced damage during contact hole etch. The area antenna ratio at poly-Si layer is 1000. Structures with various contact number, contact size, and contact density are all designed and measured.

Fig.2. Cumulative probability plots of (a) gate current I_g, (b) threshold voltage V_{th}, and (c) transconductance g_m of NMOS devices with various contact number before F-N stress.

Fig.3. Cumulative probability plots of (a) gate current I_g, (b) threshold voltage V_{th}, and (c) transconductance g_m of PMOS devices with various contact number before F-N stress.

Fig.4. Cumulative probability plots of (a) gate current and (b) threshold voltage shift of PMOS devices with various contact number after F-N stress at inversion polarity at 1 mA/cm^2 for 10 second.

Fig.5. Threshold voltage shift of (a) PMOS devices and (b) NMOS devices with various contact numbers after hot carrier stress. The PMOS devices is stressed at V_{ds}=-5 V and V_{gs}=-0.8 V. The NMOS devices is stressed at V_{ds}=4.5 V and V_{gs}=1.6 V.

Fig.6. Threshold voltage shift of PMOS devices with various contact hole size of 0.2, 0.25 and 0.3 μm. The contact space is 0.3 μm and the number is 600.

Fig.7. Threshold voltage shift of PMOS devices with various contact hole space of 0.3, 0.6, and 1.2 μm. The contact size is 0.3 μm and the contact number is 625.

Fig.1

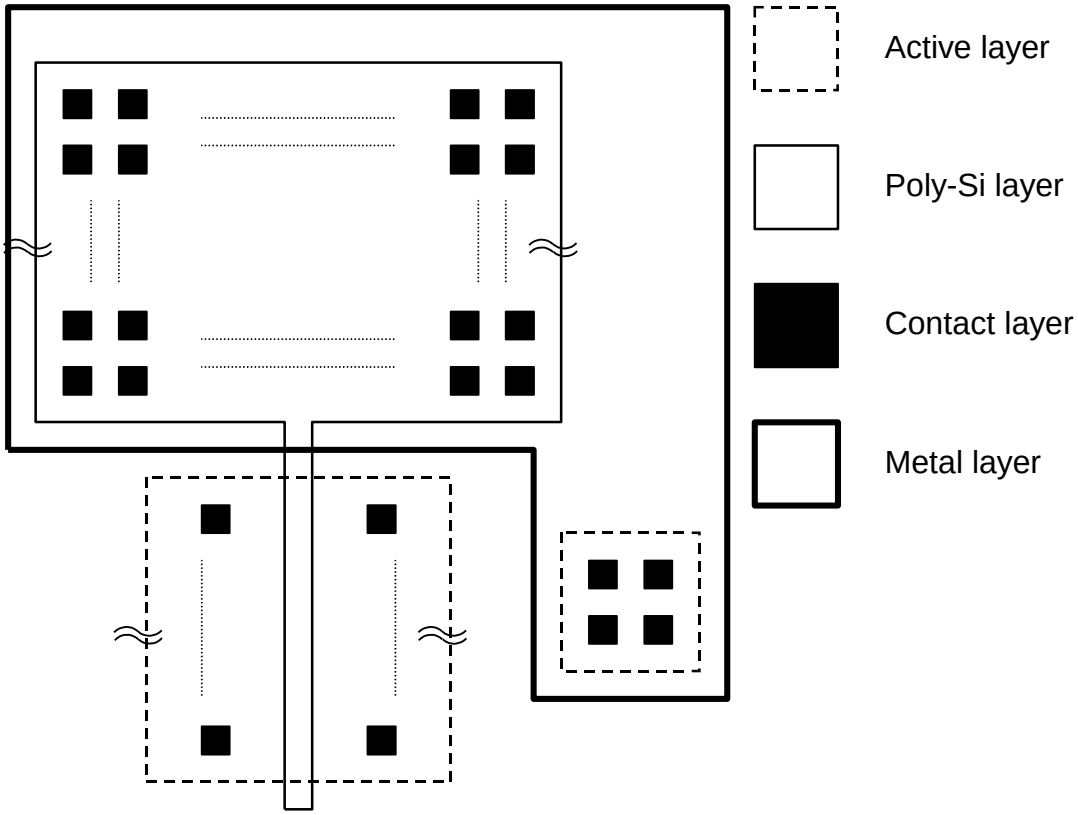
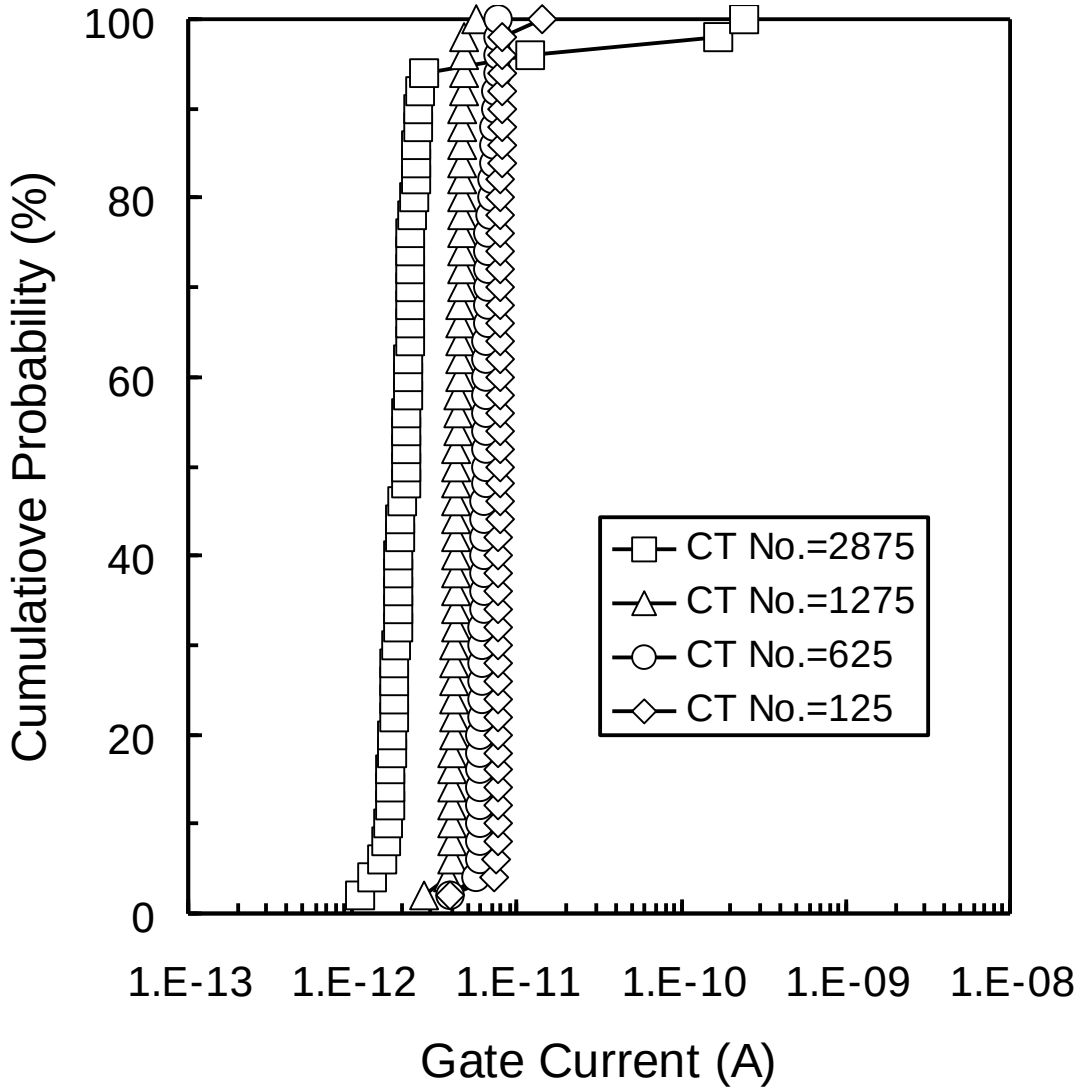


Fig.2(a)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80
60
40
20
0
Cumulatiove Probability (%)
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1.E-12
1.E-11
1.E-10
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1.E-08
Gate Current (A)
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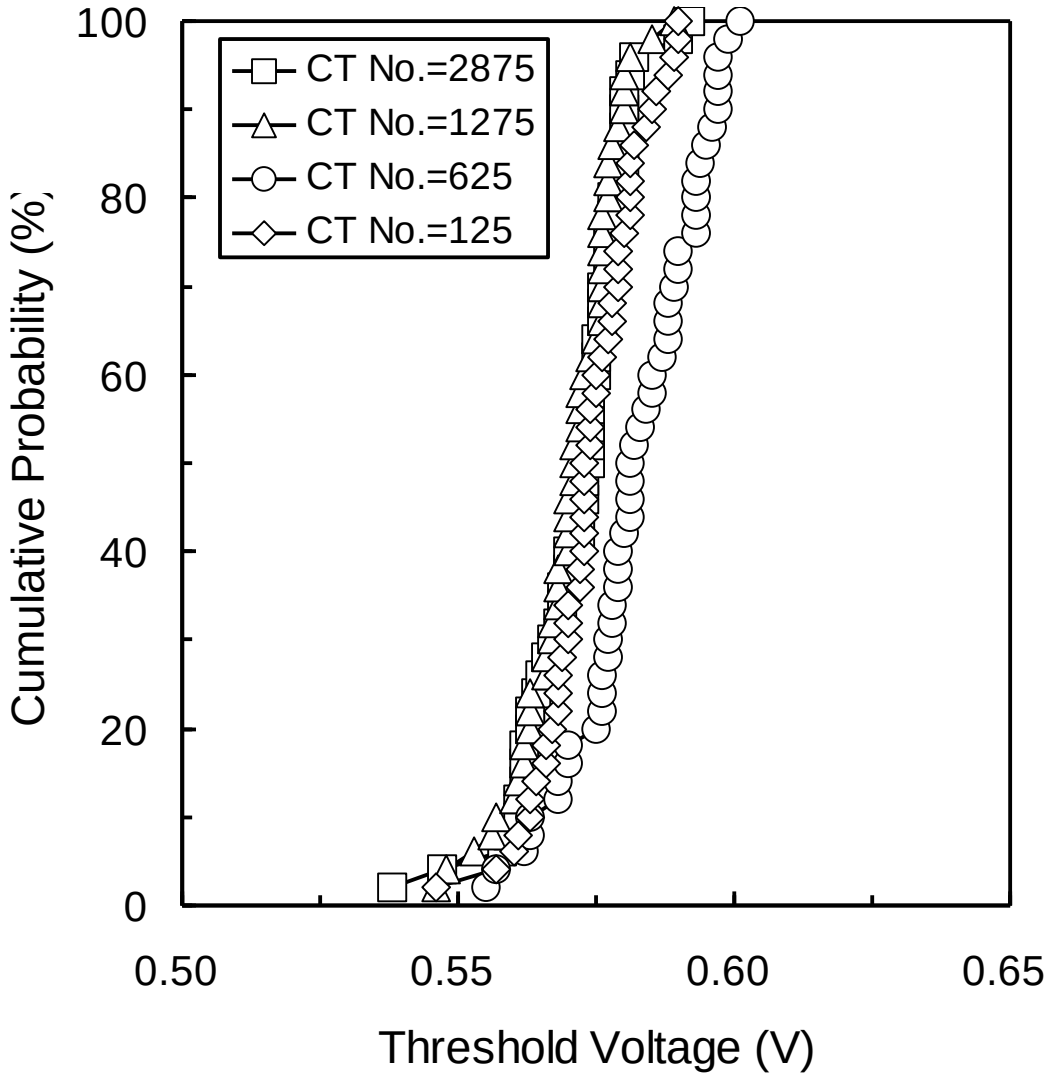
CT No.=1275
CT No.=625
CT No.=125

Fig.2(b)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CT No.=1275
CT No.=625
CT No.=125
Cumulative Probability (%)
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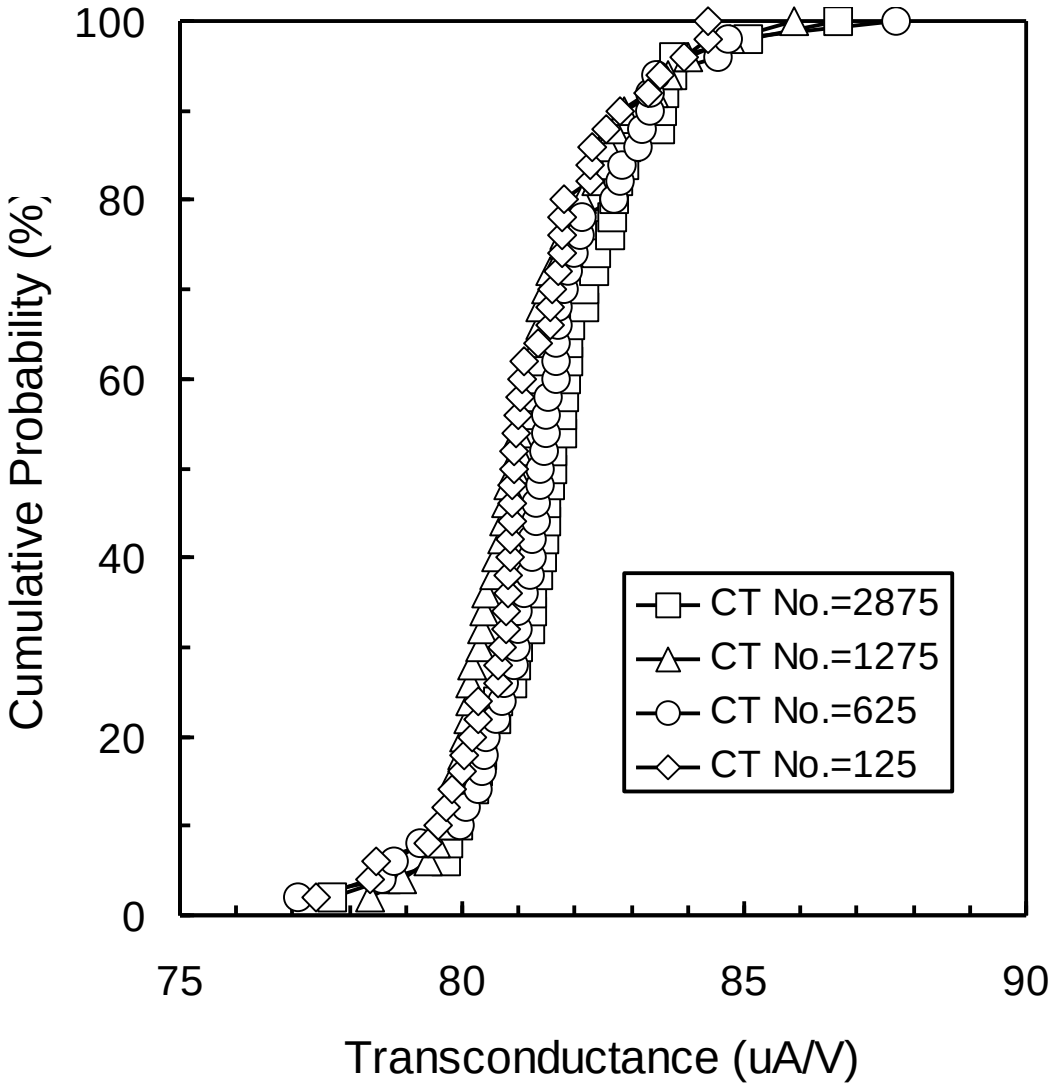
0.60
0.65
Threshold Voltage (V)

Fig.2(c)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20
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Cumulative Probability (%)
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85
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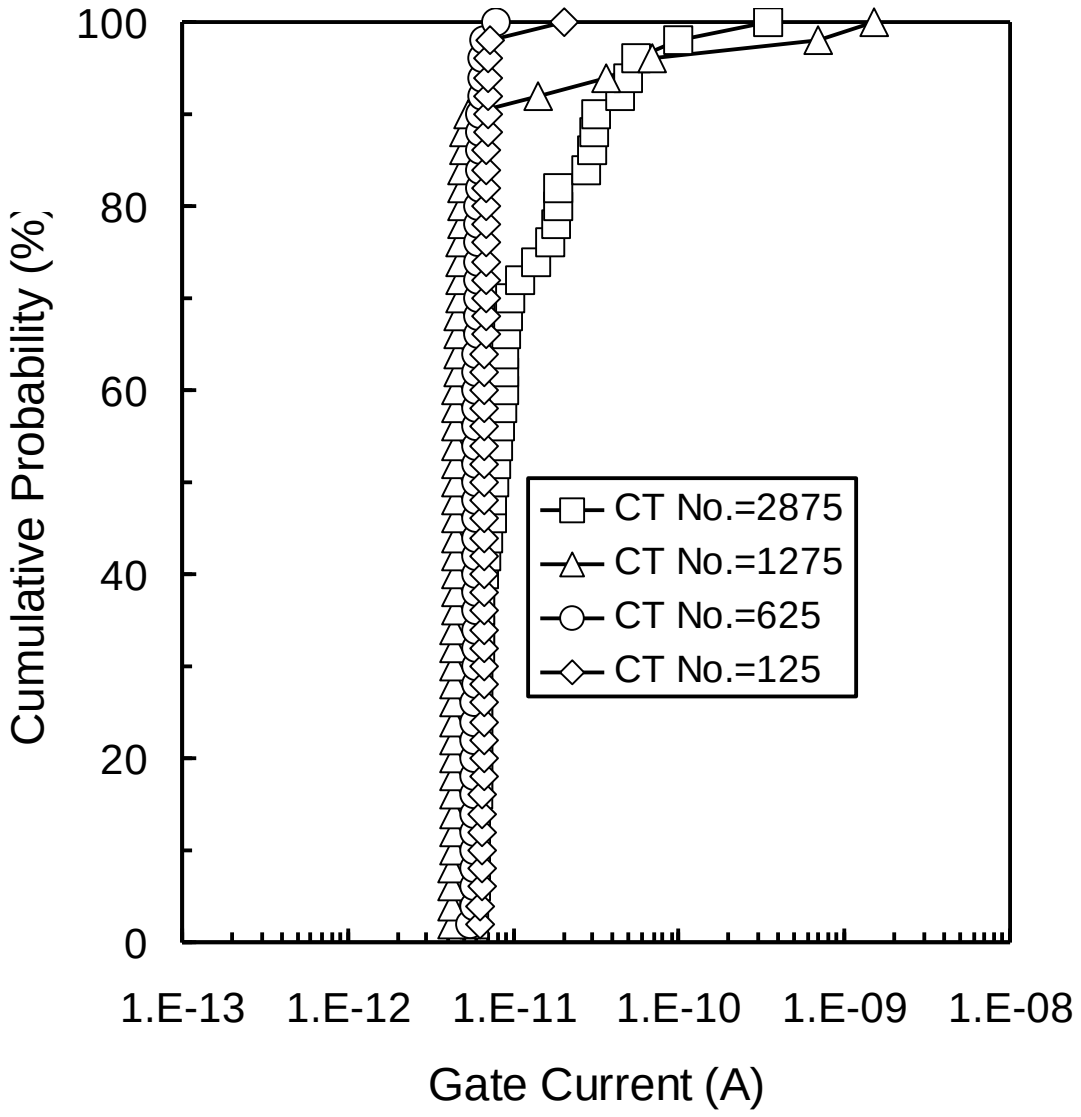
Transconductance (uA/V)
CT No.=2875
CT No.=1275
CT No.=625
CT No.=125

Fig.3(a)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80
60
40
20
0
Cumulative Probability (%)
CT No.=2875
CT No.=1275
CT No.=625
CT No.=125
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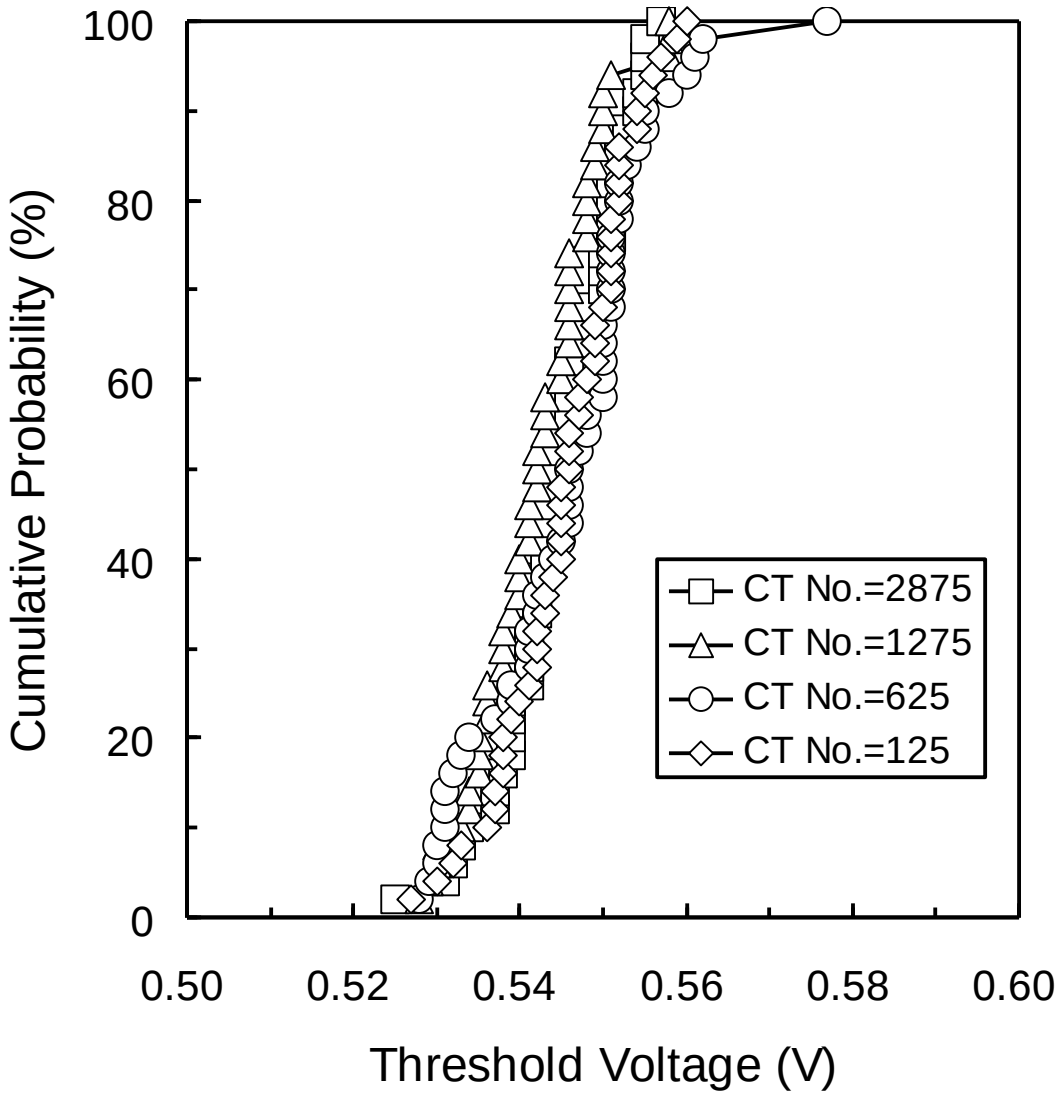
1.E-10
1.E-09
1.E-08
Gate Current (A)

Fig.3(b)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80
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Cumulative Probability (%)
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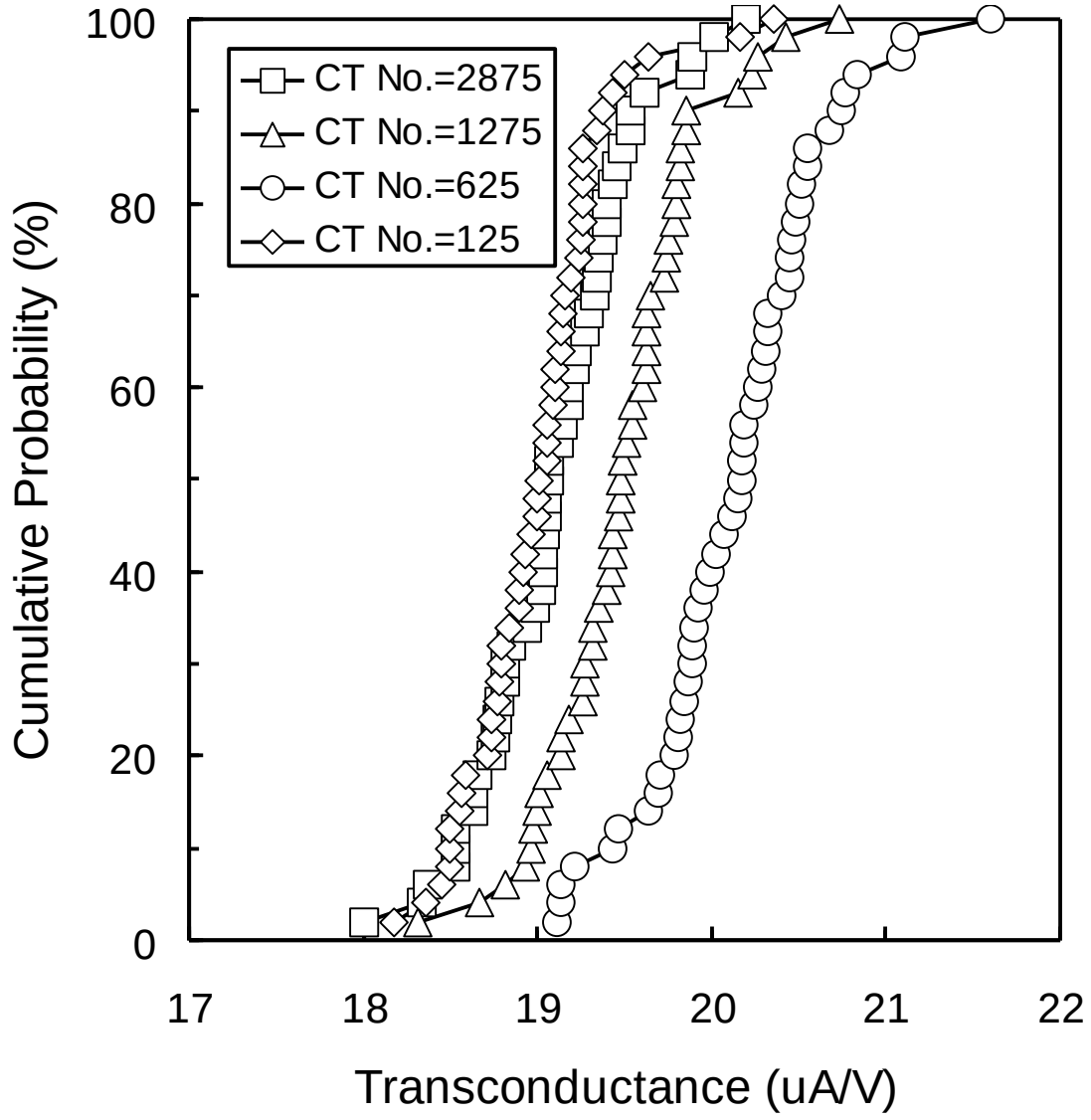
CT No.=2875
CT No.=1275
CT No.=625
CT No.=125

Fig.3(c)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CT No.=1275
CT No.=625
CT No.=125
Cumulative Probability (%)
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60
40
20
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17
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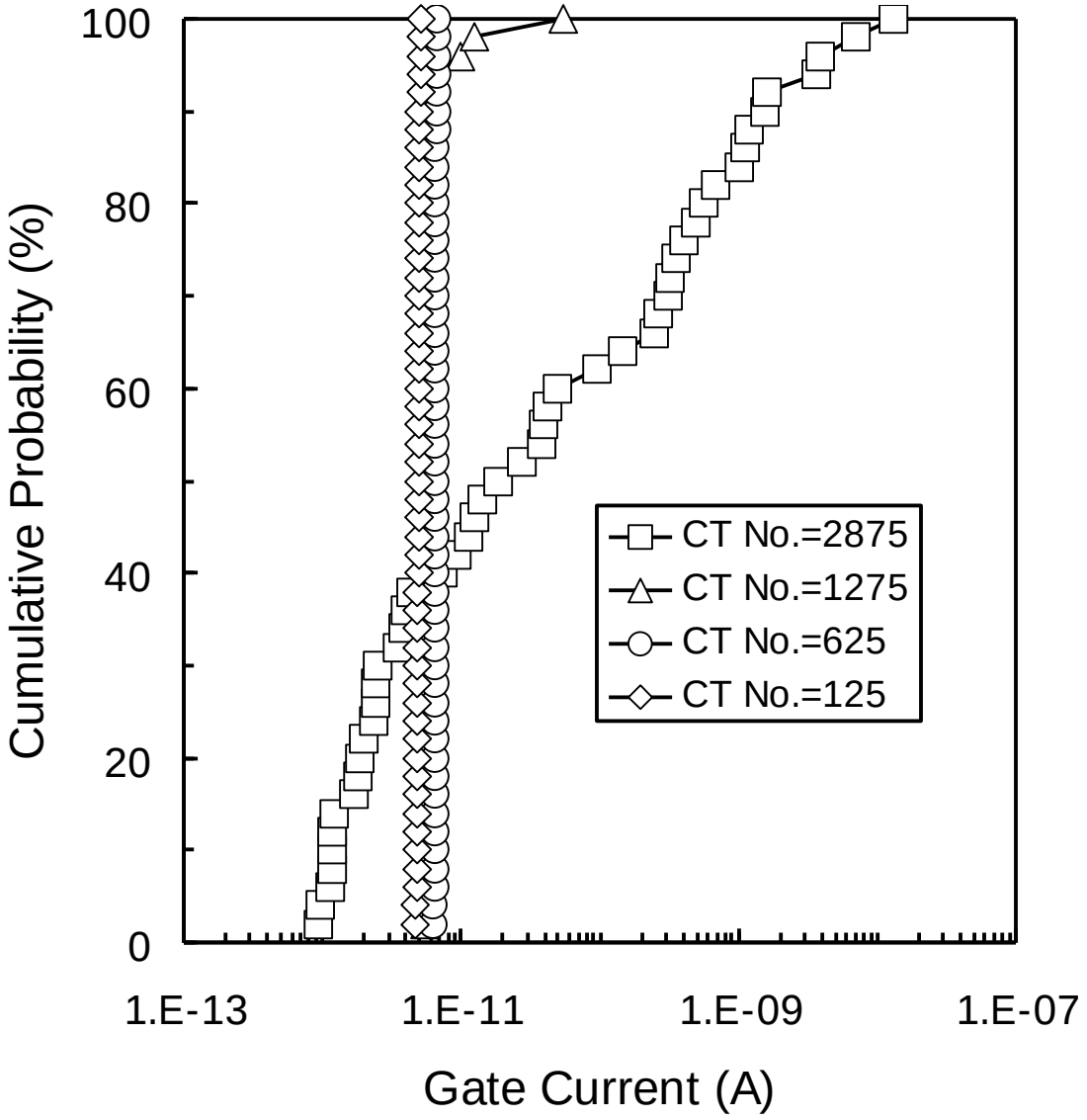
20
21
22
Transconductance (uA/V)

Fig.4(a)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60
40
20
0
Cumulative Probability (%)
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1.E-07
Gate Current (A)
CT No.=2875
CT No.=1275
CT No.=625
CT No.=125

Fig.4(b)

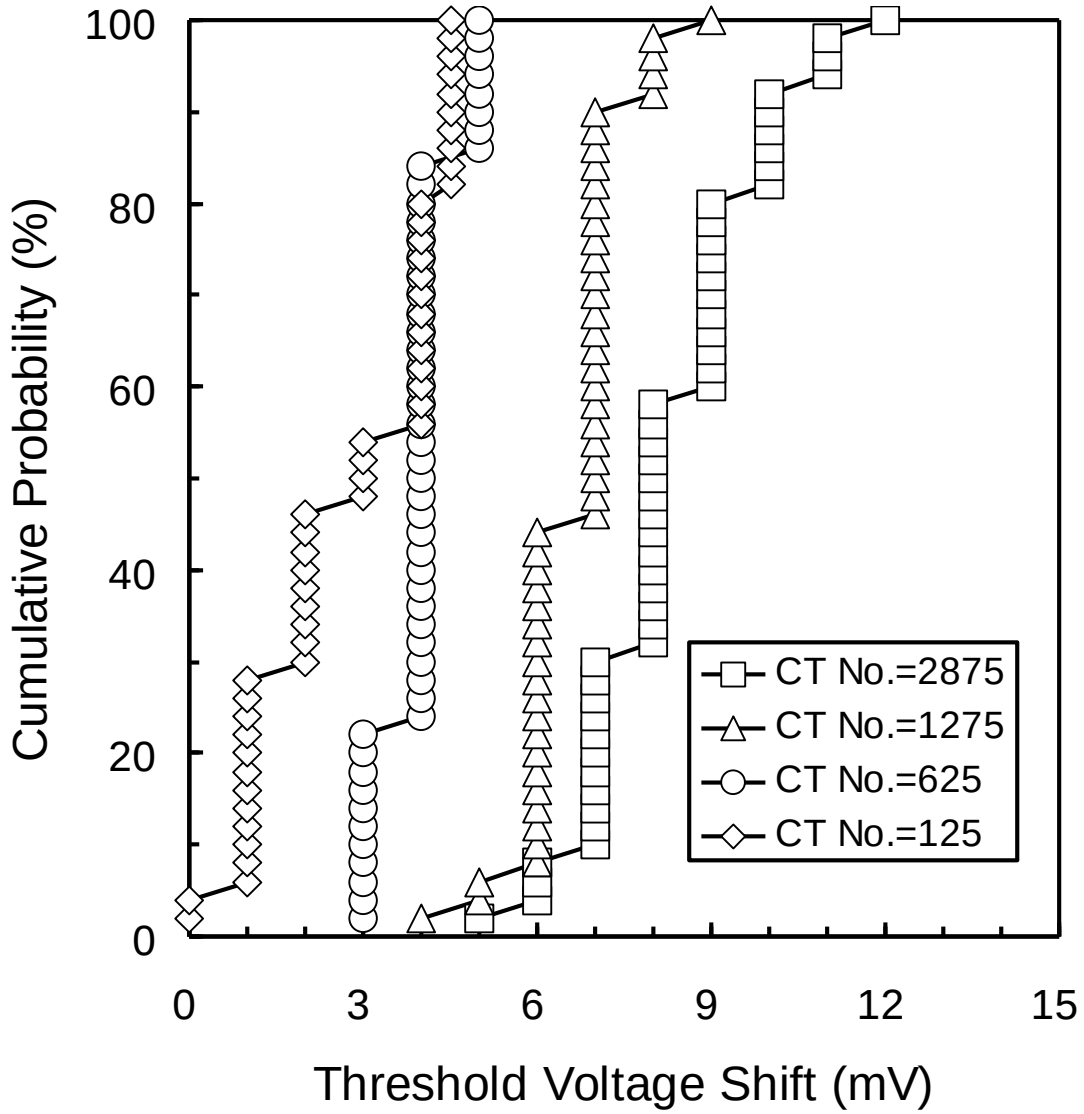
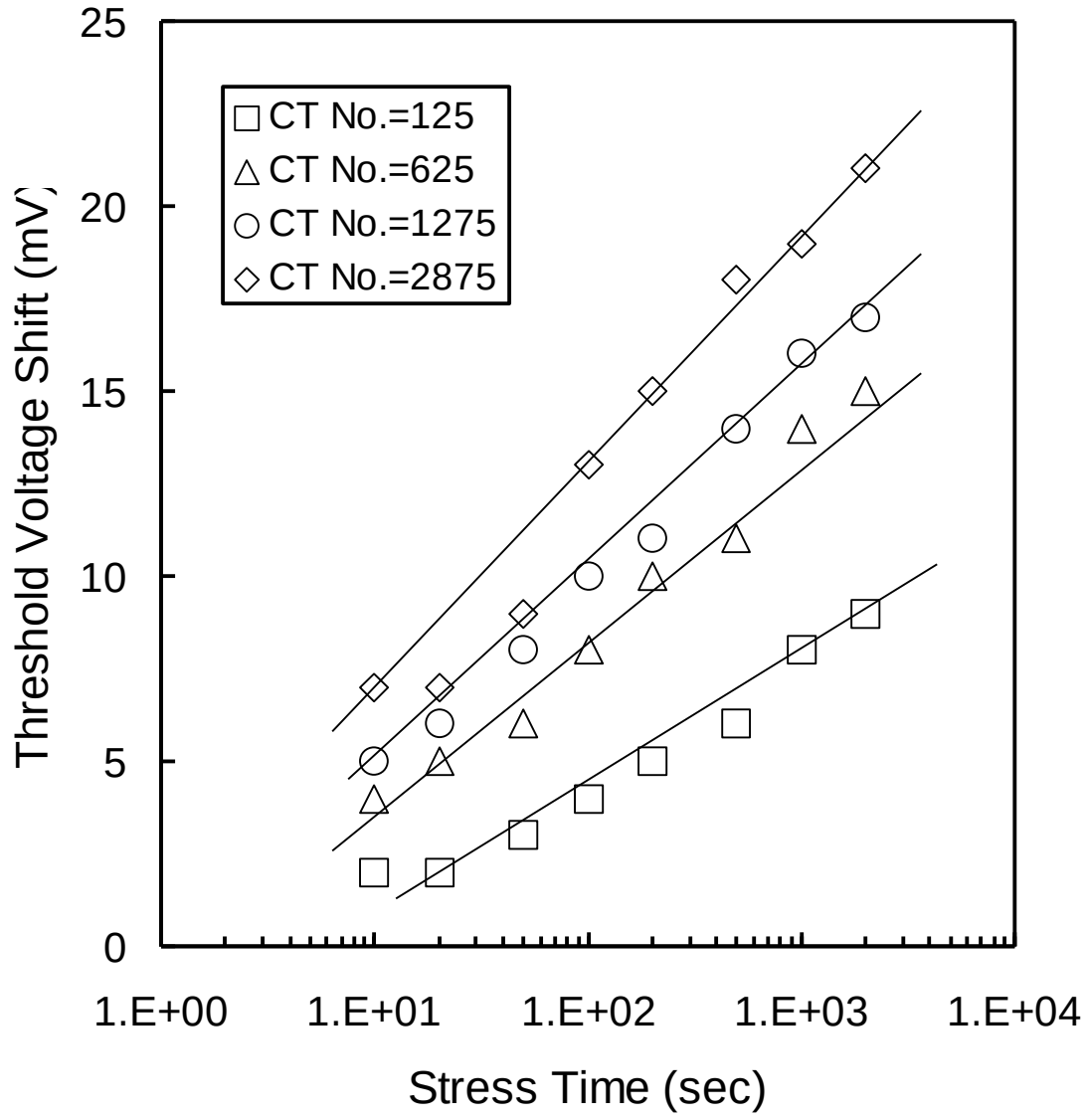

Cumulative Probability (%)
100
80
60
40
20
0
0
3
6
9
12
15
Threshold Voltage Shift (mV)
CT No.=2875
CT No.=1275
CT No.=625
CT No.=125

Fig.5(a)


25
20
15
10
5
0
Threshold Voltage Shift (mV)
CT No.=125
CT No.=625
CT No.=1275
CT No.=2875
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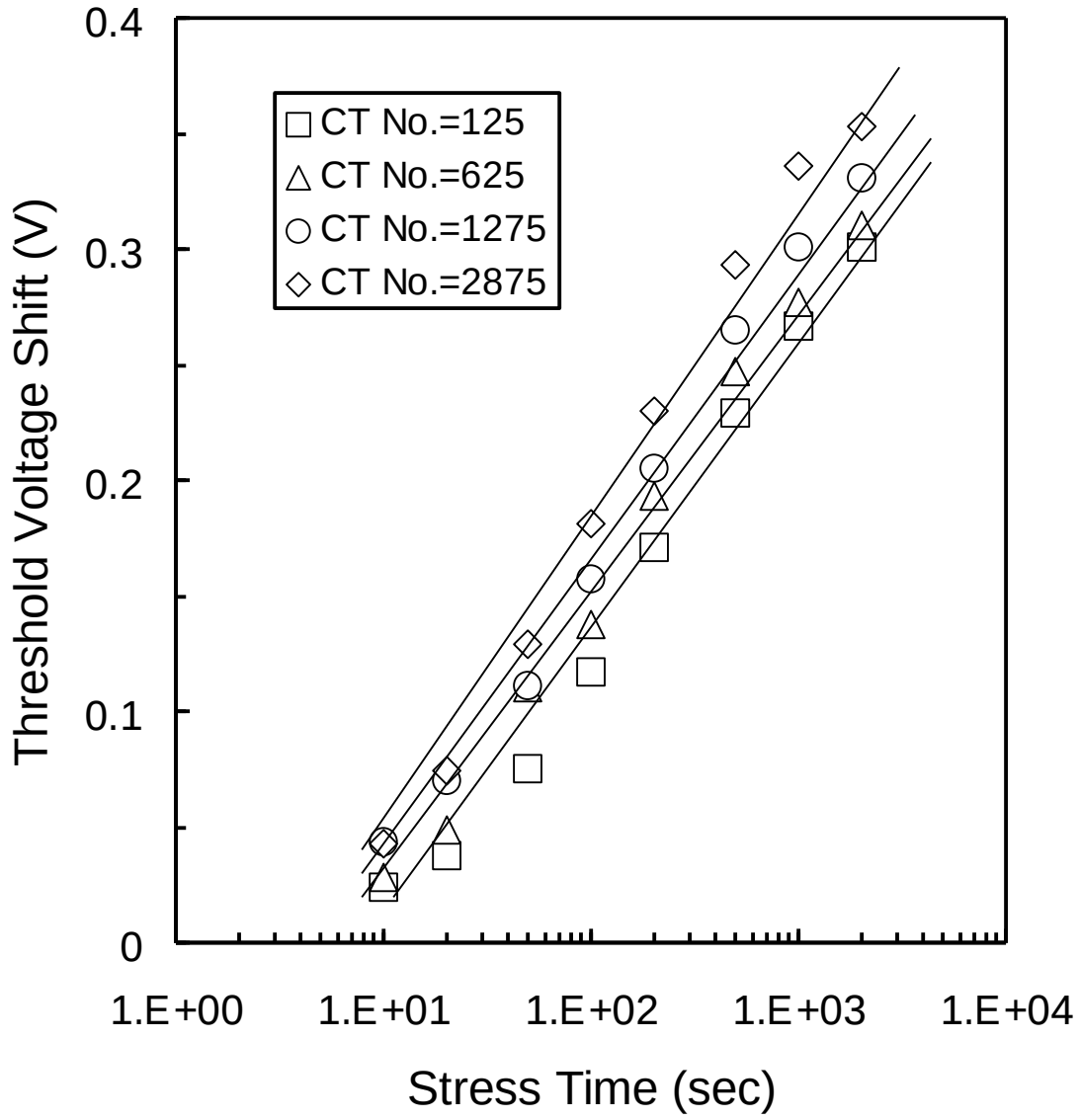
1.E+01
1.E+02
1.E+03
1.E+04
Stress Time (sec)

Fig.5(b)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0.1
0
Threshold Voltage Shift (V)
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CT No.=625
CT No.=1275
CT No.=2875
1.E+00
1.E+01
1.E+02
1.E+03
1.E+04
Stress Time (sec)

Fig.6

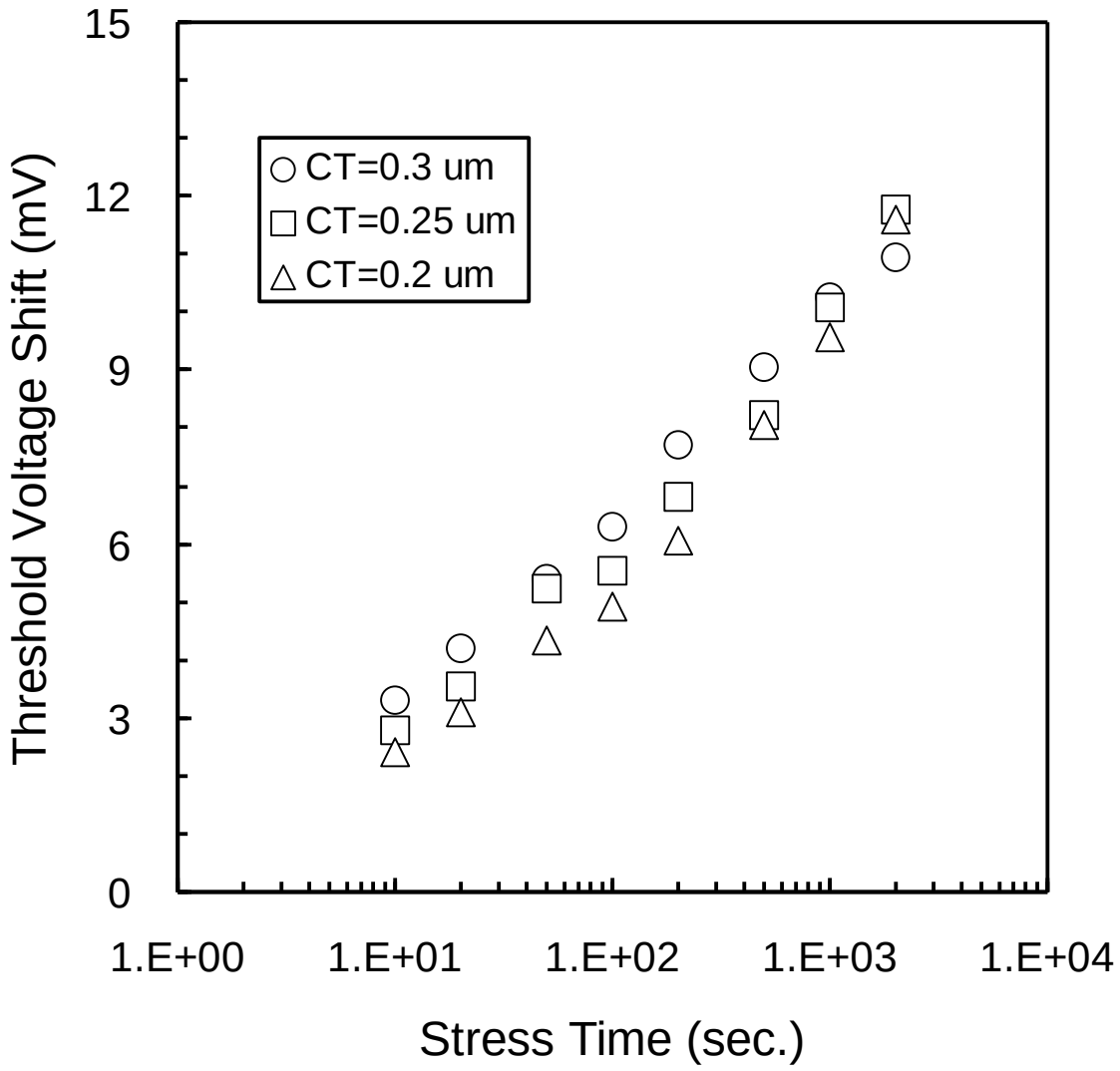
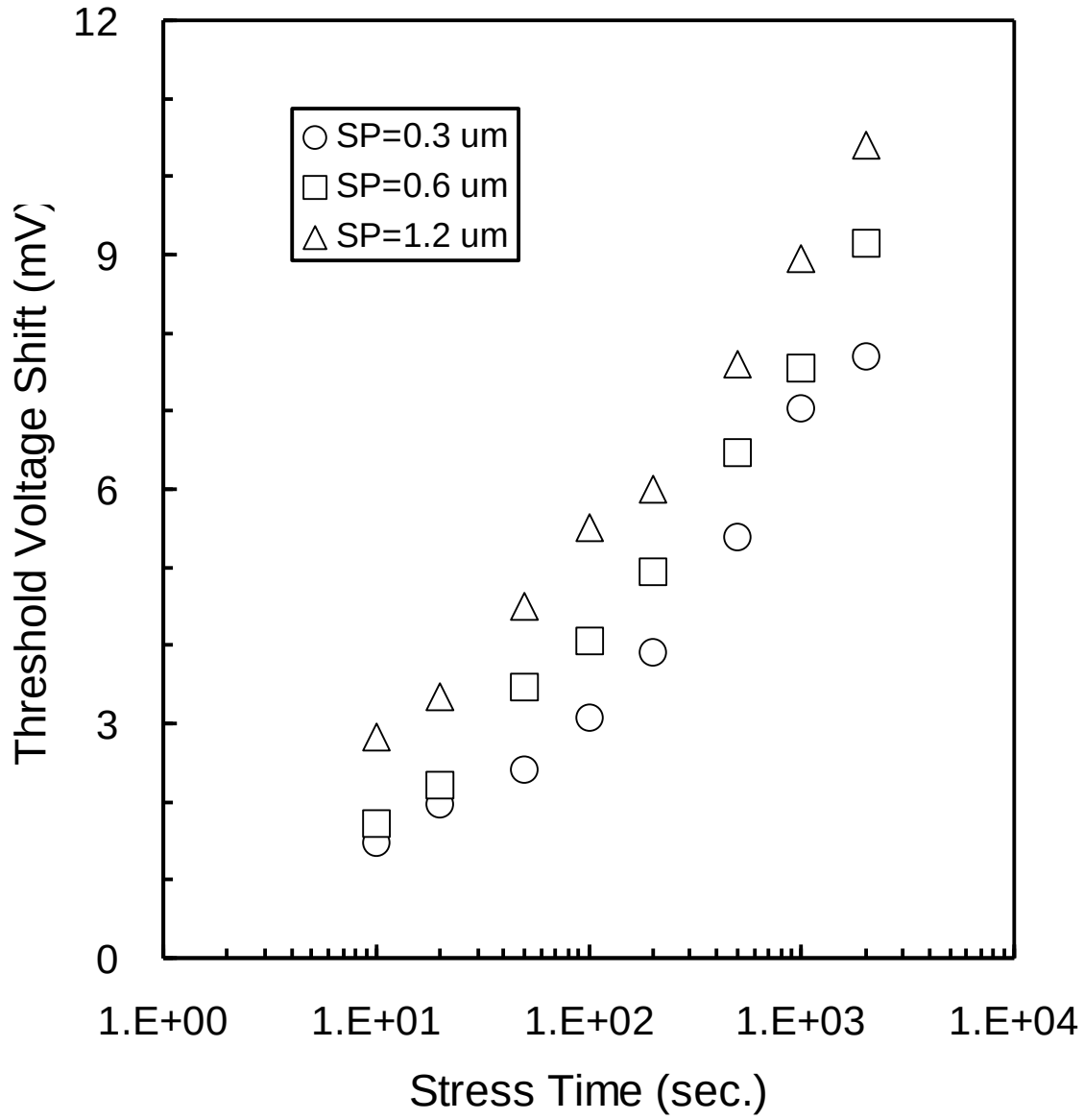

15
12
9
6
3
0
Threshold Voltage Shift (mV)
CT=0.3 um
CT=0.25 um
CT=0.2 um
1.E+00
1.E+01
1.E+02
1.E+03
1.E+04
Stress Time (sec.)

Fig.7


12
9
6
3
0
Threshold Voltage Shift (mV)
SP=0.3 um
SP=0.6 um
SP=1.2 um
1.E+00
1.E+01
1.E+02
1.E+03
1.E+04
Stress Time (sec.)