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金屬-鐵電-絕緣-半導體場效應電晶體之開發研究
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中文摘要

在這個研究中，我們使用高介電常數的三氧化二鑭絕緣層，來製作金屬–絕緣層–金屬(金氧金)電容測試結構。然後深入探究其操作原理，和實際應用面上所產生的問題，包含漏電流和其傳導機制、類比特性和其訊號失真機制、受電應力行為和劣化過程，以及介電絕緣層崩潰和可靠度特性探討等，以發展出適用於金屬–鐵電–絕緣–半導體場效應電晶體的良好絕緣層。根據實驗結果可歸結出，十奈米三氧化二鑭金氧金電容，其具有低漏電流（在外加電壓–1 V 時為 9.4 nA/cm^2），很高的崩潰電場（在 25 °C 時大於 7 MV/cm），低的電容電壓係數(頻率在 100 kHz 時為 671 ppm/V^2)，足夠高之電容密度(11.4 fF/μm^2)，以及高度穩定性和良好的可靠度等眾多優良特性。因此，鑭系高介電常數絕緣層在金屬–鐵電–絕緣–半導體場效應電晶體的應用上極具潛力。

關鍵字: 高介電常數，三氧化二鑭，金屬–絕緣層–金屬(金氧金)測試結構，金屬–鐵電–絕緣–半導體場效應電晶體

英文摘要

In this study, the metal-insulator-metal (MIM) test structure with the high dielectric constant (high-k) lanthanum oxide (La_2O_3) film was fabricated and characterized. In order to develop good insulator suitable for Metal-Ferroelectric-Insulator-Semiconductor Field Effect Transistor (MFIS-FET), the operational principles and the implementation issues of the high-k La_2O_3 MIM capacitor are discussed, including leakage current and conduction mechanisms, analog properties and distortion mechanisms, stress behaviors and degradation processes, as well as dielectric breakdown and reliability characteristics. In summary, according to the experimental results, a highly stable and reliable 10-nm La_2O_3 MIM capacitor with low leakage current (9.4 nA/cm^2 at –1 V), high breakdown strength (> 7 MV/cm at 25 °C), small VCC (671 ppm/V^2 at 100 kHz), and sufficient high capacitance density (11.4 fF/μm^2) has been successfully demonstrated. The results highlight the promise of the La-based high-k dielectrics as the insulator of MFIS-FET.

Keywords: high dielectric constant (high-k), lanthanum oxide (La_2O_3), metal-insulator-metal (MIM) test structure, Metal-Ferroelectric-Insulator-Semiconductor Field Effect Transistor (MFIS-FET)

一、前言及研究目的

隨著資訊產業膨渤發展與資訊媒體應用的日益普及，各類的資訊儲存器也就日形重要。其中電子記憶體無疑是最重要的一種。目前電子記憶體依功能主要可分為兩類，一類是強調高速存取的隨機記憶體(Random Access Memory, RAM)，其讀寫速度可在100 奈秒(ns)以下，但卻沒有永久記憶的功能。另一類則為非揮發性(Nonvolatile)的唯讀記憶體(ROM)，強調永久記憶的功能，但資料寫入的速度卻須微秒(μs)以上的時間。無法同時具備兩種功能，使得電子記憶體在應用上受到頗多限制。而鐵電薄膜的高介電係數，可應用於動態隨機記憶體，而高自發極化值則可應用於非揮發性記憶體，鐵電材料的引入為電子記憶體的發展另闢一個新的方向。。近年來由於薄膜製程技術的進步，已可在矽晶上製作出高品質的鐵電薄膜，使得它在產業的應用上受到極大重視。第一個由金屬-鐵電-半導體(Metal Ferroelectric Semiconductor, MFS)所構成的元件則是由吳泗堯(S.-Y. Wu)博士於1974年所發表[1]，其金屬-鐵電-半導體電晶體(Metal-Ferroelectric-Semiconductor Field Effect Transistor, MFIS-FET)基本的操作物理模型為Miller和McWhorter建立[2]。此元件結構與標準的金屬-絕緣體-半導體(Metal Insulator Semiconductor, MIS)相似，只不過絕緣體被鐵電薄膜所取代，不過由於鐵電薄膜與半導體的介面並不穩定，在操作過程中電荷會從矽晶表面穿過原始氧化層而陷於鐵電薄膜表面，因此元件並未能真正發揮功效。此種記憶體由於在元件製作過程中，鐵電薄膜與半導體之間容易有元素相互擴散的問題，直接影響閘極通道狀態，因此成為發展上最大的障礙。

為了要改善鐵電材料和半導體矽的接面品質，因此有許多論文開始在中間加入緩衝絕緣層來改善介面特性，使用CaF2 [3]和Al2O3 [4] 緩衝絕緣層在金屬-鐵電-絕緣-半導體電容結構上，以及使用MgO [5]和SiO2 [6]緩衝絕緣層在金屬-鐵電-絕緣-半導體電晶體結構上。雖然加入緩衝絕緣層後能改善接面特性，然而卻無法延長儲存在鐵電層中的極化電荷(Polarization Charge, FP)的保存時間(Retention Time)，以致於此金屬-鐵電-絕緣-半導體場效應電晶體領域仍處於研究發展階段，無法大量生產運用於工業界的產品上面。已有論文[7]特別指出兩種原因對極化電荷的保存時間影響的重要性，其一為在鐵電材料層所自我產生的極化電場(Depolarization Field, *Edp*)效應[8]，其二為閘極漏電流的影響[9]，此兩種因素會隨時間的增長，漸漸地抵銷鐵電材料內所儲存的極化電荷，使得極化電荷對通道的影響力消失，無法維持記憶體的特性。其中極化電荷(FP)是外界施加電壓寫入後造成的，如果要降低極化電場的影響力，唯有從提高絕緣層的電容值下手，即是選取具有高介電係數的絕緣材料，才能降低極化電場(*Edp*)效應的影響。而為了減少漏電流的注入效應，最直接的方法就是增加絕緣層厚度(ex: >10 nm) [10], [11]，來降低跨在絕緣層上的電場，然而持續增加了絕緣層厚度會造成絕緣層的電容值變小，當電容值變小時，極化電場(*Edp*)會因此增加，而又會隨時間增加漸漸地抵銷鐵電材料內所儲存的極化電荷(FP)，因此這兩者效應是互相抵制。所以減少閘極漏電流的第二種方法，就是從選擇高矽和絕緣層價帶(或導帶)的能帶差的高介電絕緣層下手[12]。電晶體在操作區間內的漏電流不能大於10 $\mu A/cm^2$，如此的漏電流才能維持極化電荷不被漏電流中和，造成降低金屬-鐵電-絕緣-半導體電晶體的記憶特性和減少記憶開口的電壓。此外極化電荷量和絕緣層的介電常數有很大的關係，選擇越高介電常數的絕緣層，才能產生更大的極化電荷量，使金屬-鐵電-絕緣-半導體電晶體符合鐵電的電滯曲線操作。為了要維持金屬-鐵電-絕緣-半導體電容系統的電中性，在操作上能承受電滯曲線上的電荷量，除了選擇高介電係數的絕緣層外，在使鐵電層經過矯頑電場的

施加後產生極化電荷儲存的狀態，絕緣層也需具有可耐高的電場(～4 MV/cm)，在此電場的操作下漏電流小於10 μA/cm^2，如此的漏電流位準為一般記憶體最低要求。

因此，本研究計畫目的在開發整合良好的高介電係數絕緣層在金屬-鐵電-絕緣-半導體電晶體的應用。根據文獻上的報導，三氧化二鑭(La_2O_3)緣層具有大的能隙(Energy Bandgap > 5 eV) [13]，相對高的介電常數(20-30) [13], [14], [15]，高崩潰電場[16]，低的界面態密度(interface state density) [13], [14]，低漏電流[13], 好的絕緣層可靠度[17]等眾多優點。是故在這個研究中，我們使用高介電常數的三氧化二鑭絕緣層，來製作金屬-絕緣層-金屬(金氧金)電容測試結構。然後深入探究其操作原理，和實際應用面上所產生的問題，包含漏電流和其傳導機制、類比特性和其訊號失真機制、受電應力行為和劣化過程，以及介電絕緣層崩潰和可靠度特性探討等，以發展出適用於金屬-鐵電-絕緣-半導體場效應電晶體的良好絕緣層。

二、研究方法

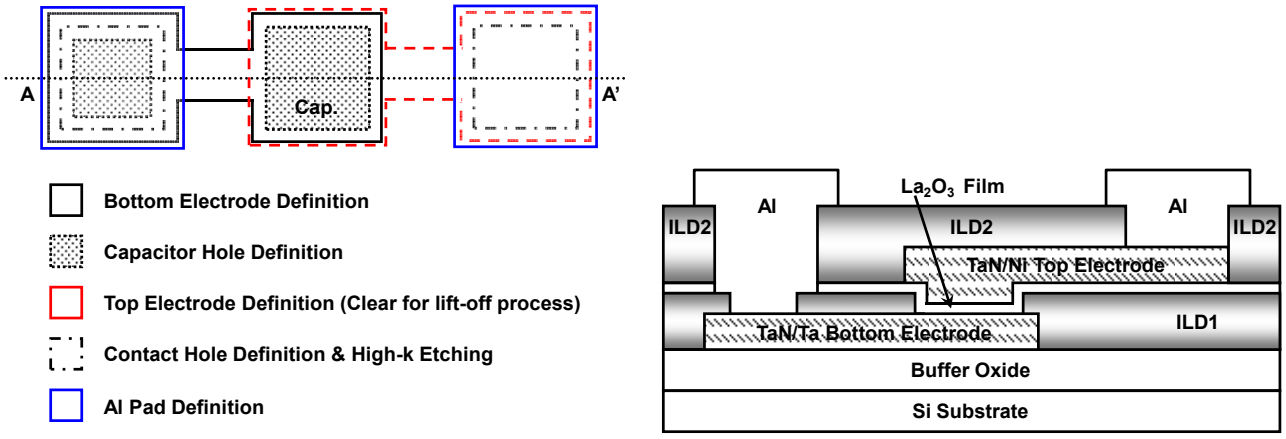
The schematic layout and its cross section along the A-A' line of the fabricated La_2O_3 MIM capacitors are shown in Figs. 1(a) and 1(b), respectively. The main fabrication steps were summarized below. After performing the standard RCA clean process to remove the native oxide and any contamination, the 1-μm thermal oxide was grown on 6-inch Si wafer as an isolation buffer layer by using wet oxidation. And then, the 200-nm tantalum (Ta) layer and the 50-nm tantalum nitride (TaN) layer were subsequently deposited on buffer oxide layer as the bottom electrode by a reactive sputtering system. Ta layer and TaN layer were used to reduce the parasitic resistance and to serve as a diffusion barrier layer, respectively. Before defining the bottom electrode of the MIM capacitor, the surface of TaN was treated by ammonia (NH_3) plasma nitridation at 300 mtorr with the RF power of 100 watts for 10 minutes to reduce the interfacial layer during the following high-k annealing processes. Besides, the metal layer TaN with NH_3 treatment has more flat surface roughness so that the leakage current of the MIM capacitor could be reduced under bottom injection condition.

The bottom electrode TaN/Ta was lithographically patterned and defined by employing a transformer-coupled-plasma (TCP) etcher with chlorine-based gas. Subsequently, the 200-nm tetraethoxylsilane (TEOS) oxide film used as the first inter-layer dielectric (ILD) isolation was deposited by utilizing a plasma-enhanced chemical vapor deposition (PECVD) system at 300 °C. The capacitor region and the bottom contact region were etched by buffered oxide etchant (BOE) solution after being opened by optical lithography process. Afterwards, the lanthanum oxide (La_2O_3) was deposited by using electron beam evaporation. The high-k dielectric La_2O_3 film on bottom electrode was annealed at 400 °C in O_2 ambient to improve its quality via fully oxidation and defects elimination. After lithography process to define the top electrode region, the 60-nm nickel (Ni) and the 30-nm TaN were subsequently deposited by electron beam evaporation and reactively sputtering, respectively. And then, the top electrode with Ni/TaN bi-layer metal was formed by using lift-off technique.

Next, the 300-nm TEOS oxide film served as the second ILD passivation layer was deposited by using a PECVD system at 300 °C. Because the La_2O_3 high-k dielectric film and the TaN metal were hardly etched by BOE solution, the contact holes were patterned by two-step

etching process for interconnection. Firstly, the 300-nm ILD passivation on contact hole region was removed by BOE solution and its could be etched, and the etching process could be stopped on the top of the TaN electrode and the La_2O_3 film. Secondly, the mixed solution of H_3PO_4: HNO_3: CH_3COOH: H_2O = 50: 2: 10: 9 heated to 60 °C was used to dissolve La_2O_3 film with high etching selectivity to the ILD passivation layer and the TaN electrodes. After the contact holes were opened by two-step wet etching process, the aluminum (Al) film of 500 nm was deposited by using a thermal evaporation system. Finally, the aluminum pads were lithographically patterned and also etched by the mixed solution of H_3PO_4: HNO_3: CH_3COOH: H_2O = 50: 2: 10: 9 at 60 °C. Ultimately, the MIM capacitors with La_2O_3 high-k dielectrics were accomplished. It was noteworthy that the maximum temperature during MIM capacitors fabrication was 400 °C, which was compatible with VLSI backend process.

An automatic measurement system consisted of a person computer (PC), Agilent-4156C, Agilent-4284A, Agilent switch, and a probe station is used for DC and low-frequency measurement of the fabricated devices. The properties of the La_2O_3 MIM capacitor are measured by the temperature-controlled chuck of the probe station, such as leakage current, capacitance density, breakdown biased voltage, and reliability characteristics. For all of electrical measurements, the voltage and the altering signal are applied to the top electrode while the bottom electrode was grounded. The leakage current-voltage (*J*-*V*) measurements are preformed on the Agilent-4156C semiconductor parameter analyzer. The capacitance-voltage (*C*-*V*) curves are measured by the Agilent 4284A precision impedance meter, and the dielectric loss-voltage (*D*-*V*) curves could also be observed at the same time. The biased voltage on the top electrode of the La_2O_3 MIM capacitor sweeps from −2 V to 2 V at frequencies varying from 10 kHz to 500 kHz by applying an ac signal with 25-mV amplitude. Moreover, from the viewpoint of practical use, it is very important to clarify the stability of MIM capacitor properties during long-term voltage stress. Therefore, the constant voltage stress (CVS) in the range of −4 V to −5 V at the temperature of 25°C is conducted by utilizing the Agilent-4156C semiconductor parameter analyzer. The *C*-*V* and *J*-*V* characteristics of La_2O_3 MIM capacitors are also measured at various time intervals during CVS testing.



(a) (b)

Fig. 1 The schematic layout of the La_2O_3 high-k MIM capacitors. (b) The cross-sectional structure along the A-A' dashed line in the layout shown in (a).

三、結果與討論

Figure 2 shows the *C*-*V* and *J*-*V* characteristics of the 10-nm La_2O_3 MIM capacitor. The capacitance density at zero bias is about 11.4 fF/μm^2, and the leakage current densities at −1.5 and +1.5 V are 16 and 56 nA/cm^2, respectively. The quadratic voltage coefficient of capacitance (α), used to depict the voltage dispersion or voltage dependency of capacitance, is obtained from fitting the *C*-*V* curves by the second-order polynomial equation:

$$C(V) = C_0 \times (\alpha \times V^2 + \beta \times V + 1), \quad (1)$$

where C_0 is the capacitance at zero bias. The α values of the 10-nm La_2O_3 MIM capacitor measured at 10 and 100 kHz are 775 and 671 ppm/V^2, respectively. The positive α represents a capacitance density rise with the increase in applied voltage, which may be attributed to the high degree of electric field polarization and carrier injection. During the voltage sweeping, some of the injected carriers would be captured by the interface trap states existing in the dielectric near the injection electrode. These trapped charges could induce dipoles following the alternating signals with a dipole relaxation time. Moreover, the other injection carriers become excess mobile charges in the insulator, and these mobile charges also follow the small ac signals with a free carrier relaxation time that depends on the mobility and density of carriers. The dipole and free carrier relaxation time contribute to various frequency-dependent characteristics in RF/analog MIM capacitors. As the measurement frequency increases, the trapped-charge-induced dipoles and the excess mobile charges hardly follow the ac signal, corresponding to the longer relaxation times of these dipoles and mobile charges. Thus, the capacitance fluctuation due to the varied applied voltages becomes smaller and results in the lower α with increasing frequency. While both dipole polarization and free carrier polarization could modulate the capacitance, the free carrier effect is believed to play the major role in the voltage dependence of capacitance, but is negligible for the zero-biased capacitance where the carrier injection ceases.

To further investigate the stability of the La_2O_3 MIM capacitor under electrical stress, the CVS test was carried out. Figure 3 shows the relative capacitance variation [$\Delta C/C(t=0)$] as a function of stress time at various CVS voltages from −4.6 to −5 V. The relative capacitance variation is defined as

$$\frac{\Delta C}{C(t=0)} = \frac{C_0(t) - C_0(t=0)}{C_0(t=0)}, \quad (2)$$

where $C_0(t=0)$ is the initial capacitance at zero bias before stress, and t is the stress time. [$\Delta C/C(t=0)$] increases with the CVS voltage and the stress time. On the other hand, [$\Delta C/C(t=0)$] is also plotted as a function of the injected charge (Q_{inj}) in the inset of Fig. 3. The relative capacitance variation increases with a logarithmic increase in Q_{inj} regardless of the stress biases, which implies that the increasing charge trapping in dielectrics during CVS is responsible for the capacitance variation. The trapped charges in the preexisting traps and in stress-induced traps generate dipoles to increase the local permittivity and the capacitance. Among them, the stress-induced dipoles contribute to the relative increase in capacitance with respect to its initial

condition, and that is the degradation of the capacitance. Specifically, the relative capacitance variation is proportional to the amount of stress-induced trapped charges. Furthermore, the trapping probability, the ratio of trapped charge variation, ΔQ_{trap}, to injected charge variation, ΔQ_{inj}, obeys a power law relation:

$$\frac{\Delta Q_{trap}}{\Delta Q_{inj}} = K \times Q_{inj}^{n}, \tag{3}$$

where K is the trapping efficiency as a function of the injected current density and the temperature, and the characteristic exponent n is a fraction. As a consequence, the logarithmic dependence of the relative capacitance variation on the injected charge is shown in the inset of Fig. 3. Moreover, the CVS conditions presented here exhibit a nearly linear relationship between Q_{inj} and stress time (not shown). The power law behavior of trapping probability brings about the slower increase in capacitance after long-term stress. Both the linear relationship between $[\Delta C/C(t=0)]$ and $\ln(Q_{inj})$ and the saturation-like behavior mentioned above are similar to the flatband voltage shift of a metal-oxide-semiconductor (MOS) capacitor under electrical stress that has been reported in many studies.

In considering the long-term stress behaviors of capacitance, Fig. 4 depicts the 10-year stability extraction of a fabricated 10-nm La_2O_3 MIM capacitor estimated by the relative capacitance variation. It could be obtained from the extrapolated $[\Delta C/C(t=0)]$ versus stress time to 10 years, as shown in the inset of Fig. 4. The 10-year degradations of 10-nm La_2O_3 MIM capacitors with an 11.4 fF/μm^2 capacitance are 6.32, 4.09, and 2.61% under CVSs of –4.6, –4.4, and –4.2 V, respectively. The operation voltage guaranteeing 0% degradation for 10 years is extrapolated at –3.93 V.

The time dependence of $\alpha(t)$ normalized to its initial value $\alpha(t=0)$ under CVSs from –4.6 to –5 V is plotted in Fig. 5. It was found that $[\alpha(t)/\alpha(t=0)]$ decreases with increasing stress time for a given stress bias. In other words, CVS improves the voltage linearity of the high-κ La_2O_3 MIM capacitor. This may be explained by the reduced carrier mobility in the La_2O_3 dielectric due to the generation of stress-induced trap states under CVS, thus leading to a longer relaxation time of mobile charges. As mentioned before, α is dominated by the free carrier polarization. The inset of Fig. 5 shows the dependence of $[\alpha(t)/\alpha(t=0)]$ on the relative variation in dielectric loss $[\Delta D/D(t=0)]$ during stress. The relative variation in dielectric loss caused by CVS with respect to its initial values is acquired as

$$\frac{\Delta D}{D(t=0)} = \frac{D_0(t) - D_0(t=0)}{D_0(t=0)}, \tag{4}$$

where $D_0(t=0)$ is the initial dielectric loss at zero bias. The relative variation in D of the La_2O_3 MIM capacitor under CVS increases with stress time and voltage (not shown), similar to the trend of the relative variation in capacitance shown in Fig. 3. It is believed that the trap/detrap processes are responsible for the dielectric loss, and the increase in D under CVS is ascribed to the generation of stress-induced trap states. Furthermore, from the inset of Fig. 5, $[\alpha(t)/\alpha(t=0)]$ linearly decreases with a logarithmic increase in relative dielectric loss, and it maintains almost

the same slope independent of the stress voltage. This linear relationship further verifies the relationship between the amount of trap generation, responsible for the dielectric loss, and the reduction of free carrier mobility, responsible for the voltage dependence of capacitance. In other words, stress-induced trap states reduce the free carrier mobility in the dielectric and therefore increase the free carrier relaxation time that decreases the α of MIM capacitors under CVS. Additionally, the time dependence of $[\alpha(t)/\alpha(t=0)]$ at various measurement frequencies under a CVS of –4.8 V is shown in Fig. 6, and the inset presents the dependence of $[\alpha(t)/\alpha(t=0)]$ on the relative variation in dielectric loss $[\Delta D/D(t=0)]$. As the measurement frequency increases, the changes in $[\alpha(t)/\alpha(t=0)]$ become smaller. This is believed to be due to the smaller $\alpha(t=0)$ at higher frequency. From the inset of Fig. 6, $[\alpha(t)/\alpha(t=0)]$ linearly decreases with a logarithmic increase in relative dielectric loss, and the slope is again independent of the measurement frequencies, and the same as that obtained in Fig. 5. As a result, one can derive that changes in κ must vary linearly with changes in D as well.

Figure 7 exhibits the cumulative results of The time-zero dielectric breakdown (TZDB) for the 10-nm La_2O_3 MIM capacitors at the measurement temperature varied from 25 to 125°C in the case of top injection, the breakdown field (E_{BD}) of 50% failure probability declines from 7.35 to 5.66 MV/cm as the temperature rises from 25 to 125°C. Besides, from the Fig. 7, it can be noted that as the measurement temperature raises, the distribution of the E_{BD} data becomes narrower. This temperature dependence of TZDB is related to the damage created in the oxide during the measurement. When carrying out the measurement, a rapid increase in applied voltage results in a rapid rise in local current density of the dielectric to generate energetic carriers that could release the energy and distort or weaken the local molecular bonds of the dielectric film. The weakened molecular bonds become very susceptible to be broken by the further injection carriers, and then a localized defective (percolation) site forms. As a conductive percolation path develops shorting the two electrodes, the breakdown occurs. For the high temperature measurement, more energetic injection carriers are available to create damage leading to lower breakdown voltage than that of low temperature measurement. The effective defect forming process at elevated temperature not only reduces the E_{BD} magnitude, but also causes the dielectrics of different MIM capacitors break down at almost the same applied voltage.

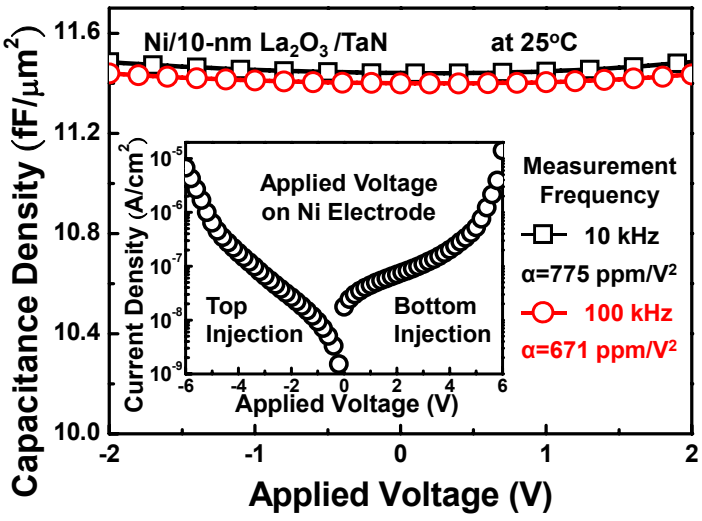


Fig. 2 The *C-V* curve, *J-V* curve, and the quadratic voltage coefficient (α) of a typical 10-nm La_2O_3 MIM capacitor.

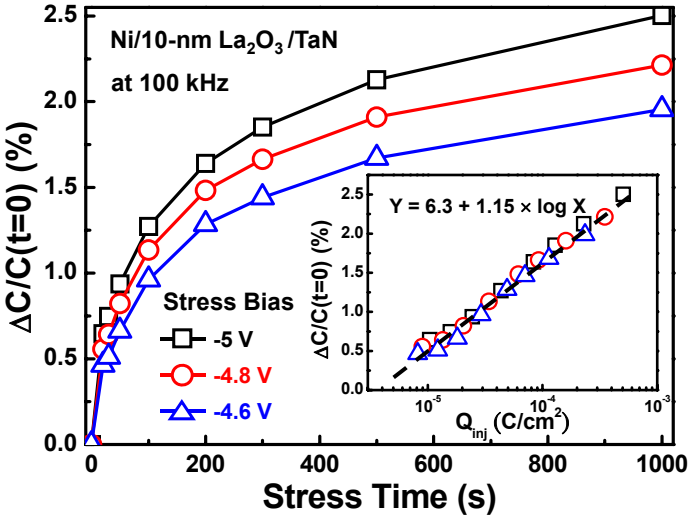


Fig. 3 Relative-capacitance variation $[C_0(t)-C_0(0)]/C_0(0)$ as a function of stress time and injection charges (Q_{inj}) at various CVS voltages from –4.6 V to –5 V.

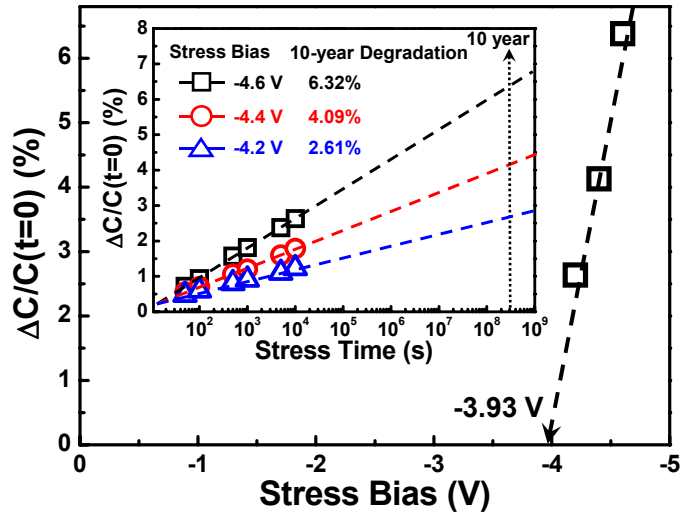


Fig. 4 The 10-year stability extraction of 10-nm La_2O_3 MIM capacitors estimated by the relative-capacitance variation.

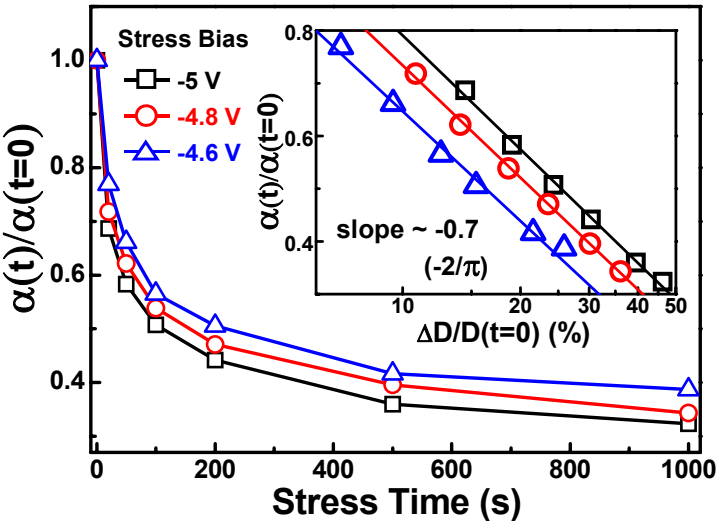


Fig. 5 Time dependence of the relative quadratic voltage coefficient of capacitance $\alpha(t)/\alpha(0)$ under a CVS of –4.6 V to –5 V.

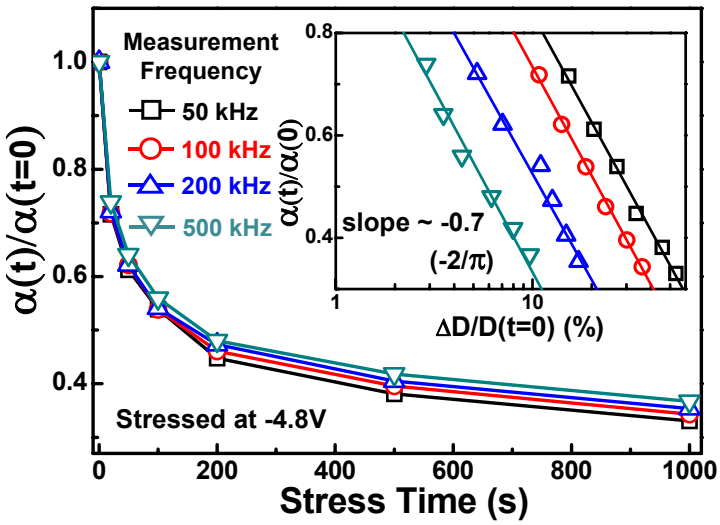


Fig. 6 Time dependence of the relative quadratic voltage coefficient of capacitance $\alpha(t)/\alpha(0)$ under a CVS voltage of –4.8 V with various measurement frequencies.

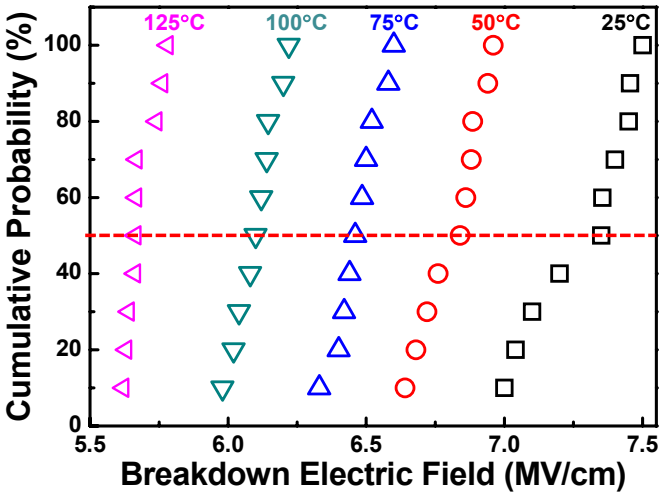


Fig. 7 The cumulative results of TZDB for the 10-nm La_2O_3 MIM capacitors at the measurement temperature varied from 25 °C to 125 °C.

四、結論

In this study, the MIM test structure with the high-k La_2O_3 film was fabricated and characterized. The operational principles and the implementation issues of the high-k La_2O_3 MIM capacitor are discussed, including leakage current and conduction mechanisms, analog properties and distortion mechanisms, stress behaviors and degradation processes, as well as dielectric breakdown and reliability characteristics. In summary, a highly stable and reliable 10-nm La_2O_3 MIM capacitor with low leakage current (9.4 nA/cm^2 at –1 V), high breakdown strength (> 7 MV/cm at 25 °C), small VCC (671 ppm/V^2 at 100 kHz), and sufficient high capacitance density (11.4 fF/μm^2) has been successfully demonstrated. The results highlight the promise of the La-based high-k dielectrics as the insulator of MFIS-FET.

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六、成果自評

此計畫經費支持一位博士班及一位碩士班學生執行研究及畢業。部分研究成果已整理成論文，目前已發表或已被接受之論文共計有一篇國際期刊論文，兩篇國際研討會論文，論文名稱與投稿期刊分別如下所示。且研究成果之論文撰寫與投稿仍在持續進行中。

七、發表國際期刊和國際會議論文

1. S.-H. Wu, C.-K. Deng, T.-H. Hou, and B.-S. Chiou, "Stability of La_2O_3 Metal-Insulator-Metal Capacitors Under Constant Voltage Stress," accepted by *Japanese Journal of Applied Physics*.
2. S.-H. Wu, C.-K. Deng, T.-H. Hou, and B.-S. Chiou, "Stability and Degradation Mechanism of La_2O_3 Metal-Insulator-Metal Capacitors Under Constant Voltage Stress," to be presented in *the 217th Meeting of ECS*, Vancouver, Canada, Apr. 25-30, 2010.
3. S.-H. Wu, C.-K. Deng, B.-S. Chiou, "Stabilities of La_2O_3 Metal-Insulator-Metal Capacitors Under Constant Voltage Stress," *Proc. of the 2009 International Conference on Solid State Devices and Materials (SSDM 2009)*, Sendai, Japan, Oct. 7-9, 2009, pp. 106-107.

出席國際會議報告書

撰寫時間： 99 年 1 月 26 日

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本人有幸得到貴單位補助，參加位於日本東北之宮城縣仙台市舉辦的2009年國際固態電子與材料會議(International Conference on Solid State Devices and Materials, SSDM 2009)，會議自10月7日至10月9日共舉行三天，並帶回資料隨身碟一份。這是此國際會議自1969年開始舉辦自今，首度提供參加者以USB隨身碟儲存的所有會議相關資料及會議發表論文。不僅查閱迅速方便，而且可節省掉以往提供紙本資料時的資源消耗，環保又有效率，獲得與會人士一致好評。由於SSDM堪稱固態電子領域中歷史悠久且相當重要的學術會議，不但有來自世界各地上千位的學術界、業界人士參加，系上也有許多教授及研究生共襄盛舉。

會議討論的主題共分十四個領域，包含Advanced Gate Stack / Si Processing and Material Science，CMOS Devices /Device Physics，Advanced Memory Technology，Applications of Nanotubes and Nanowires……等眾多現今固態電子中備受矚目及極具潛力的技術。置身其中，不單是可以學習到許多新技術、新知識，同時亦是與來自各地的科技研究人員交流的大好機會。而本人的論文“Stabilities of La_2O_3 Metal-Insulator-Metal Capacitors Under Constant Voltage Stress”，則發表於Characterization and Materials Engineering for Interconnect Integration領域中RF Device/Process Technology的Oral Session。報告時間為15分鐘，另外還有5分鐘的討論時間。由於現場聽眾提問討論踴躍，讓我獲益匪淺及得到許多靈感上的啟發。系上的柯教授研究群也有發表一篇論文於同一領域，不過是發表在Poster Session裡。

最後，再次感謝行政院國家科學委員會補助經費讓本人成行，有機會出席這麼重要的國際學術會議。不只學習、交流最新的技術與知識，為後續的研究奠定良好基礎，更讓我充分體驗日本的整潔與辦事執行效率。希望往後台灣在學術研究上能有更好的發展，在國際發光發亮！

Stabilities of La_2O_3 Metal-Insulator-Metal Capacitors Under Constant Voltage Stress

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1. Introduction

Recently, high-k metal-insulator-metal (MIM) capacitors integrated into backend interconnection as passive components have generated great interest for analog and RF applications [1], [2]. The stability of MIM capacitors is a key issue on precision performance, especially on the voltage linearity. Some studies [3], [4] have discussed the capacitance variation of SiO_2 MIM capacitors during electrical stress. However, the degradation of the MIM capacitor with high-k dielectric has not been well characterized. In this paper, the behaviors of La_2O_3 MIM capacitors under constant voltage stress (CVS) were investigated. The correlations among the injected charges (Q_{inj}), the capacitance change ($\Delta C/C_0$), the quadratic voltage coefficient of capacitance (α), and the dielectric loss (D) of the La_2O_3 MIM capacitor were also discussed.

2. Device Fabrication and Experimental Procedures

This work focused on a 10-nm La_2O_3 MIM structure with an 11.4-fF/μm^2 capacitance density and an area of 2500 μm^2. The schematic layout and the schematic cross section of the capacitor along the A-A' line in the layout are shown in Figs. 1(a) and 1(b). The high-k dielectric La_2O_3 film was deposited by e-beam evaporation and annealed in O_2 ambient to improve its quality. The top bi-layer (TaN/Ni) and bottom (TaN/Ta) electrodes were deposited by a reactive sputtering. All process temperatures during MIM capacitors fabrication were below 400 °C compatible with backend process. The samples were subjected to constant voltage stress in the range of −4.2 V to −5 V applied on the top electrode (Ni), and their capacitances variation were also measured at 25°C using an LCR meter at various intervals during CVS testing.

3. Results and Discussion

Fig. 2 shows *C-V* and *J-V* characteristics of the 10-nm La_2O_3 MIM capacitor. The leakage current is below 10^{-7} A/cm^2 under the applied voltage of ±2 V. The quadratic voltage coefficient (α) of capacitance could be fitted by the second order polynomial equation: $C(V) = C_0 \cdot (\alpha \cdot V^2 + \beta \cdot V + 1)$, where C_0 is the capacitance at zero bias. Hence, the values α of 10-nm La_2O_3 MIM capacitor measured at 10 kHz and 100 kHz are 775 ppm/V^2 and 671 ppm/V^2, respectively.

Fig. 3 illustrates the correlations among the relative capacitance variation $[C_0(t)-C_0(0)]/C_0(0)$, the stress time, and the injection charges (Q_{inj}) at various CVS voltages from −4.6 V to −5 V, where $C_0(t=0)$ is an initial capacitance at zero bias. As shown in the inset of Fig. 3, the relative-capacitance variation increases with a logarithmic increase in Q_{inj} regardless of the stress biases, which implies charge trapping in dielectric films [5]. When the carriers inject into the La_2O_3 dielectric film during CVS stress, the trapped charges could generate dipoles to increase the local permittivity and then contribute to the degradation of the capacitance [3], [4]. Besides, as shown in Fig. 3, after the $[C_0(t)-C_0(0)]/C_0(0)$ rapidly increases in the initial stress, it tends to saturate after the 1000-s stressing. This saturation could be attributed to the trapped charges near the top electrodes. After the pre-existing trap states are rapidly filled by injection charges to increase the capacitance, the trapped charges would increase the barrier height near the injection electrode and result in a saturation phenomenon [6].

Fig. 4 depicts the 10-year stability extraction of a fabricated 10-nm La_2O_3 MIM capacitor estimated by the relative-capacitance variation. It could be obtained from the extrapolated $[C_0(t)-C_0(0)]/C_0(0)$ versus stress time to 10 years, as shown in the inset in Fig. 4. The 10-year degradations of 10-nm La_2O_3 MIM capacitors with an 11.4-fF/μm^2 capacitance are 6.32 %, 4.09 %, and 2.61 % under −4.6 V, −4.4 V, and −4.2 V, respectively. The safety 10-year operation voltage with below 1-% degradation could be extrapolated by around −4 V. This long-term stability is useful for the sub-65 nm technology node, whose operating voltage is smaller than 1.5 V.

Time dependence of $\alpha(t)$ normalized to its initial value $\alpha(0)$ under CVS biases from −4.6 V to −5 V is plotted in Fig. 5. The inset presents the dependence of $\alpha(t)/\alpha(0)$ on the relative variation in dielectric loss $[D_0(t)-D_0(0)]/D_0(0)$ during stressing, where $D_0(0)$ is the fresh dielectric loss at zero bias. It can be found that $\alpha(t)/\alpha(0)$ decreases with the increasing stress time for a certain stress bias. The reason for the decrease in the voltage dependence of capacitance is that the carrier mobility is reduced by the stress-induced trap states, and then hardly follows the alternating signal with a higher relaxation time [7]. Besides, $\alpha(t)/\alpha(0)$ linearly decreases with a logarithmic increase in relative dielectric loss, but it still maintains almost the same slope under various stress voltages. It further verifies the change in voltage dispersion of capacitance is ascribed to the stress induced traps.

Dependence of $\alpha(t)/\alpha(0)$ on stress time under a CVS of −4.8V with various measurement frequencies is exhibited in Fig. 6, and the inset presents the dependence of $\alpha(t)/\alpha(0)$ on the relative variation in dielectric loss $[D_0(t)-D_0(0)]/D_0(0)$. As the measurement frequency increases, the changes in $\alpha(t)/\alpha(0)$ become smaller, and the correlation between $\alpha(t)/\alpha(0)$ and the relative variation in D has been confirmed again.

4. Conclusions

The stabilities of MIM capacitors with La_2O_3 dielectric under CVS are investigated in this paper. It could be found that the degradation in capacitance is dependent on injected charges (Q_{inj}). The correlation between the carrier injection and the relative-capacitance variation of La_2O_3 MIM capacitors is also evaluated. The improvement in voltage nonlinearity of La_2O_3 MIM capacitors during CVS testing could be attributed to the stress induced traps in dielectrics. Additionally, highly stability of 10-year lifetime was achieved for a 10-nm La_2O_3 MIM capacitor with an 11.4-fF/μm^2 capacitance density.

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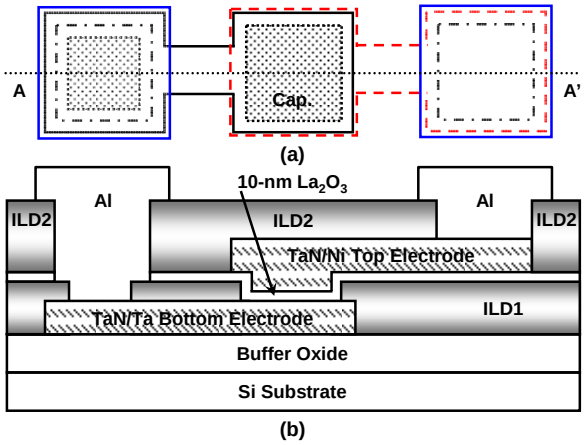

Fig. 1. The schematic layout of the La_2O_3 MIM capacitor. (b) The schematic cross section of the capacitor along the A-A' line in the layout shown in (a).

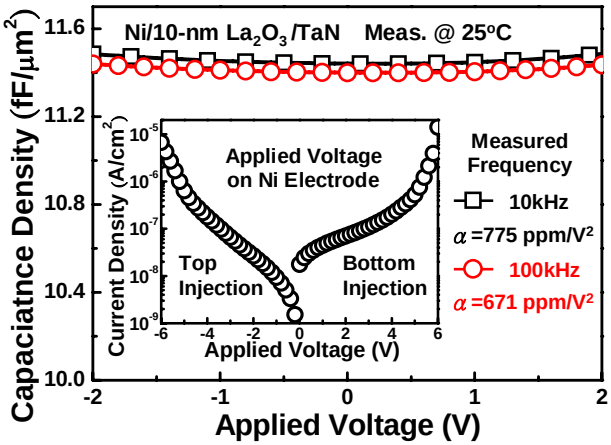

Fig. 2. The *C-V* curve, *J-V* curve, and the quadratic voltage coefficient (α) of a typical 10-nm La_2O_3 MIM capacitor.

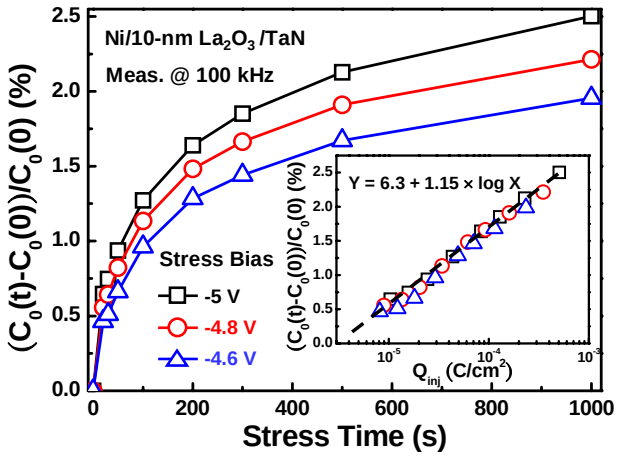

Fig. 3. Relative-capacitance variation $[C_0(t)-C_0(0)]/C_0(0)$ as a function of stress time and injection charges (Q_{inj}) at various CVS voltages from −4.6 V to −5 V.

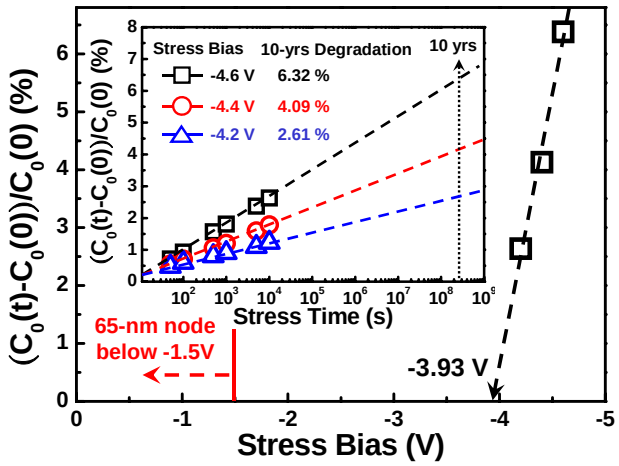

Fig. 4. The 10-year stability extraction of 10-nm La_2O_3 MIM capacitors estimated by the relative-capacitance variation.

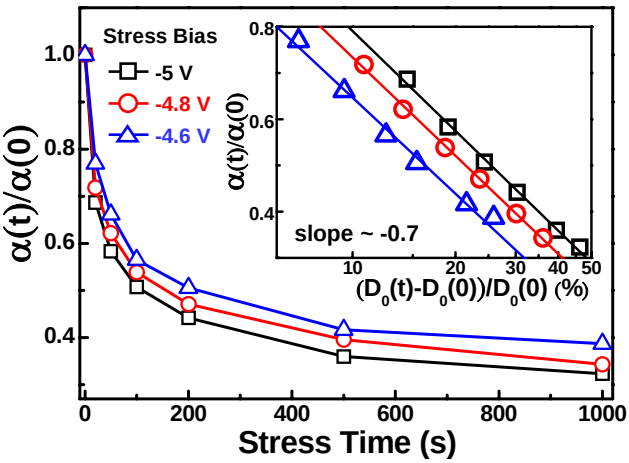

Fig. 5. Time dependence of the relative quadratic voltage coefficient of capacitance $\alpha(t)/\alpha(0)$ under a CVS of −4.6 V to −5 V.

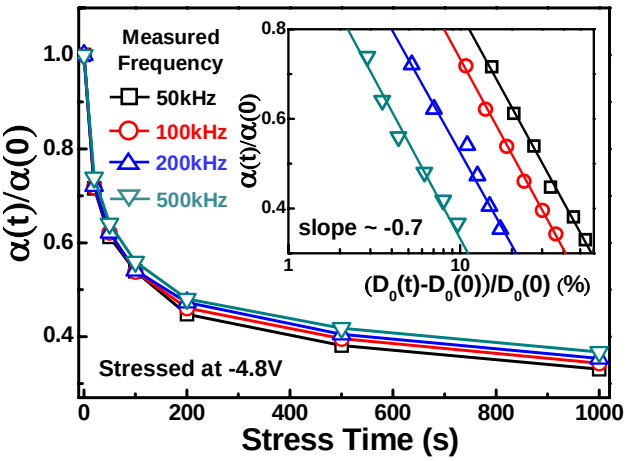

Fig. 6. Time dependence of the relative quadratic voltage coefficient of capacitance $\alpha(t)/\alpha(0)$ under a CVS voltage of −4.8 V with various measurement frequencies.