# 行政院國家科學委員會專題研究計畫 成果報告

## 先進製程技術之設計與可靠度提昇研究--子計畫三：在後佈局與測試設計所使用之良率改善技術研究(3/3)
## 研究成果報告(完整版)

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計畫參與人員： 此計畫無其他參與人員

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# National Science Council Funded Research Report On Increasing Design Reliability in Advanced Manufacturing Technology

Subproject 3: Yield Improvement Methodologies in Post-Layout Design Flow and Design for Test (3/3)

NSC 97-2220-E-009-004-
August 1, 2008 - July 31, 2009
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***Abstract*— This report is to present some results of the project funded by National Science Council in 2008 school year. Our objectives in this final year are to continue to explore and find new techniques in increasing circuit reliability due to advanced technology manufacturing variations. As the technology scales down to nanometer, the yield degradation caused by inter-die variations is getting worse. Using adaptive body bias is an effective method to mitigate the yield degradation (especially for memory compiler generated SRAMs), however we need to know a die having high threshold voltage or low threshold voltage (also called process corner) in order to use this technique. Unfortunately, it is hard to detect the process corners when PMOS and NMOS variations are uncorrelated. In this project, we propose some improved circuits of delay monitor and leakage monitor for both PMOS and NMOS process corner detection, which are uncorrelated in inter-die variations. The experimental results show that our circuits can clearly distinguish each process corner of PMOS and NMOS, thus improve the yield by adopting correct body bias. This report is from the publication of MTDT 2009.**

## I. Introduction

As the technology scales down to nanometer, the device parameters, such as gate length and oxide thickness, suffer from significant variations. If we do not consider the process variations in design stage, the real yield of the design will be far away from our expectation. In each kind of process variations, the threshold voltage mismatch is one of the most important issues. The threshold voltage variations caused by random dopant fluctuation (RDF) is inversely proportional to gate area [1], thereby the probability of device mismatch increases greatly. This is especially obvious in SRAM since SRAM cell always uses the smallest manufacturing device size [2] to ensure having high density.

In [3], it is assumed that PMOS and NMOS are correlated in threshold voltage mismatch in process variations. However when PMOS and NMOS variations are uncorrelated, it is hard to detect the process corner. The reason is that when detecting the process corner of PMOS, the results will be interfered by NMOS variations, which makes the detection fail. Hence we need an improved circuit to be able to detect PMOS and NMOS variations individually.

Memory is commonly used in various kinds of ICs. When designers design a digital circuit, memory compiler is a popular tool to provide the designers SRAM so as to integrate memory circuit with their digital circuits. In order to guarantee good yield, a memory compiler should be able to provide the components with the tolerance to high process variations. In this project, our purpose is to make the circuits generated from memory compiler immune from process variations. Our main contributions are as follows:

- We propose some improved circuits for delay monitor and leakage monitor in [3] to detect both PMOS and NMOS variations. Based on the detection results, we apply global body bias to both PMOS and NMOS. The goal is to mitigate the read-write fail caused by the inter-die variations.
- The experimental results show that our yield improvement is much better than the improvement using only NMOS body bias in some variations situations, and our circuits can guarantee that we always apply correct PMOS body bias.

The rest of the report is organized as follows. In Section II, we discuss how process variations decrease the yield and review some previous works about how to eliminate the effect of inter-die variations. In Section III, we present our improved circuits, and Section IV shows the experimental results. We conclude our work in Section V.

## II. Preliminary

In this section, we introduce some previous works in using adaptive body bias to reduce the effect of process variations, and describe our problem.

### A. Previous Works

In order to reduce the effect of process variations in SRAM architectures, many methods have been proposed. Some new SRAM cell architectures are presented in [4] [5]. Moreover, typical 6-T SRAM cell architecture uses additional circuits to enhance the yield, such as using adaptive body bias [6] [3] [7]. Since the memory compiler uses typical 6-T SRAM cell, we focus on adaptive body bias solution. By the results of [6], we can see that adaptive body bias is an effective method to improve SRAM yield. In order to apply this technique, we need circuits to detect the process corners, which is to know a die having high or low threshold voltage. In [6] [3] [7], the authors use leakage monitor and delay monitor to detect the corners. In [8] the authors propose a method using delay and slew-rate monitor to detect the process corner. Below we briefly describe adaptive body bias technique, leakage and delay monitors.

*1) Adaptive Body Bias:* The principle of adaptive body bias is that when we know that a die belongs to high threshold voltage, we can provide this die with forward body bias to decrease the threshold voltage. Similarly, when we know that a die belongs to low threshold voltage, we can provide this die with reverse body bias to increase the threshold voltage. Using this technique we can make every die tend to have normal threshold voltage, and improve the yield. This method was used to improve the yield of logic design [9]. The authors of [6] use this method to improve SRAM yield for the first time.

*2) Leakage Monitor:* [3] uses a current sensor circuit to monitor the leakage of SRAM array and generate a voltage to the comparator (the circuits referred to [3]). Then the comparator circuits compare this voltage with two reference voltages. These two reference voltages represent a die at high threshold corner and low threshold corner respectively. According to this result, we can make sure that this die belongs to high or low threshold, and the body bias selection circuit will apply correct body bias to the SRAM array. Besides, a large PMOS switch bypasses the leakage monitor at normal mode operation.

*3) Delay Monitor:* Another way to know a die with high or low threshold voltage is to use delay monitor[3] [7]. The delay monitor circuits (referred to [3]) are composed of a 600-stage long inverter chain, a counter circuit, and the comparator circuits. At first, a calibrate signal passed through the long inverter chain enables the counter. Then the counter is disabled when calibrate signal comes out the inverter chain. The comparator circuits are used to compare with two references which are represented as low threshold corner and high threshold corner. The body bias selection circuits will apply the proper body bias to SRAM array according to the result of comparator.

### B. Problem Description

In real manufacturing flow, the lithography parameters cause the PMOS and NMOS having correlated inter-die shift. It means that both PMOS and NMOS move to high or low threshold voltage. Other sources, such as global variations of doping density, may cause uncorrelated threshold voltage shift [7]. Therefore it is necessary to detect the process corner of PMOS and NMOS variations individually. Since previous works assumed that PMOS and NMOS variations are correlated, which may not be completely correct, we try to develop different circuits to detect the variations of PMOS and NMOS individually.

TABLE I

THE REQUIRED CLOCK CYCLES AT DIFFERENT INTER-DIE VARIATIONS USING THE CIRCUIT IN [3].

| 125-125 | PMOS / NMOS | HVT | NVT | LVT |
|---|---|---|---|---|
| | HVT | 15 | 13 | ♣11 |
| | NVT | ♠13 | 11 | ♢9 |
| | LVT | ♣11 | 9 | 8 |
| 150-150 | PMOS / NMOS | HVT | NVT | LVT |
| | HVT | 17 | 13 | ♣11 |
| | NVT | 14 | 11 | ♢9 |
| | LVT | ♣12 | 9 | 8 |
| 175-175 | PMOS / NMOS | HVT | NVT | LVT |
| | HVT | 18 | 14 | ♣11 |
| | NVT | ♠15 | 11 | ♢9 |
| | LVT | ♣12 | 9 | 8 |

## III. IMPROVED CIRCUITS FOR PMOS AND NMOS PROCESS CORNERS DETECTION

In this section we first present the results of using the circuits in [3] to detect the process corner when PMOS and NMOS variations are uncorrelated. Then we discuss our improved circuits of leakage monitor and delay monitor to further distinguish those variations.

### A. Delay Monitor for PMOS and NMOS Variations

Table I shows the variations results of the circuits in [3], it is clear that the PMOS and NMOS variations are not always correlated. We assume that the die suffers from both inter-die and intra-die variations: the intra-die variations have 75mv at 3-sigma and the distribution is random (based on [10]); the inter-die variations are given from 125mv to 175mv. In Table I, the first column shows the inter-die variations of PMOS and NMOS. Other columns with HVT, NVT, LVT stand for high threshold voltage, normal threshold voltage, and low threshold voltage respectively. The numerical values in the last 3 columns present the required clock numbers.

Based on [3], we may set the high threshold corner at 13 cycles and the low threshold corner at 10 cycles. We observe that when PMOS has high threshold voltage and NMOS has low threshold voltage (or PMOS has low threshold voltage and NMOS has high threshold voltage), the traditional delay monitor will be under the impression that this die has normal

threshold voltage and suggest the NMOS zero body bias. We indicate this situation with symbol ♣ in Table I. Another error will happen when PMOS has high threshold voltage and NMOS has normal threshold voltage. In this case, the circuits will be under the impression that the NMOS has high threshold voltage and suggest NMOS forward body bias, in result we get the wrong body bias. This situation is indicated with symbol ♠. The last kind of error happens when PMOS has low threshold voltage and NMOS has normal threshold voltage. In this case the circuits will be under the impression that the NMOS has low threshold voltage and suggest the reverse body bias. We indicate this situation with symbol ♢.

Based on the previous discussion, we know that if we do not concern the PMOS variations, using delay monitor may make mistakes and the probability of making this mistake is nearly 50%. Moreover, it may cause the yield worse than that without body bias in some cases. Therefore, it is necessary to concern the effect of both PMOS and NMOS variations. Below we present the detection by delay and leakage monitors.

If we want to detect the process corner of PMOS, we must remove the effect of NMOS variations. In order to achieve this, we let the PMOS and NMOS mismatch, that is, the size of PMOS are 100nm/90nm and NMOS are 110nm/90nm. Here we let PMOS have less driver ability. The delay will be dominated by PMOS thus degrading the effect of NMOS. We do not use 1V supply voltage, but use 0.7V in order to differentiate the PMOS driver ability from NMOS driver ability. Furthermore, we do not use the normal body bias, but apply forward body bias to NMOS, and apply reverse body bias to PMOS of detect circuit at detecting stage.

Table II shows the results when we use our circuits to detect PMOS inter-die variations. We set the PMOS high threshold corner at 17 and low threshold corner at 9. The results show that we can separate each kind of PMOS variations. Here 'OK' in Table II and following tables means the required cycle number is larger than 24.

Now we have already detected PMOS variations, the next stage is to detect the process corner of NMOS. In this stage, we can not change the size of inverters since the inverter size has been determined in previous stage. In previous section, we know that our MOS sizes are chosen for easily detecting PMOS variations. Here we want only NMOS variations to change delay time, we must correct the body bias of both PMOS and NMOS. We apply reverse body bias to NMOS and apply forward body bias to PMOS. The result shows in columns 3 to 5 in Table III, which indicates that our initial method is not good enough. The main problem is that the delay time is too short when PMOS has low threshold voltage. In other words, PMOS variations still affect the delay time hence the detection of NMOS variations will fail. We need a new set of improved circuits to have better detections.

Since PMOS variations still affect the delay time, we observe that if we change the initial value of counter in delay monitor, the results will be different. In order to accomplish this, we delay the enable signal of the counter circuit and show the block diagram in Fig. 1. If we have normal threshold PMOS, we let the enable signal delay 1 cycle to reach the counter circuit. If we have low threshold PMOS, we will delay 5 cycles. The modified results are shown in Table III from columns 7 to 9. Now we can know the process corner of NMOS by detecting the delay time. If the delay is more than 15 cycles, the NMOS belongs to high threshold NMOS. Similarly if the delay time is less than 11 cycles, the NMOS belongs to low threshold NMOS, and others belong to normal threshold NMOS.

In summary, our circuits are different from traditional delay monitor in the following features. First, we make the inverter MOS mismatch to let the PMOS dominate the delay time. Second, we apply body bias for detect circuit at detecting stage to have successful detections. Third, we add a delay switch circuit to remove PMOS variations when NMOS variations are detected.

TABLE II

THE RESULTS OF DETECTING PMOS INTER-DIE VARIATIONS. IN THIS TABLE WE CAN SEE THAT EACH KIND OF PMOS VARIATIONS(HVT, NVT, AND LVT) ARE SEPARATED.

| 125-125 | PMOS / NMOS | HVT | NVT | LVT |
|---|---|---|---|---|
| | HVT | OK | 13 | 8 |
| | NVT | 17 | 10 | 6 |
| | LVT | OK | 9 | 5 |
| 150-150 | PMOS / NMOS | HVT | NVT | LVT |
| | HVT | OK | 14 | 8 |
| | NVT | 21 | 10 | 6 |
| | LVT | OK | 9 | 5 |
| 175-175 | PMOS / NMOS | HVT | NVT | LVT |
| | HVT | OK | 15 | 8 |
| | NVT | OK | 10 | 6 |
| | LVT | OK | 9 | 5 |

TABLE III

THE RESULTS OF DETECTING NMOS VARIATIONS. WE CAN SEE THAT THE DELAY TIME IS AFFECTED BY PMOS VARIATIONS, HENCE WE CAN NOT DISTINGUISH NMOS VARIATIONS.

| 125-125 | PMOS / NMOS | HVT | NVT | LVT | | HVT | NVT | LVT |
|---|---|---|---|---|---|---|---|---|
| | HVT | 15 | 15 | 11 | | 15 | 16 | 16 |
| | NVT | 12 | 11 | 8 | | 12 | 12 | 13 |
| | LVT | 10 | 9 | 6 | | 10 | 10 | 11 |
| 150-150 | PMOS / NMOS | HVT | NVT | LVT | | HVT | NVT | LVT |
| | HVT | 18 | 16 | 11 | | 18 | 17 | 16 |
| | NVT | 13 | 11 | 7 | | 13 | 12 | 12 |
| | LVT | 10 | 9 | 6 | | 10 | 10 | 11 |
| 175-175 | PMOS / NMOS | HVT | NVT | LVT | | HVT | NVT | LVT |
| | HVT | 20 | 16 | 10 | | 20 | 17 | 15 |
| | NVT | 14 | 11 | 7 | | 14 | 12 | 12 |
| | LVT | 11 | 8 | 5 | | 11 | 9 | 10 |

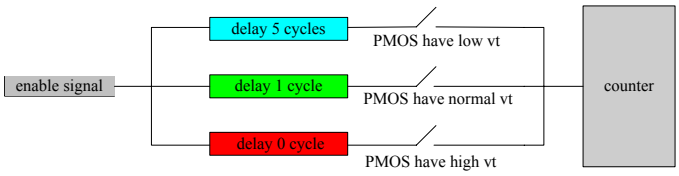


Fig. 1. Modified circuit block diagram for detecting NMOS variations. This circuit can eliminate the effect of PMOS variations when detecting the process corner of NMOS.

### *B. Leakage Monitor for PMOS and NMOS Variations*

Similar to delay monitor, if we use traditional circuits to detect the variations without considering PMOS variations, the errors will occur. The following subsections will present our modified leakage monitor circuits.

*1) Inverter Array:* Here we do some modification to the leakage monitor in [3]. We replace leakage source from the SRAM array to an inverter array. The reasons are as follows. First, we use inverter array to be the test circuit, then bypass PMOS is no longer needed. Second, we can give a value we need but not limit on 0V or 1V to the input signal of inverter. We also change the loading circuits of current mirror since we want our modified circuits be able to detect NMOS and PMOS individually. Finally, we will add body bias on current mirror circuits when we detect NMOS variations.

*2) PMOS Variations Detector Using Leakage Monitor:* Similar to delay monitor, we detect the PMOS variations first. From our experiments we find that NMOS variations affect the output, and the reason is the active NMOS loading, therefore the detection of PMOS variations fail. We modify the loading of the current mirror, and the circuit is shown in Fig. 2(a). We cascade three NMOS devices and connect their gate with a metal line to make them have the same gate voltage. The output is taken out by net1, and the result is shown in Table IV. The numerical values in the last 3 columns express the output voltage of current mirror. We can see that cascade three NMOSs remove the effect of active load NMOS variations.

*3) NMOS Variations Detector Using Leakage Monitor:* Here we need to detect the NMOS variations, and we only use normal current mirror. In order to remove the influence of PMOS (two PMOS current mirror drivers, MP1 and MP2), we give adaptive body bias to PMOS driver based on the results of the first stage. The circuit is shown in Fig. 2(b), and the result is shown in Table V.

## IV. Experimental Results

We implement our circuits in HSPICE, and use memory compiler from FARADAY to generate single port SRAM as our test circuits. We use the UMC 90nm CMOS library to implement our circuits. We use memory compiler to compile a 64-word (each word has 32 bits) single port SRAM. Monte-Carlo method is used to test the failure probability. We choose

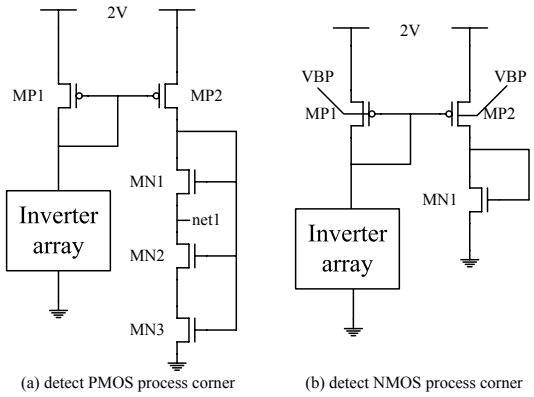


Fig. 2. Process corner detection in improved leakage monitor. (a)We replace the active NMOS loading with cascade three NMOS devices when detecting PMOS variations.(b)We apply body bias to the two PMOS drivers when detecting the process corner of NMOS.

TABLE IV

The results of modified circuits detecting PMOS variations. The high threshold process corner of PMOS can be set at 0.3V and the low one can be set at 0.45V. Each kind of PMOS variations are separated.

| 125-125 | PMOS / NMOS | HVT | NVT | LVT |
|---|---|---|---|---|
| | HVT | 0.2107 | 0.426 | 0.532 |
| | NVT | 0.2258 | 0.4196 | 0.5261 |
| | LVT | 0.2177 | 0.4022 | 0.5126 |
| 125-200 | PMOS / NMOS | HVT | NVT | LVT |
| | HVT | 0.2215 | 0.4281 | 0.5352 |
| | NVT | 0.2258 | 0.4196 | 0.5261 |
| | LVT | 0.214 | 0.3933 | 0.5040 |
| 200-125 | PMOS / NMOS | HVT | NVT | LVT |
| | HVT | 0.1367 | 0.4265 | 0.5631 |
| | NVT | 0.1458 | 0.4196 | 0.5586 |
| | LVT | 0.1367 | 0.4022 | 0.5457 |

TABLE V

The results of our circuits to detect NMOS variations. Each kind of NMOS variations are separated.

| 125-125 | PMOS / NMOS | HVT | NVT | LVT |
|---|---|---|---|---|
| | HVT | 0.5336 | 0.4530 | 0.4820 |
| | NVT | 0.4160 | 0.3316 | 0.36 |
| | LVT | 0.2892 | 0.2154 | 0.2440 |
| 125-200 | PMOS / NMOS | HVT | NVT | LVT |
| | HVT | 0.6142 | 0.5314 | 0.5608 |
| | NVT | 0.4160 | 0.3316 | 0.36 |
| | LVT | 0.2303 | 0.1465 | 0.1752 |
| 200-125 | PMOS / NMOS | HVT | NVT | LVT |
| | HVT | 0.4916 | 0.4530 | 0.5271 |
| | NVT | 0.3742 | 0.3316 | 0.4032 |
| | LVT | 0.2576 | 0.2154 | 0.2865 |

TABLE VI

TOTAL FAILURE NUMBER OF THE SINGLE PORT SRAM WITH 125MV ASSUMPTION FOR INTER-DIE VARIATIONS AND 75MV ASSUMPTION FOR INTRA-DIE VARIATIONS. THIS SHOWS THAT WE CAN GET MUCH LESS MISTAKES AND OUR APPROACH OUTPERFORMS THE TECHNIQUE APPLYING ONLY NMOS BODY BIAS.

| 125mv | Without body bias | | Only NMOS body bias | | [3] | | Ours | |
|---|---|---|---|---|---|---|---|---|
| PMOS-NMOS | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| high– high | 25 | 108 | 2 | 1 | 2 | 1 | 2 | 0 |
| high– zero | 3 | 0 | 3 | 0 | 4 | 0 | 0 | 0 |
| high– low | 14 | 9 | 9 | 0 | 14 | 9 | 6 | 0 |
| zero– high | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| zero– low | 4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| low – high | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| low – zero | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| low – low | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

640 cells per circuit as our test samples, and the results are shown in Table VI and VII.

In Table VI, each test circuit suffers from both inter-die and intra-die variations. The inter-die variations are set at 125mv and the intra-die variations are set at 75mv. The first column presents the process corner of PMOS and NMOS respectively. The second column presents the original circuits without using body bias. The sub-columns 0 and 1 represent the action of "write 0 then read the data out" and "write 1 then read it out" respectively. Other numerical values represent the failure numbers in 640 times test. The third column shows that we only use NMOS body bias and we assume that all predictions are correct. The fourth column presents the result of using the circuits in [3]. And the final column presents the results of using our proposed circuits. We can see that our improved circuits will always get the right prediction, and our yield improvement will be better than the technique applying only NMOS body bias.

In Table VII, all experimental setups are the same as in Table VI except for the 150mv assumption for inter-die variations. We can see that when PMOS and NMOS both have high threshold, the yield is degraded, and using only NMOS body bias can not satisfy the requirement of yield improvement. The yield improvement of using both PMOS and NMOS body bias is obvious in this table.

## V. CONCLUSION

In this project, we have proposed some improved circuits of delay monitor and leakage monitor in process corner detection. These circuits can correctly detect both PMOS and NMOS variations, and improve the yield by decreasing the influence of inter-die variations. All of our test circuits are generated from a widely used memory compiler. The experimental results show that some situations can not improve yield by using only NMOS body bias, but using both PMOS and NMOS body bias can improve the yield significantly. Besides, the results

TABLE VII

TOTAL FAILURE NUMBER OF THE SINGLE PORT SRAM WITH 150MV ASSUMPTION FOR INTER-DIE VARIATIONS AND 75MV ASSUMPTION FOR INTRA-DIE VARIATIONS.

| 150mv | Without body bias | | Only NMOS body bias | | [3] | | Ours | |
|---|---|---|---|---|---|---|---|---|
| PMOS-NMOS | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| high– high | 45 | 508 | 38 | 432 | 38 | 432 | 31 | 97 |
| high– zero | 7 | 0 | 7 | 0 | 13 | 0 | 1 | 0 |
| high– low | 24 | 28 | 19 | 10 | 24 | 28 | 14 | 5 |
| zero– high | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| zero– low | 6 | 1 | 2 | 0 | 2 | 0 | 2 | 0 |
| low – high | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| low – zero | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| low – low | 4 | 0 | 2 | 0 | 2 | 0 | 4 | 0 |

also show that our proposed circuits can almost get the right predictions of variations. Even we get wrong prediction of NMOS, our yield can still be improved by adapting correct PMOS body bias.

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# 行政院國家科學委員會補助國內專家學者出席國際學術會議報告

2009 年 10 月 31 日

附件三

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|---|---|---|---|
| 時間<br>會議<br>地點 | January 19-22, 2009<br>Yokohama, Japan | 本會核定<br>補助文號 | 計畫編號 97-2220-E-009-004 |
| 會議名稱 | 2009 IEEE/ACM Asia and South Pacific Design Automation Conference (ASP-DAC) | | |

一、參與會議經過：

2009 ASP-DAC was held in Yokohama, Japan. There are three Keynote speeches, including the one given by Dr. Leon Stok, who is IBM’s EDA director and past DAC chair. I have attended several important sessions, including the one which I am very impressive: Challenges in 3D integrated circuit design. The invited talks show the most recent trends in this research topic, and it helps me a lot in writing the proposals to NSC. Other presentations are also fairly good, I have learned a lot during the attendance.

二、與會心得

I am the Technical Program Committee for this year, and I will be the Organizing Committee of this conference next year, I have observed many things to be helpful for the next conference held in Taiwan in 2010. I sincerely hope we can do better next year.

三、建議

3D IC is one of most promising research fields in the near future, we hope we can learn more from this conference and other related conferences so that we can be one of the top research teams in the country.

四、攜回資料名稱及內容:

攜回一論文集

五、其他

N/A