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計畫類別: ☑ **個別型計畫** ☐ **整合型計畫**
計畫編號: NSC-89-2213-E009-047
執行期間: 88 **年** 7 **月** 1 **日** **至** 89 **年** 7 **月** 31 **日**

計畫主持人: **張翼**
共同主持人:

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中華民國 89 **年** 10 **月** 26 **日**

The development of 2.4V GaAs power PHEMT for wireless communication application

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主持人: **張翼 國立交通大學材料科學與工程研究所**
計畫參與人員: **陳仕鴻 曾孟修 顧成芳 國立交通大學材料科學與工程研究所**

中文摘要

具有高效率、高線性度之個人無線通訊用 2.4 **伏特操作雙δ摻雜砷化鋁鎵/砷化銦鎵/砷化鎵假晶式高電子遷移率電晶體** (PHEMT)**已研發完成。 閘極寬** 20.16 mm **之元件，在** 2.4 **伏特汲極電壓與** 1.9 GHz **頻率操作下，其輸出功率可達** 30 dBm**，並具有超過** 60 %**之功率增加效率。在** 2.4 **伏特汲極低電壓下，元件仍具有高效率，乃因使用具有高汲極電流與高電子遷移之雙δ摻雜假晶式高電子遷移率電晶體結構，另外，並縮減元件之尺寸，以降低膝電壓與減小源極電阻，使元件更適用於低電壓操作。**
關鍵詞:線性度; 砷化鋁鎵; 假晶高遷移率電晶體

Abstract
A 2.4-V operation dual delta doped AlGaAs/ InGaAs/GaAs pseudomorphic high electron mobility transistor (PHEMT) with high efficiency and high linearity for personal communications has been developed. The 20.16 mm gate width device operating at a drain bias of 2.4 V at 1.9 GHz gives an output power of 30.0 dBm and a power added efficiency over 60%. The high efficiency at 2.4 V bias is attributed to the dual delta doped PHEMT structure which has high drain current and high electron mobility and to the shrinkage of the device layout which results in the low knee voltage and low source resistance of the device.

I. INTRODUCTION

Power amplifier is one of the key component for wireless communication systems. In recent years, high performance power GaAs devices including heterojunction bipolar transistors (HBT's) [1-3], enhancement-mode high electron mobility transistors (HEMT's) [4-6] for low voltage devices application[7-10] is popular topic for wireless communication. Advanced high performance wireless communication systems require high efficiency, high linearity power transistors operating at low supply voltage. The advantages of low voltage operation include reducing power consumption of the circuits, decreasing the number of the battery cells used and the reduction of the size and weight of the system. In this study, a low voltage 1-watt device is developed. Dual delta doped AlGaAs/InGaAs/GaAs PHEMT structure is used in this study, this is because dual delta doped PHEMT has high current capability and high electron mobility. The device developed a width of 20.16 mm device with reduction in the device layout. The reduction in the device layout results in low knee voltage and low source resistance for the device and results in excellent efficiency for the device at low voltage application.

II. DEVICE LAYOUT AND FABRICATION

3-inch (1 0 0) oriented semi-insulating GaAs epitaxial wafer was used for device fabrication. The Epitaxial layer was grown by the Molecular Beam Epitaxy (MBE) technique. The structure of the dual delta doped AlGaAs/InGaAs/GaAs PHEMT is shown in Fig. 1. The active part was 85 Å InGaAs channel layer sandwiched between an upper 35Å undoped AlGaAs layer and a lower 40Å undoped GaAs layer. The two dimensional electron gas (2-DEG) was formed in the pseudomorphic InGaAs channel by electron transfer from silicon delta doping above and below the InGaAs layer. A heavily Si-doped GaAs cap was formed to provide the good ohmic contacts and reduce the source resistance. The fabricated device had a total gate width of 20.16 mm width with each finger 120 μm in length. The drain to source spacing is 4 μm and the gate length is 0.5 μm. The device covers 1665 x 350 μm^2 area, which is quite

compact compared to regular power device layout. Fig. 2 is the optical photograph of a finished device. The device isolation was accomplished by wet etching using HF based solution. The ohmic metal, Au/Ge/Ni was deposited by electron-beam evaporation followed by rapid thermal annealing at 300°C for 10 seconds. Gate was formed by Ti/Pt/Au metal. PECVD (Plasma Enhanced Chemical Vapor Deposition) silicon nitride was used for the device passivation. Gold plated airbridges were used for interconnections of the 20.16 mm width PHEMT's. Finally, the device was thinned to 5 mil and metallized with backside gold plating. to improve the device performance.

III. DEVICE PERFORMANCE

The device developed has a saturation current of 6A. The pinch off voltage of the device is around -1.1 V. The maximum transconductance of this device is 340 mS/mm. The breakdown voltage of this device is 12V. Fig. 3 is the I-V characteristics of the device with gate bias from –0.7 V to pinch off. The high current density and high transconductance of this device is due to the dual delta doped HEMT structure.

Power performance of this device was measured at 1.9 GHz and with a drain bias of 2.4 V. The device was operated under class AB condition with a bias drain current of 400 mA. The power characteristics were measured by a power tuning system, in which the input and output tuners with variable capacitors and inductors were used to provide the conjugate matched input and load impedances for the optimum power performance. Fig. 4 shows the output power, power added efficiency and power gain as a function of the input power for the 20.16 mm wide device. For the 20.16 mm device, the maximum power under 2.4 V bias condition, the maximum output power is 30 dBm and the power added efficiency of this device at the maximum output power is 61.5%. The gain of this device at maximum output power is 8.47 dB. The linear gain was 11.56 dB and the output power at 1 dB compression was 28.12 dBm with a power-added efficiency of 47.5%. The PHEMT with high efficiency, high linearity and high output power is suitable for low voltage wireless communication applications.

IV. CONCLUSIONS

A 2.4 V low voltage application power HEMT was developed. The device has a double delta doped AlGaAs/InGaAs/GaAs structure to provide high drain current density and high transconductance. The size of the layout of this device was reduced to improve the knee voltage and source resistance for low voltage applications. The device developed shows an output power of 30 dBm with a power added efficiency of 61.5% and the gain of the device at the maximum output power is 8.47 dB. The device developed should be applicable to next generation wireless communication systems.

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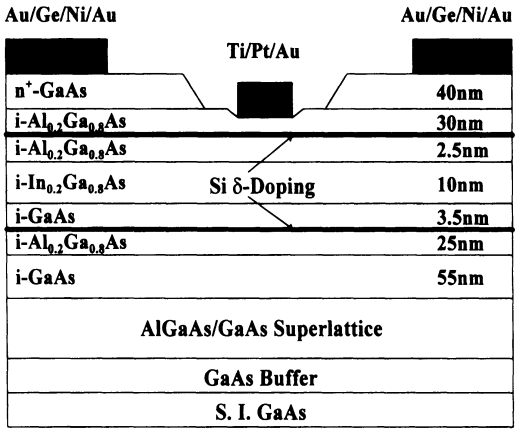

Fig. 1 Structure of the δ-doped AlGaAs/InGaAs power PHEMT.

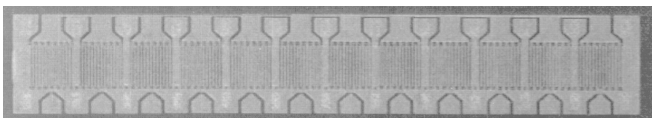

Fig. 2 The top view of the 20.16-mm-wide power PHEMT manufactured.

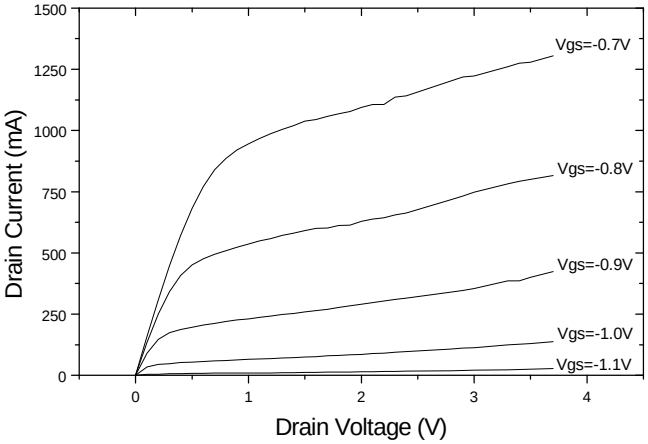

Fig. 3 The current-voltage characteristics of the 20.16-mm-wide power PHEMT with gate bias from –0.7 V to pinch off.

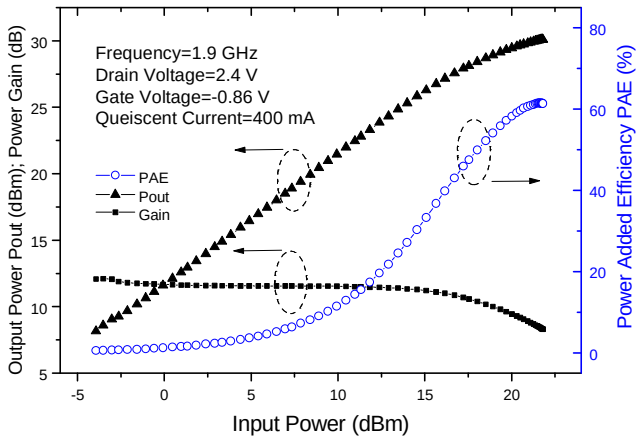

Fig. 4 Output power, power added efficiency and power gain as a function of input power for the 20.16-mm GaAs power PHEMT.