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Geometry-Scalable Parasitic Deembedding Methodology for On-Wafer Microwave Characterization of MOSFETs

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***Abstract*—This paper presents a geometry-scalable parasitic deembedding technique for on-wafer S-parameter measurements of silicon MOSFETs. The proposed methodology is based on the transmission-line theory and the cascade and parallel combinations of two-port networks. We use only one "reflect" and one "thru" dummy structure on a wafer to remove the feeding networks with arbitrary geometry surrounding the MOS transistors. The shielding technique is employed to improve the substrate isolation and fixture scalability. To mitigate the parasitic effects of the dangling leg between the MOSFET and the ground plane, microstriplike interconnects are introduced to mount the devices. Full-wave electromagnetic simulations were also accomplished to substantiate the interconnect scalability and network combinations. The MOS transistors and deembedding dummy patterns were implemented in a 0.13-μm standard CMOS technology and characterized up to 30 GHz. Compared with the conventional deembedding methods, the proposed approach consumes less than 33% of chip area and characterization time for modeling test keys, while still maintaining high accuracy.**

***Index Terms*—Deembedding, microwave measurements, modeling, MOSFETs, parasitics.**

I. Introduction

THE DESIGN of silicon-based radio-frequency integrated circuits (RFICs) and monolithic microwave integrated circuits requires reliable process technology and foundry design kits. Device modeling and parasitic extraction are significant issues for circuit design to minimize the failures and frequency shifts. Since reliable RF models call for accurate wafer-level microwave characterization of active and passive components, testing methodologies and modeling test keys should be carefully developed to evaluate the intrinsic device characteristics. One such measuring technique is parasitic deembedding, which provides the consistent removal of the unwanted parasitic elements of the on-wafer test fixture.

To extract the intrinsic device parameters from microwave measurements, much research effort has been focused on this particular subject. van Wijnen *et al.* [1] first reported the open deembedding method to remove the admittances of the probe pads using an open dummy structure. Koolen *et al.* [2] showed that the open-short deembedding procedure using one open and one short dummy pattern could be used to further subtract the impedances of the probe pads and interconnects. Although many other deembedding techniques for parasitic subtraction have been developed, the open-short deembedding is still the current industry standard due to its simplicity and accuracy [3]–[6]. The aforementioned deembedding methods utilize lumped equivalent circuits to model the feeding networks of the test fixtures in series–shunt configurations. However, as the device is operated at microwave frequencies and/or the interconnect length is considerable, the lumped-circuit assumption would become invalid because of the distributed nature of the test structures. In an attempt to solve this issue, Chen and Deen suggested that the deembedding method based on cascade configuration could be used to eliminate the parasitic effects without any lumped-circuit representation [7]. Moreover, a flexible cascade-based deembedding was also developed to reduce the consumption of chip area [8].

Although much work has been done to date, most research has focused on the accuracy of the parasitic estimation and correction [9]. The purpose of this investigation was to propose a systematic parasitic deembedding procedure to minimize the chip area and characterization time in a mass-production line. With the utilization of the shielding technique, the suggested reflect and thru dummy structures can be used to calculate the parasitics of probe pads and the transmission-line parameters of interconnects, respectively [10]. Based on the transmission-line theory and microwave network analysis, the proposed method can generate the parasitics of feeding networks with arbitrary geometry to efficiently and accurately deembed the parasitic effects of the fixtured MOS transistors with various gate dimensions and multiplier factors. To validate this geometry-scalable deembedding theory, MOS transistors and deembedding structures were fabricated using a UMC 0.13-μm CMOS process, and full-wave electromagnetic (EM) simulations were carried out.

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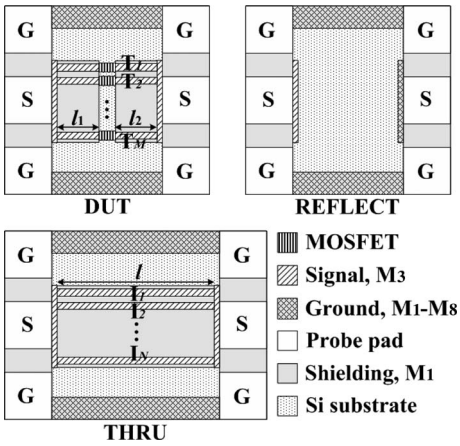

Fig. 1. Illustration of the on-wafer MOSFET test structure and corresponding dummy structures for proposed geometry-scalable deembedding method.

II. Geometry-Scalable Deembedding Theory

A. On-Wafer Test Fixtures

Fig. 1 shows the on-wafer test fixtures, which contain a device-under-test (DUT) and its corresponding dummy structures, for the proposed deembedding theory. The design of RF test keys for global device modeling must cover the complete physical device dimensions, such as channel length, channel width, finger number, multiplier factor, etc. Therefore, both single- and multitransistor $(T_1 - T_M)$ test fixtures should be employed to extract the device characteristics, multiplier effects, and proximity effects. In general, the gate and drain of the MOSFET are, respectively, connected to the input and output ports, while the source and silicon substrate are tied together to the ground reference. In our design, the source of the MOSFET is connected to the ground shield beneath the signal traces to form a microstriplike transmission line, and thus, the parasitics of the dangling leg between the transistor and the ground plane can be eliminated by simply using a two-port model [11], [12]. Here, the ground shield not only improves the substrate isolation but also provides good fixture scalability [10] and interconnect scalability [8] for the proposed method. The substrate-shielded reflect structure, which consists of a simple open at the input port and a simple short at the output port or vice versa, is used to remove the parasitics of the ground-signal-ground (GSG) pads [10]. A thru dummy with an N-conductor interconnect $(I_1 - I_N)$ is used to evaluate the transmission-line parameters for subtracting the interconnect parasitics of the M-transistor test fixtures. It should be noted that the multiconductor thru is employed, instead of a single-conductor one, to mitigate the step-discontinuity effects of the pad-to-interconnect interface [13]. Both the discontinuities, respectively, between the probe pads and the interconnection lines and between the interconnection line and the DUT have low-pass effects on the transmission characteristics. Although the step-discontinuity effects are difficult to be extracted and deembedded, they can be mitigated by using the tapered transition.

Fig. 2(a) shows the semidistributed parasitic model based on the cascade and parallel configurations for the modeling test keys. The parasitic components Y_{PAD} and Z_{PAD}, which

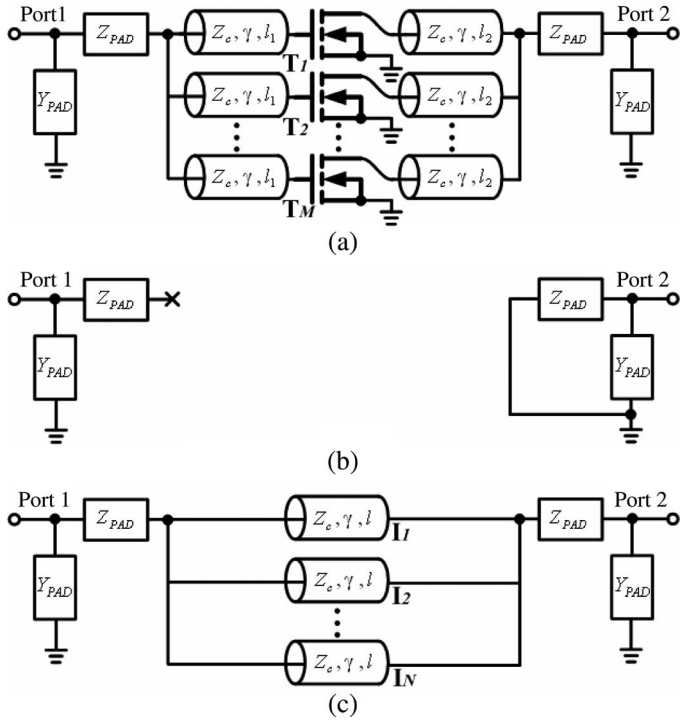

Fig. 2. Suggested parasitic models for the proposed on-wafer test structures. (a) DUT. (b) Reflect dummy structure. (c) Thru dummy structure.

can be replicated from the reflect structure in Fig. 2(b), are the shunt admittance and series impedance of the probe pads, respectively. Since, here, the shielding technique is applied, the multiconductor interconnect can be modeled as isolated transmission lines in parallel with each other. As shown in Fig. 2(c), after subtracting the probe-pad parasitics of the N-conductor thru dummy, the transmission-line parameters of a single-conductor interconnect calculated using the network analysis can be employed to estimate the parasitic effects of the interconnects with arbitrary geometry.

B. Combination of Microwave Networks

As mentioned in the previous section, both the cascade and parallel combinations of two-port networks would be utilized to establish the deembedding procedure. In this case, it is convenient to characterize the fixtured transistors using the $ABCD$-parameter representation. For the cascade connection of two two-port networks, the overall $ABCD$ matrix $[A_C]$ is equal to the product of the individual $ABCD$ matrices [14], namely

$$[A_C] = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix}. \tag{1}$$

Consequently, the embedding and deembedding of two-port networks can be accomplished by multiplying a given matrix by a matrix and by an inverse of matrix, respectively [8].

Similarly, we can have the overall $ABCD$ matrix $[A_P]$ of the two-port networks connected in parallel as follows:

$$[A_P] = \begin{bmatrix} \frac{A_1B_2+B_1A_2}{B_1+B_2} & \frac{B_1B_2}{B_1+B_2} \\ C_1 + C_2 + \frac{(A_1-A_2)(D_2-D_1)}{B_1+B_2} & \frac{D_1B_2+B_1D_2}{B_1+B_2} \end{bmatrix}. \tag{2}$$

Consider the case of multiconductor interconnects shown in Figs. 1 and 2. The input/output feeding networks are equally divided into M microstriplike transmission lines with appropriate line separation, and as a result, the overall $ABCD$ matrix of the M identical two-port networks oriented in parallel can be derived based on (2) as

$$\begin{bmatrix} A_P & B_P \\ C_P & D_P \end{bmatrix} = \begin{bmatrix} A & \frac{B}{M} \\ MC & D \end{bmatrix} \tag{3}$$

where A, B, C, and D are the $ABCD$ parameters of each single-conductor microstrip.

According to the network analysis mentioned earlier, the parasitics of the MOSFET test structures modeled in the cascade and parallel configurations can be evaluated and then deembedded.

C. Deembedding Procedure

As shown in Fig. 2, the $ABCD$ matrices of the probe-pad parasitics for ports 1 and 2 are, respectively

$$\begin{aligned}[A_{\mathrm{PAD1}}] &= \begin{bmatrix} 1 & 0 \\ Y_{\mathrm{PAD}} & 1 \end{bmatrix} \begin{bmatrix} 1 & Z_{\mathrm{PAD}} \\ 0 & 1 \end{bmatrix} \\ &= \begin{bmatrix} 1 & Z_{\mathrm{PAD}} \\ Y_{\mathrm{PAD}} & 1 + Y_{\mathrm{PAD}} Z_{\mathrm{PAD}} \end{bmatrix} \end{aligned} \tag{4}$$

$$\begin{aligned}[A_{\mathrm{PAD2}}] &= \begin{bmatrix} 1 & Z_{\mathrm{PAD}} \\ 0 & 1 \end{bmatrix} \begin{bmatrix} 1 & 0 \\ Y_{\mathrm{PAD}} & 1 \end{bmatrix} \\ &= \begin{bmatrix} 1 + Y_{\mathrm{PAD}} Z_{\mathrm{PAD}} & Z_{\mathrm{PAD}} \\ Y_{\mathrm{PAD}} & 1 \end{bmatrix}. \end{aligned} \tag{5}$$

It should be noted that $Y_{\mathrm{PAD}} = Y_{\mathrm{REFLECT},11}$ and $Z_{\mathrm{PAD}} = 1/(Y_{\mathrm{REFLECT},22} - Y_{\mathrm{REFLECT},11})$, where $[Y_{\mathrm{REFLECT}}]$ is the admittance matrix of the reflect dummy. The thru dummy can be modeled in cascade connection, and its pad parasitics can be subtracted by using $[A_{\mathrm{INT}}] = [A_{\mathrm{PAD1}}]^{-1}[A_{\mathrm{THRU}}][A_{\mathrm{PAD2}}]^{-1}$, where the superscript "-1" denotes the inverse of the matrix and $[A_{\mathrm{THRU}}]$ and $[A_{\mathrm{INT}}]$ are the $ABCD$ matrices of the thru dummy and the N-conductor interconnect without probe-pad parasitics, respectively. Accordingly, the transmission-line parameters of the N-conductor interconnect, such as characteristic impedance Z_C and propagation constant γ, can be evaluated as in [15]. Here, we have

$$[A_{\mathrm{INT}}] = \begin{bmatrix} \cosh \gamma l & Z_C \sinh \gamma l \\ \frac{1}{Z_C} \sinh \gamma l & \cosh \gamma l \end{bmatrix}. \tag{6}$$

Based on the aforementioned results, the parasitic effects of the input/output interconnects with arbitrary line length (l_1 and l_2) for an M-transistor test fixture can be efficiently calculated from the $ABCD$ matrix of an N-conductor thru, and thus

$$[A_{\mathrm{INTi}}] = \begin{bmatrix} \cosh \gamma l_i & \frac{NZ_C}{M} \sinh \gamma l_i \\ \frac{M}{NZ_C} \sinh \gamma l_i & \cosh \gamma l_i \end{bmatrix}, \qquad i = 1, 2. \tag{7}$$

The detailed procedure for S-parameter deembedding is summarized as follows.

1) Measure the S-parameters $[S_{\mathrm{DUT}}]$, $[S_{\mathrm{REFLECT}}]$, and $[S_{\mathrm{THRU}}]$ of the DUT, reflect, and thru, respectively.
2) Convert $[S_{\mathrm{REFLECT}}]$ to its admittance matrix $[Y_{\mathrm{REFLECT}}]$, and calculate the $ABCD$ matrices $[A_{\mathrm{PAD1}}]$ and $[A_{\mathrm{PAD2}}]$ of probe pads from (4) and (5).
3) Extract the intrinsic interconnect parameters using $[A_{\mathrm{INT}}] = [A_{\mathrm{PAD1}}]^{-1}[A_{\mathrm{THRU}}][A_{\mathrm{PAD2}}]^{-1}$, and calculate the characteristic impedance Z_C and propagation constant γ as in [15].
4) Calculate the $ABCD$ matrices $[A_{\mathrm{INT1}}]$ and $[A_{\mathrm{INT2}}]$ for the input/output interconnects from (7).
5) Calculate the $ABCD$ matrices $[A_{\mathrm{IN}}]$ and $[A_{\mathrm{OUT}}]$, which are, respectively, the input and output feeding networks, from $[A_{\mathrm{IN}}] = [A_{\mathrm{PAD1}}][A_{\mathrm{INT1}}]$ and $[A_{\mathrm{OUT}}] = [A_{\mathrm{INT2}}][A_{\mathrm{PAD2}}]$.
6) Convert $[S_{\mathrm{DUT}}]$ to its $ABCD$ matrix $[A_{\mathrm{DUT}}]$, and calculate the $ABCD$ matrix $[A_D]$ of the intrinsic MOSFETs using $[A_D] = [A_{\mathrm{IN}}]^{-1}[A_{\mathrm{DUT}}][A_{\mathrm{OUT}}]^{-1}$.
7) Convert $[A_D]$ to its S-parameters $[S_D]$.

III. Results and Discussion

To verify the proposed deembedding theory, MOS transistors and the corresponding deembedding structures were fabricated using a 0.13-μm eight-metal-layer CMOS process. The NMOS transistors with the dimensions of gate length $(L_g) = 0.13$ μm, gate width $(W_g) = 4$ μm, number of fingers $(N_f) = 16$, and multiplier factor $(M) = 1, 2, 4,$ and 8 were connected in a two-port GSG configuration. The multiconductor interconnects with the dimensions of line length (l_1 and l_2) $= 41$ μm, line width $(W) = 6$ μm, and line separation $(S) = 7.5$ μm were designed with the EM simulations and placed between the probe pads and transistors. The solid ground shield under the feeding networks was fabricated using the M_1 copper layer (the lowest metal layer) with thickness of 0.32 μm and electrically connected to the ground pads. The dc and RF measurements of the on-wafer test structures were performed on an Agilent 4142B Modular DC Source/Monitor and an Agilent 8510 C Vector Network Analyzer, respectively. Before starting the S-parameter measurements, the measurement system was calibrated using the line-reflect-reflect-match calibration procedure with a ceramic impedance standard substrate.

A. EM Simulations

In this section, the full-wave EM simulations based on the method of moment were performed to design the feeding networks. As shown in Fig. 3, two two-port microstrip geometries were simulated: shunt microstrips on a silicon substrate and on a ground shield. In practice, the interconnect scalability would be degraded by improper parasitic deembedding [8], and therefore, here, the interconnect length of the thru dummy was set to about 300 μm to mitigate the parasitic effects as well as save the chip area. Fig. 3(a) and (b) shows the simulated characteristic impedances as a function of frequency for unshielded and substrate-shielded shunt microstrips, respectively. The line length and line width were held constant at 300 and 6 μm, respectively, and the line separation (S) was altered from 5 to 100 μm. As the line separation increases, the impedance of the unshielded shunt microstrips becomes lower because of

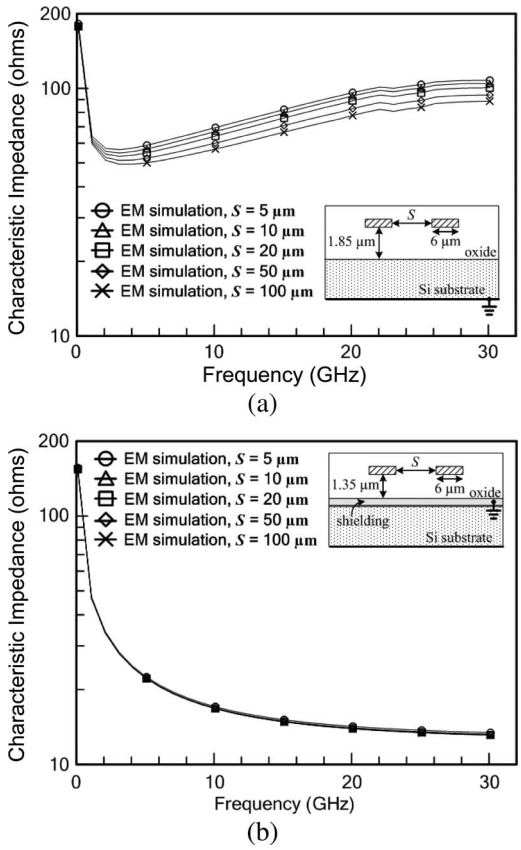

Fig. 3. EM-simulated characteristic impedance versus frequency for different guided wave structures. (a) Shunt microstrips without shielding. (b) Shunt microstrips with shielding.

the increasing of the effective line width, while the substrate-shielded ones show approximately identical impedance. We found that the parasitic effects, which come from the EM coupling between each microstrip and substrate networks, can be reduced by using the ground shielding. These results indicate that the shunt microstrips can be divided into isolated two-port networks by the use of the ground shielding and careful design of the microstrip geometry. Here, a line separation of 7.5 μm was adopted according to the transistor size and arrangement.

Based on the aforementioned findings, we can efficiently reproduce and deembed the parasitics of the shielded feeding networks with arbitrary line length and number of lines.

B. Microwave Measurements

Fig. 4 shows the layout of the fabricated modeling test keys and dummy structures for the industry-standard open-short deembedding [2] and the proposed method. In this paper, a two-conductor thru is selected to mitigate the step-discontinuity effects of the pad-to-interconnect junction and to generate the interconnect parasitics. Fig. 5 compares the characteristic impedances calculated based on (7) to that measured from the thru dummies with various numbers of lines ($N = 1, 2, 4,$ and 8). The return loss and insertion loss of the thru dummies obtained from measurements and calculations are also shown in Fig. 6 for comparison. It can be seen that the calculations match well with the measurements, and it can be proved that only

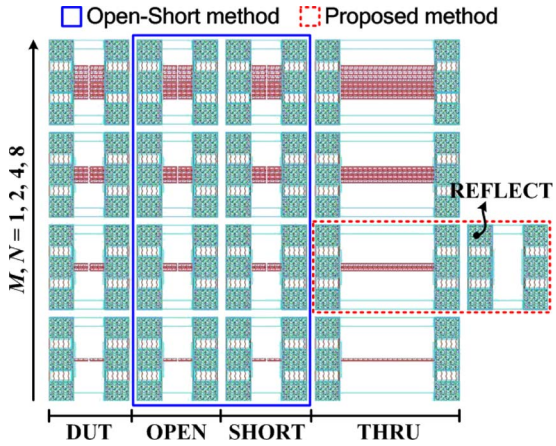

Fig. 4. Layout of the on-wafer MOSFET test structures and deembedding structures for the open-short method [2] and proposed method.

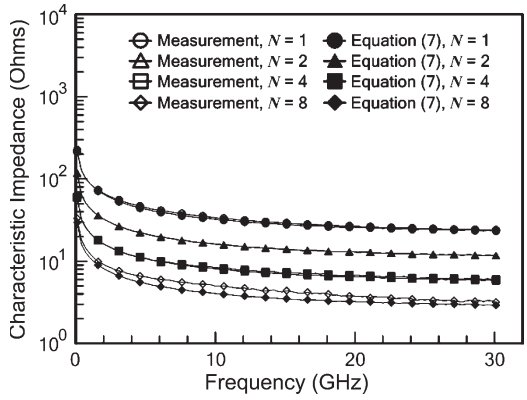

Fig. 5. Measured and calculated ($N = 2$) characteristic impedance versus frequency for thru dummy structures with different numbers of lines ($N = 1, 2, 4,$ and 8). The pad parasitics of thru dummies are removed.

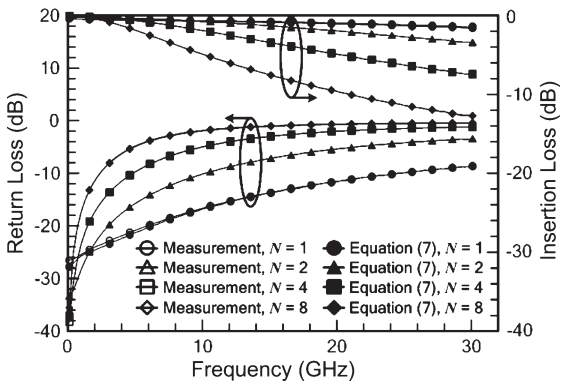

Fig. 6. Measured and calculated ($N = 2$) return loss and insertion loss versus frequency for thru dummy structures with different numbers of lines ($N = 1, 2, 4,$ and 8). The pad parasitics of thru dummies are removed.

one thru dummy would be required. Fig. 7 shows the two-port S-parameters of the MOSFET test fixtures with various multiplier factors ($M = 1, 2, 4,$ and 8) biased at $V_{GS} = 1.2$ V and $V_{DS} = 1.2$ V. These results are deembedded using the open-short method and the proposed one. As we can see, the results obtained from the two different methods are in excellent agreement over the entire frequency range. Fig. 8(a)–(f) shows some figures of merit such as voltage gain G_u, current

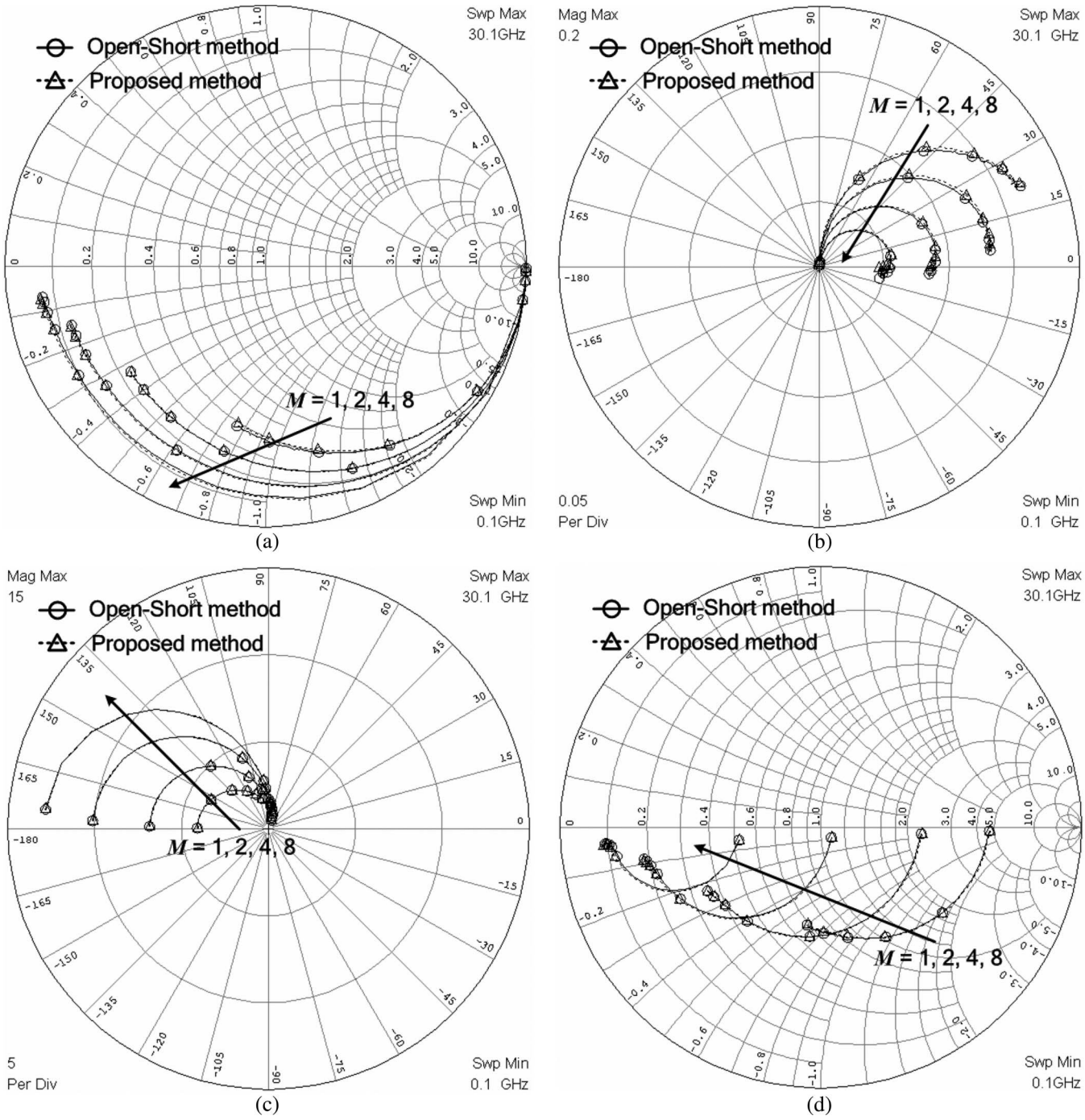

Fig. 7. Deembedded S-parameters of the fixtured MOSFETs with different multiplier factors ($M = 1, 2, 4,$ and 8) biased at $V_{\rm GS} = V_{\rm DS} = 1.2$ V. (a) S_{11}. (b) S_{12}. (c) S_{21}. (d) S_{22}.

gain H_{21}, maximum stable gain MSG, transconductance g_m, gate–drain capacitance $C_{\rm gd}$, gate–source capacitance $C_{\rm gs}$, and output resistance $R_{\rm ds}$. These results also show negligible differences in transistor characteristics and extracted model parameters [16] between these two methods. As shown in Figs. 5 and 8, one potential risk is that the interconnection of a different number of lines influences the extracted characteristics, particularly when the number of lines increases. This is because the parasitics of interconnection between shunt microctrips contribute to the extracted transmission-line parameters, and these effects should also be taken into account to improve the accuracy of the proposed method. As a result, the proposed geometry-scalable deembedding methodology can be used to accurately extract the intrinsic device characteristics.

Typically, the conventional deembedding methods employ more than two dummy structures [2]–[7] for each DUT, and thus, the chip area for modeling test keys is considerable. The geometry-scalable method can reduce the chip area and characterization time to less than one-third (33%) of the conventional ones since only two dummy structures are needed for all DUTs on a wafer. In addition, the proposed method can be applied to characterize various devices, such as varactor, resistor, BJT,

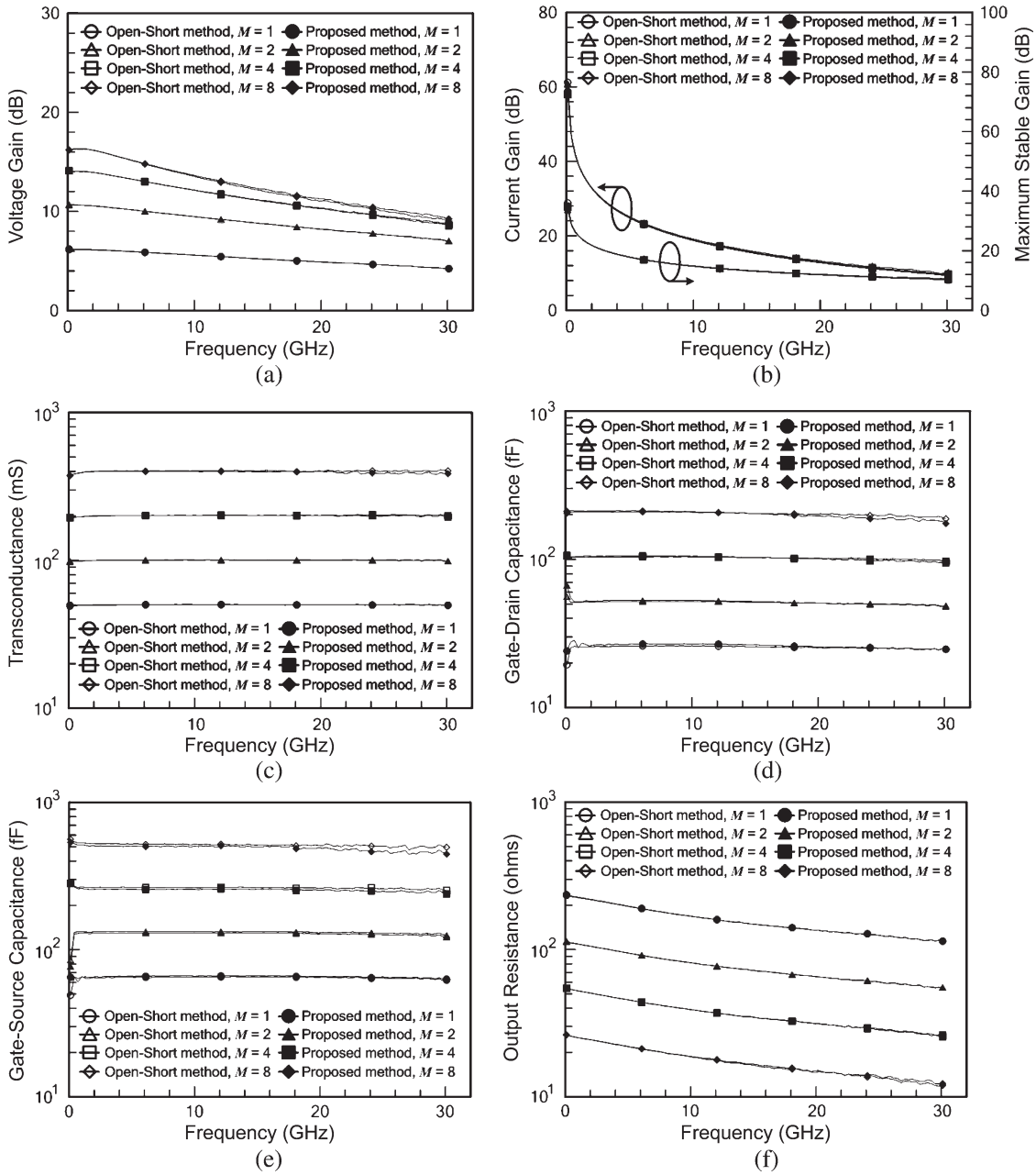

Fig. 8. Deembedded transistor characteristics and extracted model parameters of the fixtured MOSFETs with different multiplier factors ($M = 1, 2, 4,$ and 8) biased at $V_{\rm GS} = V_{\rm DS} = 1.2$ V. (a) Voltage gain G_u. (b) Current gain H_{21} and maximum stable gain MSG. (c) Transconductance g_m. (d) Gate–drain capacitance $C_{\rm gd}$. (e) Gate–source capacitance $C_{\rm gs}$. (f) Output resistance $R_{\rm ds}$.

MIM capacitor, etc., and its noise deembedding procedure can be constructed based on the studies in [17] and [18].

IV. Conclusion

In this paper, a systematic parasitic deembedding method for two-port on-wafer MOSFET characterization has been presented and verified. The proposed deembedding method based on the transmission-line theory and microwave network analysis employs only two substrate-shielded dummy structures to replicate and deembed the external parasitic networks of the fixtured MOSFETs over the whole wafer. Both the interconnect scalability and the deembedding accuracy of the proposed method are validated up to 30 GHz. The deembedded results substantiate that the proposed method is accurate, area efficient, and time saving for evaluating the intrinsic characteristics of silicon-based devices.

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