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High-resolution MOS magnetic sensor with thin oxide in standard submicron CMOS process

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Abstract

In this paper, new results obtained with an NMOS magnetic-field sensor made by an industrial 0.8 μm CMOS process are presented. The major disadvantage of MOS magnetic sensors, a larger noise, can be overcome by the submicron CMOS process with 19 nm gate oxide. The device with $W/L = 60\ \mu m/50\ \mu m$ biased at saturation region has a resolution of 150 nT $(Hz)^{-1/2}$ at 1 kHz and 400 nT $(Hz)^{-1/2}$ at 100 Hz, respectively. Even when the device size is scaled down to $W/L = 6\ \mu m/5\ \mu m$, the resolution still has the value of 1.5 μT $(Hz)^{-1/2}$ at 1 kHz. The dependence of sensitivity and current-related sensitivity for various bias conditions is discussed in detail and a simple model to explain these trends is established.

Keywords: CMOS; magnetic sensors; MOS

1. Introduction

In 1966, the MOS magnetic sensor was first reported by Gallagher and Corak [1]. The basic structure of the MOS magnetic sensor consists of a classical field-effect transistor with lateral symmetrical Hall probes as shown in Fig. 1. When a magnetic field is applied perpendicularly to the MOS element, a Hall voltage will be created at the Hall probes. Because the conduction layer in a MOS device is very thin, about 0.01 μm, the Hall voltage of a MOS device is much larger than that of the general bulk material in spite of the lower mobility in the channel region.

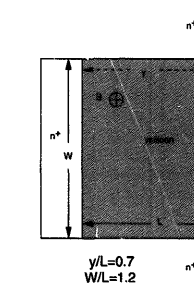

Fig. 1. Top view of NMOS magnetic sensor.

For MOS magnetic sensors, numerous studies about sensitivity and noise have been carried out to find the optimal conditions and magnetic field integrated sensors have mainly been realized using IC technology without additional processing steps [2–5] such as micromachining. According to the submicron CMOS process, the MOSFET device can be manufactured with a thin gate oxide. The thin oxide in a submicron CMOS process can help us to improve the major disadvantage of MOS magnetic sensors, which is a larger $1/f$ noise resulting from surface-carrier trapping by the oxide traps. The noise is a fundamental parameter, allowing the detection limit to be determined. If we want to improve the resolution of the MOS magnetic sensor, it is necessary for us to reduce the $1/f$ noise. The power spectral density of the low-frequency $1/f$ noise can be calculated by

$$S_V(f) \propto N_{ot}/[f(WL)(C_{ox})^2]$$

where WL is the device area, C_{ox} is the gate oxide capacitor per unit area and N_{ot} is the interface trap density. If we reduce the gate oxide thickness, we can increase the gate oxide capacitance. The better-growing thin oxide technology in the submicron CMOS process can also reduce the interface trap density. Therefore, the $1/f$ noise will be reduced more much in the submicron CMOS process. In this paper, we use the industrial 0.8 μm CMOS process with 19 nm gate oxide

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thickness to fabricate our MOS magnetic sensors and prove that when biased in the saturation region, they really have higher resolution (about 0.15 μT) than those previously reported (about 1–10 μT) [6,7]. We also compare the characteristics of devices with different areas. The various bias conditions have also been discussed with relation to sensitivity and relative sensitivity. We find the sensitivity is almostly directly proportional to gate bias when the device is biased in the saturation region and slightly inversely proportional to the gate voltage when the device is biased in the linear region. The classical MOSFET current formula and the Hall effect formula are used successfully to explain these phenomena.

2. Device design and fabrication

Fig. 1 shows the top view of our NMOS magnetic sensors, which are designed at CIC, Hinchu, Taiwan and fabricated at TSMC, Hinchu, Taiwan by the standard 0.8 μm single-poly double-metal CMOS process. The substrate concentration is 5.3×10^{16} cm^{-3}, the gate oxide thickness is 19 nm and the threshold voltage of the MOSFET is 0.8 V. The standard polysilicon gate technology can form self-aligned source, drain and lateral Hall probes. To obtain the optimal results, the geometry W/L ratio is equal to 1.2 and the Hall probes are located at $y/L=0.7$, corresponding to the maximun of the sensitivity [8,9].

3. Experimental results and discussion

3.1. Sensitivity

When a magnetic field is applied perpendicularly to the Hall plate sensor, a Hall voltage will be created between the lateral Hall probes, which is given by

$$|V_h| = GIB/(nqt) \quad (1)$$

where G is the geometry coefficient, I is the MOS drain current, B is the applied magnetic field, n is the electron concentration, q is the electron charge and t is the inversion layer thickness.

Fig. 2 shows the output Hall voltage of the device with $W/L=60$ μm/50 μm with V_g at 5 V in different applied magnetic fields. When the drain voltage of the MOS device is below 2 V, we can observe that the Hall voltage increases with the drain voltage because the MOS device is biased in the linear region. The output Hall voltages are almost constant when the device is in the saturation region. The maximum output Hall voltage of 42 mV is obtained when the device is biased with V_g at 5 V and V_d at 5 V in a 5 kG magnetic field. The sensitivity is calculated from

$$\partial|V_h|/\partial B = GI/(nqt) \quad (2)$$

Fig. 3(a) and (b) shows the sensitivity of the sensors with $W/L=60$ μm/50 μm and $W/L=6$ μm/5 μm for various bias values. We find that when the drain voltage is below 1 V, the sensitivity decreases slightly with gate voltage. These phenomena can be explained in the following statement. The MOSFET operates in the linear region when $V_g - V_t \gg V_d$ and the depth of the inversion layer is almost the same in the entire channel. If the MOSFET is in strong inversion, the surface charge density (Q_{ch}) can be calculated [10] by

$$Q_{ch} = C_{ox}(V_g - V_t) \quad (3)$$

and the MOSFET current formula [11] is

$$I_d = (W/L)\mu_n C_{ox}(V_g - V_t)V_d \quad (4)$$

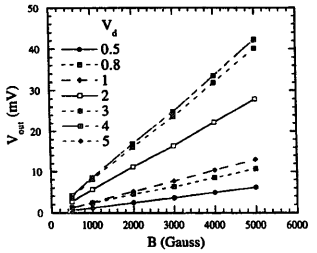

Fig. 2. Output Hall voltage of the NMOS magnetic sensor with $W/L=60$ μm/50 μm with V_g at 5 V.

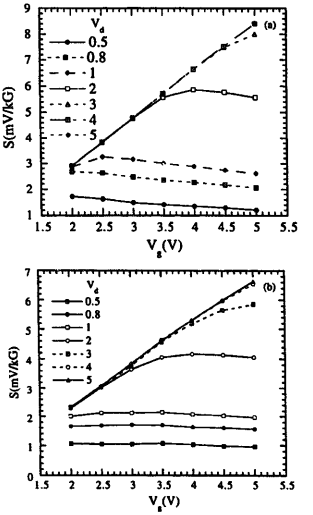

Fig. 3. Sensitivity of the sensor with (a) $W/L=60$ μm/50 μm and (b) $W/L=6$ μm/5 μm for various bias conditions.

for $V_d < V_g - V_t$, so that Eq. (2) becomes

$$\partial|V_h|/\partial B = G(W/L)\mu_n V_d = 1.2G\mu_n V_d \quad (5)$$

since $W/L = 1.2$. From Eq. (5), we can understand that the sensitivity is directly proportional to mobility and drain bias. When the gate voltage increases, the normal electrical field increases to increase the electron scattering frequency so that the electron mobility decreases [12] and the sensitivity decreases. It would be very interesting that the sensor current increases with gate bias but the Hall voltage decreases. Therefore, we can observe that the sensitivity decreases slightly with gate voltage. If the MOSFET operates in the saturation region ($V_d > 2$ V), the drain current is

$$I_d = 1/2(W/L)\mu_n C_{ox}(V_g - V_t)^2 \quad (6)$$

then

$$\partial|V_h|/\partial B = 1/2G(W/L)\mu_n(V_g - V_t) = 0.6G\mu_n(V_g - V_t) \quad (7)$$

The sensitivity is almost directly proportional to gate voltage. This characteristic is very convenient for application. We can easily control the device operation by choosing an appropriate bias condition. In Fig. 3(a) and (b), if the drain voltage is 2 V and the gate voltage is below 3.5 V, the MOSFET is biased in the saturation region so that the sensitivity curve is linear. If the gate voltage is above 3.5 V, the MOSFET is biased in the linear region so that the sensitivity decreases slightly with gate voltage.

We can conclude from Fig. 3(a) and (b) that the more stable bias condition is in the saturation region. In this region, the sensitivity is almostly independent of drain voltage and the relation of gate bias is linear, which is easily controlled in application. In our devices, the maximum sensitivity can reach 7–9 mV kG^{-1} when biased with V_g at 5 V and V_d at 5 V. We also compare the sensitivities of the two devices with different areas ($W/L = 60\ \mu m/50\ \mu m$, $6\ \mu m/5\ \mu m$) but the same W/L ratio (equal to 1.2). From Fig. 3(a) and (b), the sensitivities of both the devices are shown to be almost the same. Therefore, the values of the length and the width of the devices with the same W/L ratio does not have a strong influence on the sensitivity.

3.2. Relative sensitivity

Fig. 4 shows the current-related sensitivity of the device with $W/L = 60\ \mu m/50\ \mu m$ for various gate voltages and drain voltages. Therefore, the relative sensitivity is given by

$$S_r = 1/I(\partial V_h/\partial B) = G/Q_{ch} = G/(nqt) \quad (8)$$

If we consider the relative sensitivity in detail, the surface charge should take the drain-voltage influence [10] into account. The surface charge is given by

$$Q_{ch} = C_{ox}[V_g - V_t - V_c(v_d)] \quad (9)$$

where $V_c(v_d)$ is the channel voltage, which depends on the position of the Hall probes and drain voltage. In our samples, the position of the Hall probes is fixed so that Q_{ch} only depends on drain voltage, therefore,

$$S_r = 1/I(\partial V_h/\partial B) = G/\{C_{ox}[V_g - V_t - V_c(v_d)]\} \quad (10)$$

From Eq. (10), we can understand that the relative sensitivity is inversely proportional to the gate voltage and increases with drain voltage. Fig. 4 shows the current-related sensitivity of MOS magnetic sensors with $W/L = 60\ \mu m/50\ \mu m$. We can find that when the gate voltage is equal to 2 V, the relative sensitivity has the maximun value of 40 mV (mA kG)$^{-1}$ and when the gate voltage is equal to 5 V, the minimum value is 10 mV (mA kG)$^{-1}$. It also increases with drain voltage. The difference of the sensitivities between the devices biased at V_d of 0.5 and 5 V with the same gate voltage is about 8 mV (mA kG)$^{-1}$. Fig. 5 shows the relative sensitivity of the different sized MOS magnetic sensors ($W/L = 60\ \mu m/50\ \mu m$, $6\ \mu m/5\ \mu m$) with V_d at 0.5 and 4 V. Although the large-area device and the small-area device have the same W/L and drain current, the relative sensitivities are not the same. This shows that the surface charges of the two devices are not the same. Therefore, we can deduce from Eq. (9) that the channel voltages of the Hall probes of the two devices with the same W/L and y/L ratios

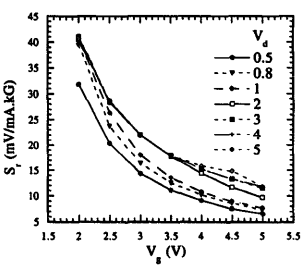

Fig. 4. Current-related sensitivity of the sensor with $W/L = 60\ \mu m/50\ \mu m$ for various bias conditions.

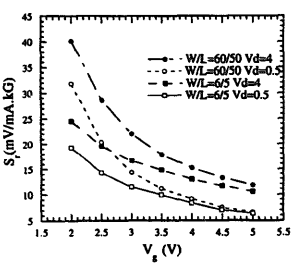

Fig. 5. Comparison of the relative sensitivities of sensors with $W/L = 60\ \mu m/50\ \mu m$ and $W/L = 6\ \mu m/5\ \mu m$ biased at $V_d = 0.5$ and 4 V.

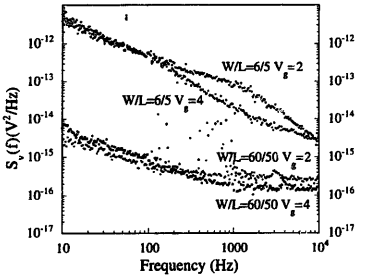

Fig. 6. Comparison of the noise power spectral of sensors with $W/L = 60\ \mu m/50\ \mu m$ and $W/L = 6\ \mu m/5\ \mu m$ with V_g at 2 and 4 V.

biased at the same V_d are different. The difference of the relative sensitivity between the two devices biased at small gate voltage is larger than that at large gate voltage. When the gate voltage is close to 5 V, the difference is very small and the relative sensitivities of both the devices approach 10 mV (mA kG)$^{-1}$.

3.3. Resolution

The limitation of detection of a MOS magnetic sensor due to the sensor noise can be defined as the minimum field B_{min} that can be observed when working in a narrow frequency bandwidth Δf (1 Hz) around a given frequency f (1 kHz), for a signal-to-noise ratio equal to 1. Therefore, B_{min} is given by

$$B_{min} = [S_v(f)\Delta f]^{1/2}/S \quad (12)$$

where $S_v(f)$ is the noise power spectral density and S is the sensitivity.

Fig. 6 shows the power spectral density S_v of the samples with $W/L = 60\ \mu m/50\ \mu m$ and $6\ \mu m/5\ \mu m$ in no magnetic field. When the device with $W/L = 60\ \mu m/50\ \mu m$ is biased at $V_g = 4$ V, $V_d = 5$ V the noise power density is only about 10^{-16} V^2 Hz^{-1} at 1 kHz and 7×10^{-16} V^2 Hz^{-1} at 100 Hz, respectively. The device with the same bias condition has a sensitivity of 6.7 mV (mA kG)$^{-1}$. Therefore, the minimum detectable magnetic field is 150 nT (Hz)$^{-1/2}$ at 1 kHz and 400 nT (Hz)$^{-1/2}$ at 100 Hz. Even when the device is scaled down to $W/L = 6\ \mu m/5\ \mu m$, the resolution is still 1.5 μT (Hz)$^{-1/2}$ at 1 kHz. These results have shown that the MOS magnetic sensor made in the submicron CMOS process with thin oxide can promote resolution about ten times better than previous reports. The main reason is that the better technology for growing thin oxide in the submicron CMOS process can reduce the interface trap density and increases the gate oxide capacitor so that the noise power decreases [13]. From the power spectral density formula, we can understand that the noise is inversely proportional to device area. To design a high-resolution MOS magnetic sensor, a larger area with high-quality thin oxide is the better choice.

4. Conclusions

Although the MOS magnetic sensor has good sensitivity, the too large noise is always the main disadvantage so that it cannot have a very high resolution. In this paper, we have proved that a MOS magnetic sensor biased in the saturation region with a high resolution of 150 nT (Hz)$^{-1/2}$ at 1 kHz can be made using high-quality thin oxide in an industrial 0.8 μm CMOS process. Because the interface state traps are reduced and the gate oxide capacitance increased, the noise can be reduced. Therefore, the deep submicron CMOS process with a thinner gate oxide (< 100 Å) and higher quality oxide could increase the resolution considerably. In our experiments, we also find that the sensitivity is almostly directly proportional to gate voltage when the device is biased in the saturation region and slightly inversely proportional to gate voltage in the linear region.

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Biographies

Hong-Ming Yang received the M.S. degree in electronic engineering from the National Chiao Tung University, Taiwan, in 1992. He is a Ph.D. student at National Chiao Tung University and has been pursuing his research on microsensors since 1993.

Yu-Chung Huang received the masters degree in electrical engineering in 1982, and the Ph.D. degree in process engineering in 1985, both from the Technical University of Berlin, Germany. Since 1985 he has been associate professor in the Department of Electronics at the National Chiao Tung University, Taiwan. His research interests are the design of sensors and methology for measurement.

Tan-Fu Lei received the B.S. degree in electrical engineering from National Cheng Kung University, Tainan, Taiwan, in 1967 and the M.S. and Ph.D. degrees in electronic engineering from National Chiao Tung University, Hsinchu, Taiwan, in 1970 and 1979, respectively. In 1983, he joined the faculty at National Chiao Tung University as an associate professor in the Department of Electronics Engineering and the Institute of Electronics. From 1984 to 1986, he was the director of the Semiconductor Research Center. Presently, he is a professor in that department and the associate director of the National Nano Device Laboratory. His research interests are semiconductor devices and magnetic sensors.

Chung-Len Lee received the B.S. degree from National Taiwan University, and the M.S. and Ph.D. degrees from Carnegie-Mellon University, Pittsburg, PA, all in electrical engineering, in 1968, 1971, and 1975, respectively. He joined the Department of Electronic Engineering, National Chiao Tung University, as a faculty member in 1975, and is currently a professor. His teaching and research have been in the areas of optoelectronics, integrated circuits and computer-aided design. He was the director of Semiconductor Research Center of the University from 1980 to 1983, and has been the director of the Submicron Professionals Training Center since 1989. He has supervised the theses of more than 100 M.S. and Ph.D. students and has published more than 200 papers in journals and conferences in the above area.

Shu-Chi Chao was born in 1957, graduated from Boston College, and from M.I.T. with a Ph.D. degree in chemistry in 1986. Presently he is an associate professor in the Department of Electrophysics, National Chiao-Tung University, Hsin-Chu, Taiwan.