Design of 2xVDD-Tolerant I/O Buffer with Considerations of Gate-Oxide Reliability and Hot-Carrier Degradation

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***Abstract* — A new 2xVDD-tolerant I/O buffer circuit, realized with only 1xVDD devices in nanoscale CMOS technology, to prevent transistors against gate-oxide reliability and hot-carrier degradation is proposed. The new proposed 2xVDD-tolerant I/O buffer has been implemented in a 130-nm CMOS process to serve a 2.5-V/1.2-V mixed-voltage interface without using the additional thick gate-oxide (2.5-V) devices. This 2xVDD-tolerant I/O buffer has been successfully confirmed by the experimental results with a signal speed of up to 133 MHz for PCI-X application.**

I. INTRODUCTION

With the rapid development of complementary metal oxide semiconductor (CMOS) techniques, the transistor dimension has been continually scaled down to reduce chip area, to increase operating speed, and to save power consumption. As well as, the normal supply voltage (VDD) to drive the chip is also reduced correspondingly. The thickness of gate oxide becomes much thinner in order to reduce the core power supply voltage (VDD) for resulting in lower power consumption. In the meanwhile, the maximum tolerable voltage across the transistor terminals (drain, source, gate, and bulk) should be correspondingly decreased to ensure lifetime. However, some earlier standardized protocols or ICs designed and fabricated with previous (high-VDD) CMOS generations may communicate in a microelectronics system with the chips fabricated in advanced (low-VDD) CMOS processes. Therefore, the chips in advanced CMOS processes will face to the interface of input signals with voltage levels higher than their normal supply voltage (VDD). Such mixed-voltage I/O interfaces must be designed to overcome several problems, such as gate-oxide reliability [1], hot-carrier degradation [2], and undesired circuit leakage paths [3].

A conventional mixed-voltage I/O buffer with the gate-tracking circuit and the dynamic n-well bias circuit is shown in Fig. 1 [4]. This mixed-voltage I/O buffer can tolerate to 2xVDD input signal without suffering gate-oxide reliability, hot-carrier degradation, and the undesired circuit leakage in the steady state. However, during the transition from receiving 2xVDD input signal to transmitting 0-V output signal, the transistors MN0 and MN3 will suffer hot-carrier degradation. The transistor MP5 also suffers gate-oxide reliability problem. Moreover, the transistors MN2, MP2, and MN3 also suffer hot-carrier degradation during the transition from receiving 2xVDD input signal to transmitting VDD output signal.

A modified design with three-stacked transistors for such a 2xVDD-tolerant I/O buffer circuit was reported in [5] to eliminate hot-carrier issue, as shown in Fig. 2. However, the gate-oxide overstress issue still happened in the transistor MP1 in Fig. 2 during the transition. Also, the transmission circuit (with transistors MN2 and MP2 in Fig. 2) still suffers the hot-carrier degradation issue during the transition.

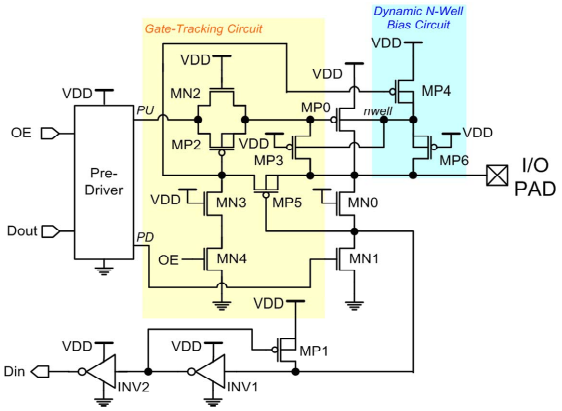


Figure 1. The conventional mixed-voltage I/O buffer designed with gate-tracking circuit and dynamic n-well bias circuit to slove gate-oxide reliability issue [4].

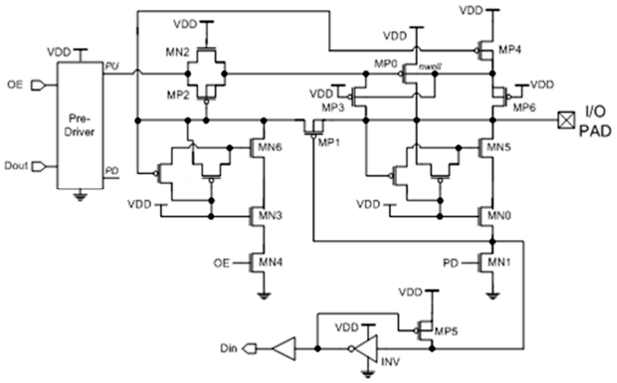


Figure 2. The mixed-voltage I/O buffer designed with three-stacked transistors to prevent hot-carrier degradtion [5].

In this work, to solve the aforementioned problems in the prior arts, a 2xVDD-tolerant I/O buffer with new transmitting circuit and new gate control circuit to completely solve the gate-oxide reliability and hot-carrier degradation is proposed and verified in a 130-nm CMOS process with only 1xVDD devices.

II. New Proposed I/O Buffer

The new proposed 2xVDD-tolerant I/O buffer realized with only 1xVDD devices to prevent transistors against gate-oxide reliability and hot-carrier degradation is shown in Fig. 3, which keeps the significant design advantages of the prior arts with three additional new modifications. The design concepts of the major parts in this new proposed I/O buffer are introduced in the following.

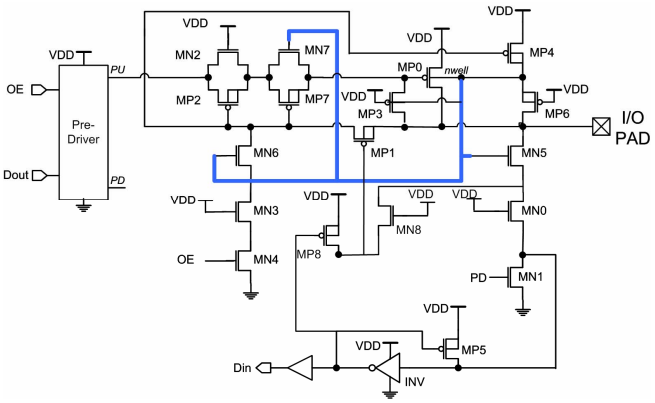


Figure 3. The new proposed 2xVDD-tolerant I/O buffer realized with only 1xVDD devices to prevent transistors against gate-oxide reliability and hot-carrier degradation.

A. Circuit Operation

The basic structure for mixed-voltage I/O buffer typically includes a pre-driver, a dynamic n-well bias circuit, two or three-stacked transistors, gate-tracking circuit, and an input stage unit, which is controlled by an enable signal EN. The circuit operating modes include a receive mode (for receiving an input signal) and a transmit mode (for transmitting an output signal). The corresponding circuit operating voltages in the proposed 2xVDD-tolerant I/O buffer circuit in Fig. 3 are listed in Table I.

TABLE I
OPERATIONS OF THE NEW PROPOSED 2XVDD-TOLERANT I/O BUFFER IN STEADY STATE

Operating Modes	Signals at I/O PAD	Voltage Level of the Floating N-well
Receive	Low (0 V)	VDD
Receive	High (2xVDD)	2xVDD
Transmit	Low (0 V)	VDD
Transmit	High (VDD)	VDD

B. Gate Control Circuit

Dynamic floating n-well technique has been applied to the mixed-voltage I/O circuit to prevent the possible leakage current path in the PMOS transistors of the pull-up network. By surveying the voltage waveform of the floating n-well, the floating n-well voltage is kept at VDD in receiving 0 V and in transmit mode, and kept at 2xVDD for receiving input signal of 2xVDD. Such a voltage level at the floating n-well presents a similar function to the gate control signal for the top transistor (MN5) of the three-stacked NMOS structures. Therefore, the new gate control circuit can be directly implemented by the dynamic floating n-well self-biased circuit to save silicon area.

C. Transmitting Circuit

The new transmitting circuit uses the "stacked" concept in both PMOS and NMOS transistors appropriately to create a new "stacked transmission gate." As shown in Fig. 3, the gate terminal of MN2 is connected to VDD, and the gate terminal of MN7 is connected to the floating n-well terminal, so are MN3 and MN0. Aside from NMOS transistors, the gate terminals of other two PMOS transistors are connected together to the drain terminal of MN6. In the transmit mode, the transistors MN7 and MP7 serve as a transmission gate (similar to MN2 and MP2). When receiving an input signal of 2xVDD at I/O pad, transistors MP2 and MP7 turn off and the transistors MN7 and MN2 prevent high drain-to-source voltage (V_{ds}). During the transition from receiving an input signal of 2xVDD to transmitting an output signal of VDD, the drain voltage of transistor MN2 would keep at 2xVDD - ΔV initially due to the diode-connected transistor MN7 (where ΔV is the V_{ds} of the diode-connected transistor MN7). Then, it keeps a lower V_{ds} across MN2 and MP2 after the source voltage of MN2 starts to be pulled down to 0 V. Due to the lower V_{ds} of the stacked structures, the hot-carrier degradation problem in the transmission gates of Fig. 1 and Fig. 2 would not appear in this new design. Moreover, since the gate voltage of MP2 and MP7, and the drain and source terminals of MN7 are pulled down to 0 V while the gate terminal of MP0 is pulled down to 0 V, the gate-source voltages and the gate-drain voltages of MN7, MP7, MN2 and MP2 keep in a safe region (lower than VDD). Thus, the new transmitting circuit does not suffer hot-carrier degradation and gate-oxide overstress problems.

D. Modificaton to Prevent Gate-Oxide Overstress

In Fig. 1, the gate terminal and the source terminal of transistor MP5 are connected to the drain terminal and the source terminal of MN0, respectively. In Fig. 2, the gate terminal and the source terminal of the MP1 is connected to the source terminal of MN0 and the drain terminal of MN5, respectively. During the transition from receiving an input signal of 2xVDD to transmitting an output signal of 0V, transistor MN0 in Fig. 1 suffers hot-carrier degradation and the voltage difference between the drain terminal of MN5

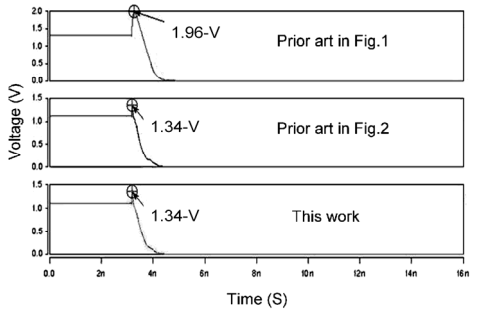
and the source terminal of MN0 in Fig. 2 is much larger than VDD, therefore transistor MP5 in Fig. 1 and transistor MP1 in Fig. 2 also suffer gate-oxide reliability problem.

To solve such a problem, the gate terminal of MOS transistor can be connected to an appropriate node instead of the original one, which is the source terminal of MN0 in Fig. 1 and Fig. 2. In Fig. 3, the appropriate point is realized by the additional connection of a PMOS transistor and an NMOS transistor. MN8 provides similar function as MN0 with smaller size, and transistor MP8 works similarly as MP5. With the similar structure, the gate terminal of MP1 receives similar voltage as that of MP1 in previous design. In the receive mode, the gate voltage of MP1 is conducted to VDD by MN8 and MP8. In the transmit mode, the gate voltage is conducted to 0 V or VDD as the source terminal of MN1 does. However, since the gate terminal of MP1 is not conducted to ground as immediately as the drain terminal of MN1 does, large $|V_{gs}|$ value does not occur in MP1. The gate voltage of MP1 is pulled down gradually by MN8 and the other NMOS transistors when transition from receiving 2xVDD input signal to transmitting 0-V output signal. Thus, the new proposed design does not suffer gate-oxide reliability problem in both steady state and transient state.

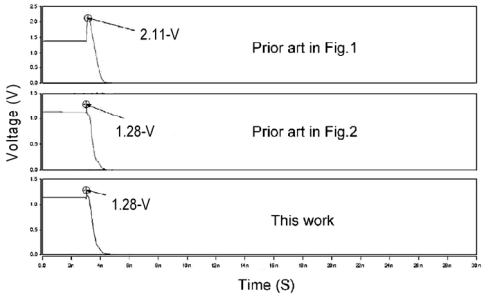
III. Simulation Results

The simulation results of the new proposed 2xVDD-tolerant I/O buffer to prevent hot-carrier degradation and gate-oxide reliability have been verified by the HSPICE simulation in a 130-nm CMOS technology with VDD of 1.2 V. Fig. 4(a) shows the V_{ds} of MN0 among the three I/O buffers, from receiving 2.5-V input signal to transmitting 0-V output signal. Fig. 4(b) shows the V_{ds} of MN3 among the three I/O buffers from receiving 2.5-V input signal to transmitting 0-V output signal. In Fig. 4(a) and Fig. 4(b), MN0 and MN3 of the prior art in Fig. 1 suffer serious hot-carrier degradation problem due to the large V_{ds}. Since the drain-to-source voltage of MN0 and MN3 are nearly the same for the new buffer shown in Fig. 3 and the buffer shown in Fig. 2, the capabilities of preventing hot-carrier degradation when receiving 2.5-V input signal are almost the same between these two buffers (Fig. 2 and Fig. 3). However, the new buffer is more efficient in area saving.

Fig. 5 shows the V_{ds} waveforms of the transistors in the transmitting circuit of the new proposed I/O buffer and the other two previous designs, from receiving 2.5-V input signal to transmitting 1.2-V output signal. As shown in Fig. 5, the transistors in the new proposed I/O buffer have lower drain-to-source voltage, which is more robust to prevent hot-carrier degradation. Fig. 6 shows the comparison of the gate-to-source voltages between prior arts and new proposed I/O buffer. The peak $|V_{gs}|$ value of the I/O buffers in the prior designs is larger than VDD of 1.2 V. However, the V_{gs} of MP1 in the proposed I/O buffer is below VDD, which is confirmed more robust than the previous designs in both hot-carrier degradation and gate-oxide reliability.



(a)



(b)

Figure 4. Comparison of the drain-to-source voltage (V_{ds}) of (a) MN0 and (b) MN3 between the new proposed I/O buffer and the two previous designs (Fig. 1 and Fig. 2) during the transition from receiving 2.5-V input signal to transmitting 0-V output signal.

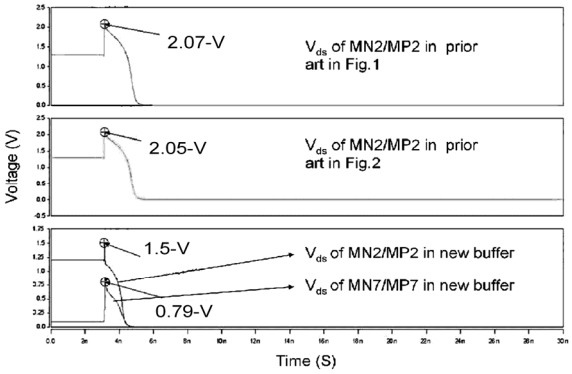


Figure 5. Comparison of the drain-to-source voltage (V_{ds}) between transistors in the transmitting circuits during the transition from receiving 2.5-V input signal to transmitting 1.2-V output signal.

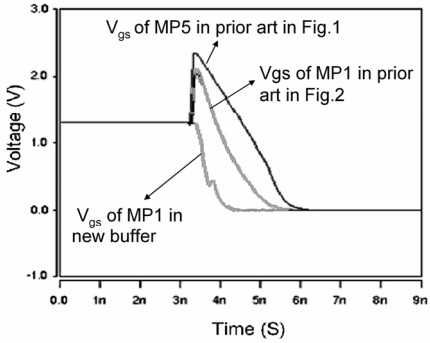


Figure 6. Comparison of the gate-to-source (V_{gs}) voltage across some transistors in the proposed I/O buffers and the two previous designs (Fig. 1 and Fig. 2) during the transition from receiving 2.5-V to transmitting 0-V output signals.

IV. EXPERIMENTAL RESULTS

The new proposed 2xVDD-tolerant I/O buffer has been fabricated in a 130-nm 1.2-V CMOS process with only thin-oxide (1.2-V) devices. The layout top view of test chip is shown in Fig. 7 with the corresponding circuit blocks, including VDD power cell, I/O circuit, Dout pad, EN pad, Din pad, and VSS power cell. The size of the I/O circuit is 107.73μm×65.38μm (not including the bond pad). Fig. 8 shows the measured waveforms of the proposed 2xVDD-tolerant I/O buffer in the receive mode to receive the 1-MHz input signals with voltage swing of 0-to-2.5 V at I/O PAD, where the input data has been successfully transmitted to Din with a voltage swing of 0-to-1.2 V. Fig. 9(a) and Fig. 9(b) show the measured waveforms at the I/O pad in the transmit mode to transmit the 10-kHz and 133-MHz output signals with a voltage swing of 0-to-1.2 V given at Dout, respectively.

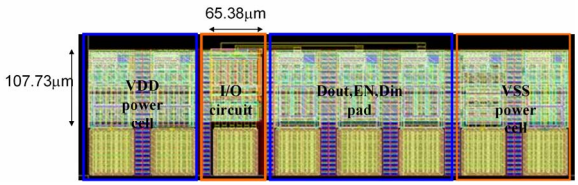


Figure 7. Layout top view of test chip to verify the new proposed 2xVDD-tolerant I/O buffer in a 130-nm CMOS process.

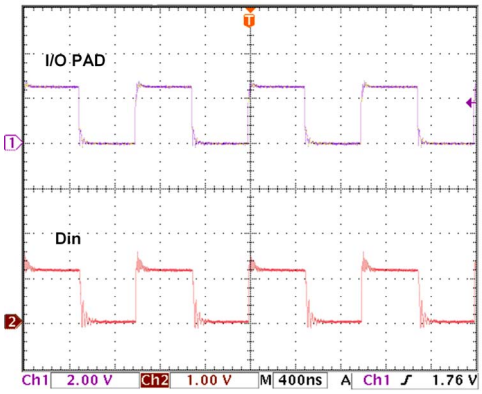
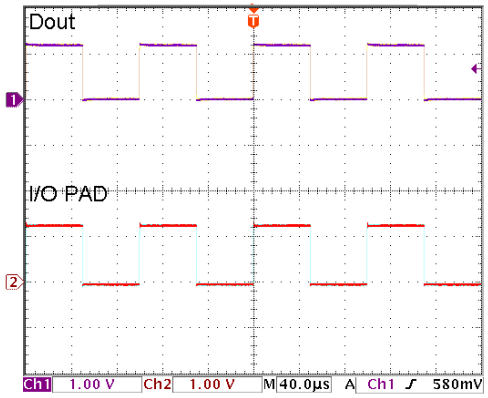


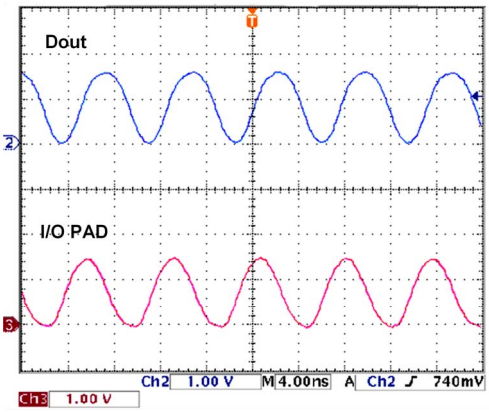
Figure 8. Measured waveforms of the proposed 2xVDD-tolerant I/O buffer operating at VDD of 1.2 V when receiving 0-to-2.5 V input signals at I/O PAD.

V. CONCLUSION

A new 2xVDD-tolerant I/O buffer against gate-oxide overstress and hot-carrier degradation has been successfully verified in a 130-nm 1.2-V CMOS process with only thin-oxide devices. The gate-to-source, gate-to- drain, and drain-to-source voltages of the transistors in the new proposed 2xVDD-tolerant I/O buffer can be kept within the normal operating voltage (VDD). The new proposed 2xVDD-tolerant I/O buffer can receive 1.2-V/2.5-V input signals or transmit 1.2-V output signals up to 133 MHz, which is compatible to the I/O specifications of PCI-X in the mixed-voltage I/O interfaces.



(a)



(b)

Figure 9. Measured waveforms at I/O pad of the propsoed 2xVDD-tolerant I/O buffer operating at VDD of 1.2 V when transmitting 0-to-1.2 V output signals at (a) 10 kHz and (b) 133 MHz.

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