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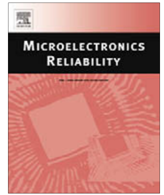

Device and circuit level suppression techniques for random-dopant-induced static noise margin fluctuation in 16-nm-gate SRAM cell

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ABSTRACT

In this study, a three-dimensional "atomistic" coupled device-circuit simulation is performed to explore the impact of process-variation-effect (PVE) and random-dopant-fluctuation (RDF) on static noise margin (SNM) of 16-nm complementary metal–oxide–semiconductor (CMOS) static random access memory (SRAM) cells. Fluctuation suppression approaches, based on circuit and device viewpoints, are further implemented to examine the associated characteristics in 16-nm-gate SRAM cells. From the circuit viewpoint, the SNM of 8T planar SRAM is enlarged to 230 mV and the variation of SNM (σ_{SNM}) is reduced to 22 mV at a cost of 30% extra chip area. As for device level improvement, silicon-on-insulator (SOI) FinFETs replaced the planar MOSFETs in 6T SRAM is further examined. The SNM of 6T SOI FinFETs SRAM is 125 mV and the σ_{SNM} is suppressed significantly to 5.4 mV. However, development of fabrication process for SOI FinFET SRAM is crucial for sub-22 nm technology era.

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1. Introduction

Threshold voltage (V_{th}) fluctuation is pronounced and becomes crucial for the design window and reliability of ultra large-scale integration devices and circuits [1–4], as the dimension of CMOS devices shrunk into sub-45 nm scale. Randomness factors resulting from manufacturing process have induced significant fluctuations of electrical characteristics in 16 nm CMOS devices and circuits. Intrinsic parameter fluctuations, such as process variations and random dopants fluctuation may limit the functionality due to significant component mismatch in area constrained circuits, such as static random access memory (SRAM).

In this study, an experimentally validated three-dimensional (3D) "atomistic" coupled device-circuit simulation approach is employed to analyze the process-variation- and random-dopant-induced characteristic fluctuations in 16-nm 6T and 8T SRAM circuits [5]. Based on the statistically generated large-scale doping profiles, 3D device simulation is first performed by solving a set of quantum drift–diffusion equations consisting of the Poisson equation, the current continuity equations for electron and holes, and the density gradient equation under our parallel computing system [6]. In the estimation of characteristics fluctuations of 16-nm SRAM cells, coupled device-circuit simulation [7] is then conducted due to lack of equivalent circuit models for 16 nm CMOS devices. This approach considers the richest physical insight and allows us to concurrently capture the discrete-dopant-number-and-position-induced fluctuations. Notably, the accuracy of developed analyzing technique was quantitatively verified with experimental results of sub-20 nm CMOS devices [8]. Characteristics fluctuations induced by process-variation-effect (PVE) and random-dopant-fluctuation (RDF) and suppression approaches are examined for the 6T and 8T SRAM cells with 16 nm CMOS and SOI FinFET devices.

2. Methodology

The explored devices are all with $1.48 \times 10^{18}\ \text{cm}^{-3}$ nominal channel doping concentrations. They have a SiO_2 gate oxide thickness of 1.2 nm. Mid-gap gate material, TiN, is used in the device. Threshold voltage (V_{th}) of 65-nm-gate MOSFET is calibrated to 280 mV for studying the roll-off characteristics of SNM and SNM fluctuation (σ_{SNM}). For RDF, to consider the randomness of the number and position of discrete channel dopants, 6062 dopants are randomly generated in a large cube (160 nm × 160 nm × 160 nm), in which the equivalent doping concentration is $1.48 \times 10^{18}\ \text{cm}^{-3}$, as shown in Fig. 1a. The large cube is then partitioned into 125 sub-cubes of (32 nm × 32 nm × 32 nm). The number of dopants may vary from 10 to 40, and the average number is 25, as shown in Fig. 1b and c, respectively. These sub-cubes are equivalently mapped into the device channel for the 3D "atomistic" device simulation with discrete dopants, as shown in Fig. 1e. Similarly, we can generate the sets of discrete dopant cases for the 65-nm- and 16-nm-gate devices, as shown in Fig. 1d and f, respectively [1,2,8]. We also apply the statistical approach to evaluate the effect of

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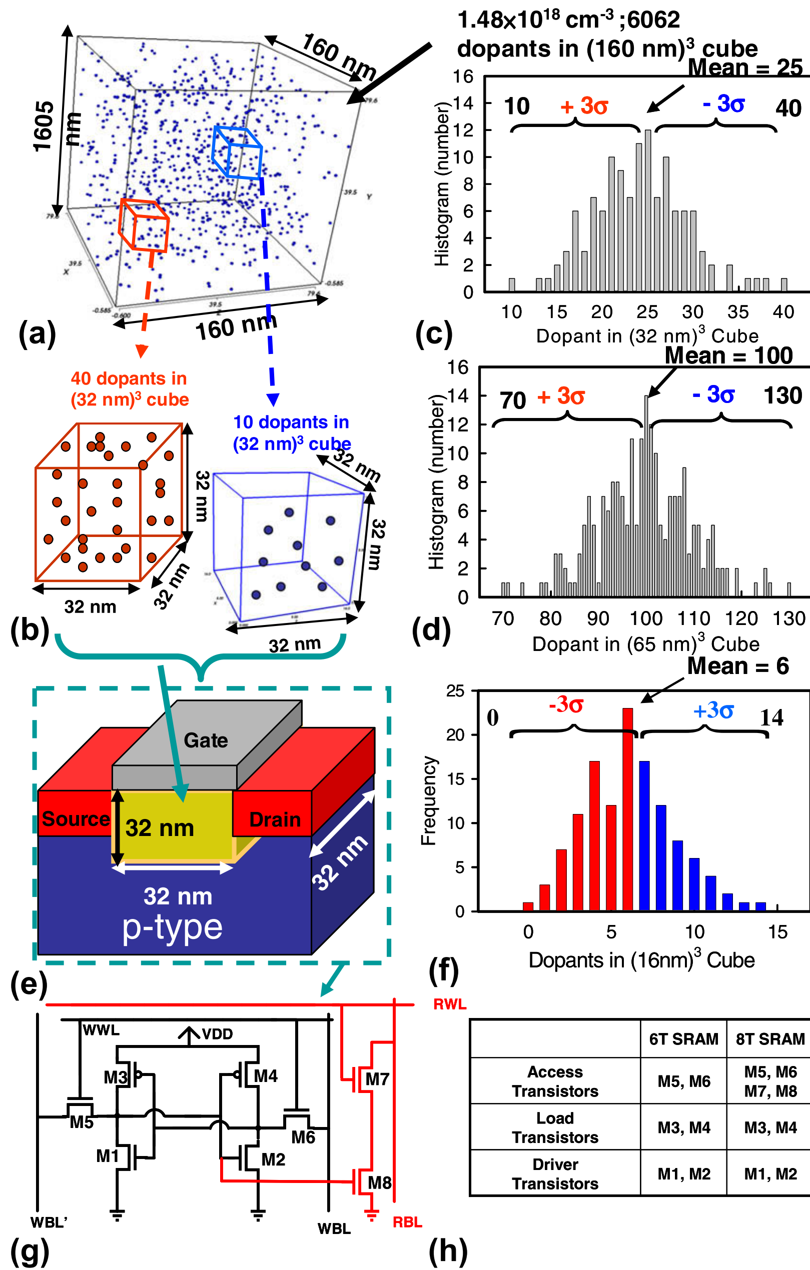


Fig. 1. (a) Discrete dopants randomly distributed in the large cube with the average concentration of 1.48×10^{18} cm^{-3}. There will be 6062 dopants within the cube, for 32-nm-gate devices, dopants may vary from 10 to 40 (average is 25), within its sub-cubes of 32 nm × 32 nm × 32 nm (b and c). The sub-cubes are equivalently mapped into channel region for discrete dopant simulation as shown in MOSFET (e). The dopants may vary from 70 to 130 (average = 100) for 65-nm-gate devices (d) and 0 to 14 (average = 6) for 16-nm-gate devices (f). The schematic of 6T SRAM cell (g), where the circuit including the red part is for 8T SRAM cell. The main functions of all transistors are summarized in (h).

process-variation-effect [9], following the projections of the ITRS 2007. Fig. 1g illustrates the explored 6T (circuit without red part) and 8T SRAM cells and the main function of each transistor is summarized in Fig. 1h. In estimating circuit characteristics of ultra-small nanoscale devices, and for capturing the discrete-dopant-number-and-position-induced fluctuations, coupled device-circuit simulation is employed. Device characteristic of SRAM is first estimated by solving the device transport equations and are used as initial guesses in the coupled device-circuit simulation. The circuit nodal equations of the test SRAM circuit are formulated, according to the current and voltage conservation laws (i.e., KCL and KVL), and then directly coupled to the device transport equations (in the form of a large matrix containing the circuit and device equations), which are solved simultaneously to obtain the circuit characteristics.

3. Results and discussion

Fig. 2a and b shows the roll-off characteristics for V_{th} and SNM for 65-nm- to 16-nm-gate n-type planar MOSFETs, respectively. The error bars are the RDF- and PVE-induced V_{th} fluctuation (σV_{th}) and σ_{SNM} for each corresponding technology node. As the gate length scales from 65 nm to 16 nm, the threshold voltage is decreased and the total σV_{th} increases significantly from 16 mV to 64 mV. Moreover, The RDF plays the major source of fluctuation

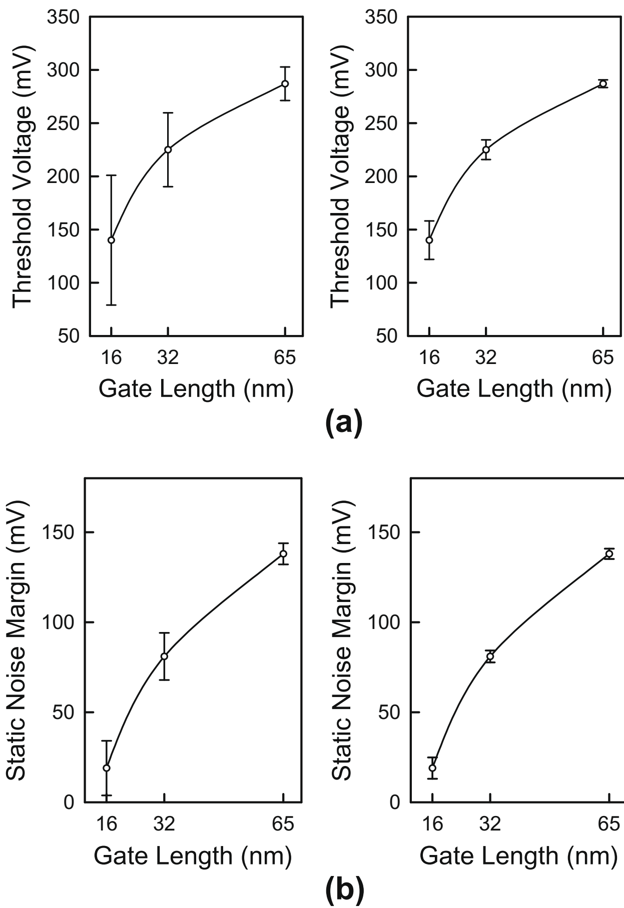


Fig. 2. (a)V_{th} and (b) SNM fluctuations induced by RDF and PVE for different gate lengths of planar MOSFETs.

and may induce two to four times larger fluctuation than the PVE. The V_{th} of 16-nm MOSFET is around four times larger than that of 65-nm, which follows the trend of analytical model [10]. For SNM and σ_{SNM}, as gate length scales from 65 nm to 16 nm, SNM decreases significantly from 138 mV to 20 mV. Fig. 3a shows the normalized σ_{SNM} for the explored SRAM. For the normalized σ_{SNM}, the RDF induced normalized SNM fluctuation increases from 4.3% to 80%. The significant increase of SNM fluctuation reveals the highly dependence of SNM fluctuation on the dimensions of transistors. To confirm the simulation accuracy for circuit characteristic fluctuations and further find out the most sensitive components in SRAM, the transistors in a 6T 16-nm-gate SRAM are classified into driver, access, and load transistor and then analyzed. Fig. 3b shows the sensitivity of SRAM by investigating the RDF in different transistor pairs. The access transistors contribute the largest SNM fluctuations because the stored data was read out through the access transistors during the read operation. Since the influences of each transistor pairs on total SNM fluctuation (σ_{SNM_Total}) are almost statistically independent, σ_{SNM_Total} can be expressed as:

$$\sigma^2_{SNM_Total} \approx \sigma^2_{SNM_Driver} + \sigma^2_{SNM_Access} + \sigma^2_{SNM_Load}, \quad (1)$$

where σ_{SNM_Driver}, σ_{SNM_Access}, and σ_{SNM_Load} are σ_{SNM} induced by the driver, access, and load transistors, respectively. The component wise calculation of σ_{SNM} using the right hand side of Eq. (1) shows σ_{SNM_Total} is about 36 mV, which is a good agreement to the result obtaining from all transistor with totally random fluctuation, 38 mV.

Due to the worse operation characteristics for 6T planar CMOS SRAM with V_{th} = 140 mV, various improvement and suppression approaches based on the circuit and device viewpoints are implemented to examine the associated characteristics in 16-nm-gate SRAM cells. From the circuit viewpoint, an 8T planar CMOS SRAM architecture [5] is first explored. Fig. 4a shows the static transfer characteristics of 8T SRAM cells including RDF-fluctuated cases, where the device V_{th} is 140 mV. The dashed lines illustrated RDF and PVE fluctuated cases, and the solid line is the nominal case. Due to the separation of data access element, the influence result from bit-line is reduced and increased the nominal SNM to 233 mV. The RDF induced SNM fluctuation is 22 mV, which is less than 10% variation. Comparing with original planar 6T SRAM cell, the nominal SNM is 12 times larger and normalized RDF induced SNM fluctuation is suppressed by a factor of 8.4. Though the 8T SRAM can enlarge the SNM and reduced the SNM fluctuation, the chip area is increased by 30%. Notably, the 6T SRAM with cell ratio equal to two also require 30% extra area; however, the nominal SNM is 92 mV, which is not enough for proper circuit operation and therefore will not be discuss herein.

Fig. 4b presents the sensitivity of SNM fluctuation of 8T SRAM cell, where the impact of access transistors is significantly reduced due to the read operation is not performed through these two transistors in 8T structure and the driver transistors become

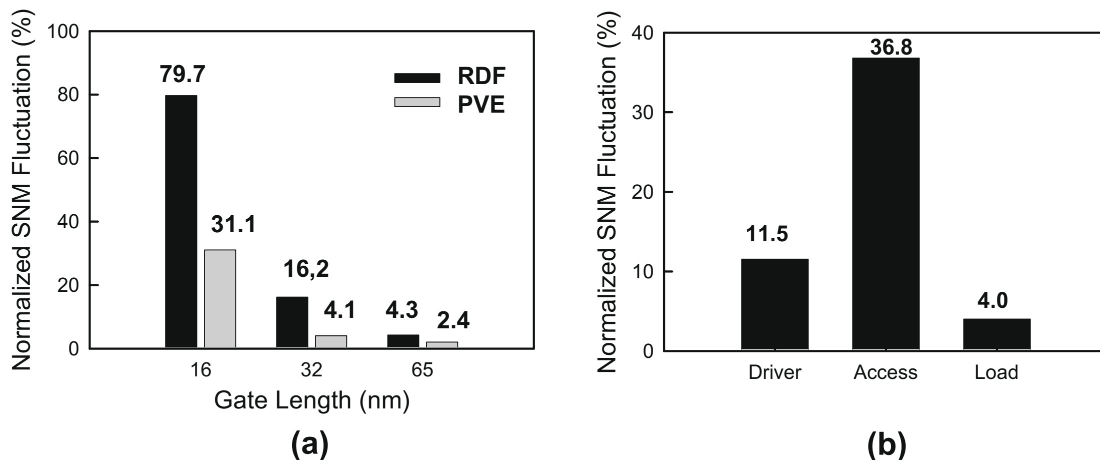


Fig. 3. (a) SNM fluctuations induced by RDF and PVE for different gate lengths of SRAM cells. (b) The influence of different transistor pairs on total SNM fluctuation of planar 6T SRAM cell.

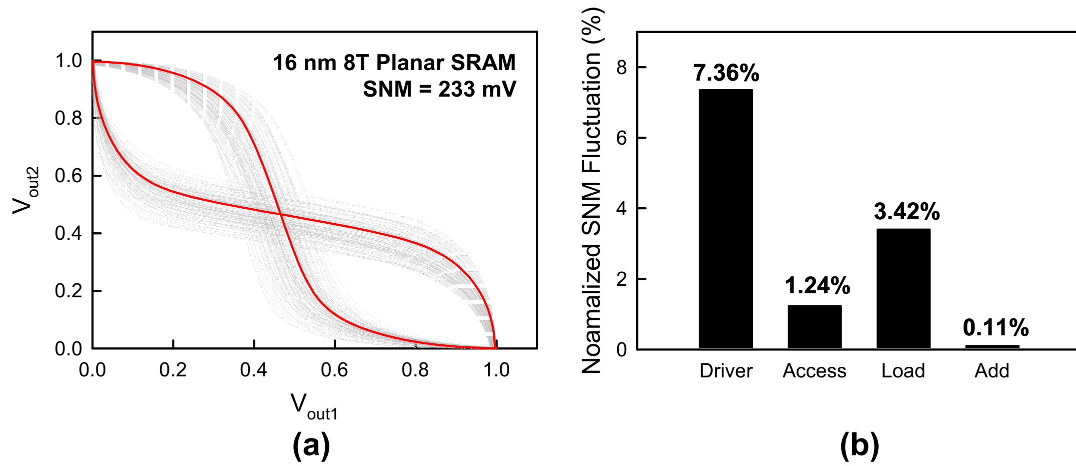


Fig. 4. (a) Static transfer characteristics of planar 8T SRAM cells. (b) The influence of different transistor pairs on total SNM fluctuation of planar 8T SRAM cell.

the dominating factor of the SNM fluctuation. To further suppress the RDF induced SNM fluctuation, vertical doping profile engineering, as shown in Fig. 5a, has been implemented to reduce the RDF induced fluctuations in planar SRAM cells with high V_{th}. Fig. 5b shows the static transfer characteristics of 16 nm planar SRAM with higher V_{th} devices with vertical doping profile. The vertical doping profile engineering can further suppress RDF induced SNM fluctuation from 41.7 mV to 30.5 mV; however, it may also suffer from more serious short channel effect (SCE), which reduces the SNM to 71 mV. Additionally, the PVE-induced SNM fluctuation is increased from 18 mV to 24.4 mV. To alleviate this point, based on the same layout area as 16-nm-gate planar MOSFETs, a 16-nm-gate SOI FinFETs as shown in Fig. 6a is then adopted to replace the planar MOSFETs to examine associated fluctuation resistivity against RDF and PVE. Without loss of generality, the equivalent doping concentration is 1.48×10^{18} cm^{-3} and the nominal V_{th} of SOI FinFETs is 140 mV. The number of dopants in a sub-cube may vary from 2 to 24, and the average is 13, as shown in Fig. 6a. Fig. 6b shows static transfer characteristics of 16 nm SOI FinFET SRAM cells, where the inset presents the RDF and PVE-induced σV_{th}. Comparing with the original case, the SNM of 6T SOI FinFETs SRAM is 125 mV and the σ_{SNM} is suppressed significantly to 5.4 mV (4.3% normalized σ_{SNM}).

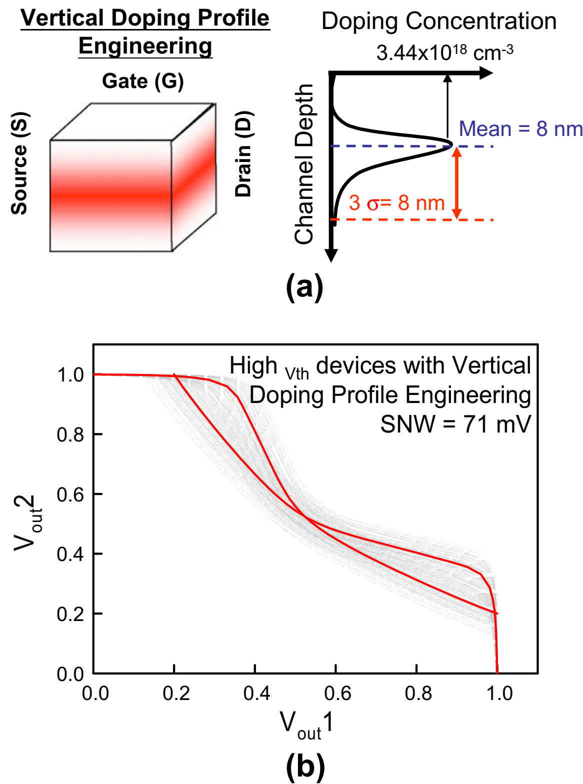
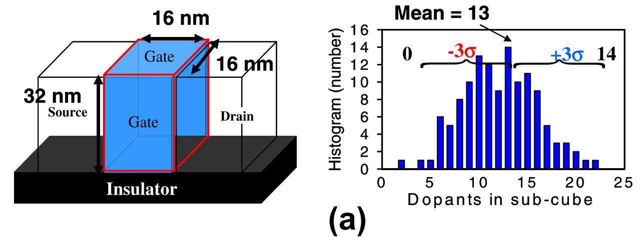


Fig. 5. (a) Illustration of doping profile engineering. (b) Static transfer characteristics of improved 6T SRAM cells, the threshold voltage of devices were raised to 350 mV.



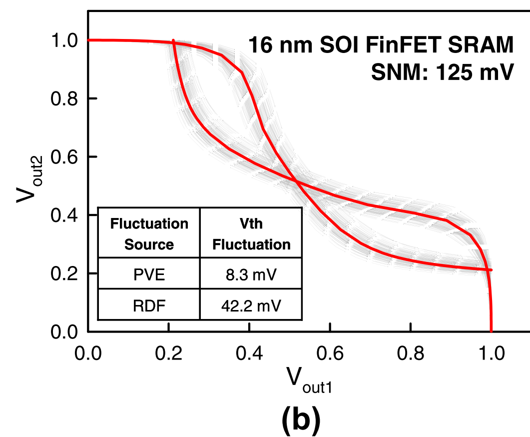


Fig. 6. (a) The explored SOI FinFET structure and distribution of generated discrete dopant cases. (b) Nominal and fluctuated static transfer characteristics of 16 nm SOI FinFET SRAM cells.

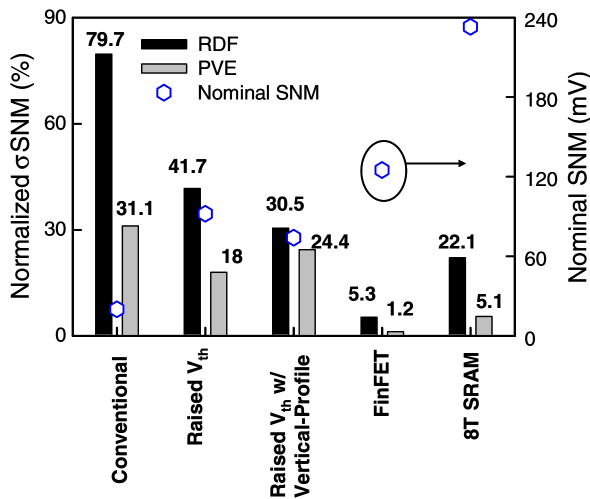


Fig. 7. Summary of intrinsic-parameter-fluctuation-induced SNM and SNM fluctuation for different improvement techniques.

4. Conclusions

Fig. 7 summarized various fluctuation improvement techniques. From the circuit viewpoint, an 8T planar SRAM architecture is explored whose SNM is enlarged to 230 mV and the σ_{SNM} is reduced to 22 mV (around 9.6% normalized σ_{SNM}) at a cost of 30% extra chip area. To prevent the increase of chip area, SOI FinFETs replaced the planar MOSFETs in 6T SRAM is further examined. The SNM of 6T SOI FinFETs SRAM is 125 mV and the σ_{SNM} is suppressed significantly to 5.4 mV (4.3% normalized σ_{SNM}). The 8T SRAM architecture can provide largest SNM and is promising in near future design; however, to prevent the increase of chip area and suppress the intrinsic parameter fluctuations, development of fabrication for SOI FinFET SRAM is crucial for sub-22 nm technology era.

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