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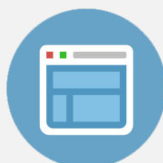
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Discrete-dopant-induced characteristic fluctuations in 16 nm multiple-gate silicon-on-insulator devices

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The impact of the number and position of discrete dopants on device characteristics is crucial in determining the behavior of nanoscale semiconductor devices. This study explores discrete-dopant-induced characteristic fluctuations in 16 nm single-, double-, triple-, and (square shape) surrounding-gate silicon-on-insulator (SOI) devices. Discrete dopants are statistically positioned in the three-dimensional channel region to examine associated carrier transportation characteristics, concurrently capturing "dopant concentration variation" and "dopant position fluctuation." An experimentally validated simulation was conducted to investigate the threshold voltage (V_{th}) fluctuation and the variation of the on- and off-state currents of the four explored structures. The fluctuations of V_{th} of the double-, triple- and surrounding-gate devices are 2.2, 3.3 and 4 times smaller, respectively, than that of planar SOI. Results of this study provide further insight into the problem of fluctuation and the mechanism of immunity against fluctuation in ultrasmall field effect transistors (FETs) with vertical channel structures, such as fin-typed FETs.
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I. INTRODUCTION

Ion implantation, diffusion, and thermal annealing induce significant random fluctuations in the electrical characteristics in nanometer metal-oxide-semiconductor field effect transistors (MOSFETs). Various randomness effects have recently been investigated both experimentally and theoretically.[1–20] Fluctuations of characteristics are caused not only by a variation in the average doping density, which is associated with a fluctuation in the number of dopants, but also with the particular random distribution of dopants in the channel region. Fluctuations are particularly pronounced when the spatial scale of doping and oxide thickness variations becomes comparable with the dimensions of devices.[12,19,20] The International Roadmap for Semiconductors has forecasted a transition from conventional bulk devices to silicon-on-insulator (SOI) devices and then to multiple-gate SOIs as high-performance devices.[21] Accordingly, nanoscale devices with vertical channel structures, such as double-, triple-, and surrounding-gate fin-type field effect transistors (FinFETs), are of great interest.[22–24] However, channel doping must be employed to alter the threshold voltage in today's semiconductor manufacturing processes. Consequently, characteristic fluctuation that is induced by discrete dopants is important in these nanoscale MOSFETs, which have fascinating structures. Diverse approaches, such as small-signal analysis,[10–12] drift diffusion,[13–15] and Monte Carlo simulation,[16–18] have recently been reported to study variation- and fluctuation-related issues in semiconductor devices. Unfortunately, the effect of the number and position of discrete dopants on the characteristics of the aforementioned devices has not been clearly investigated.

This study explores the discrete-dopant-induced characteristic fluctuations in 16 nm single-, double-, triple-, and surrounding-gate SOI devices. The discrete dopants are statistically positioned in the three-dimensional (3D) channel

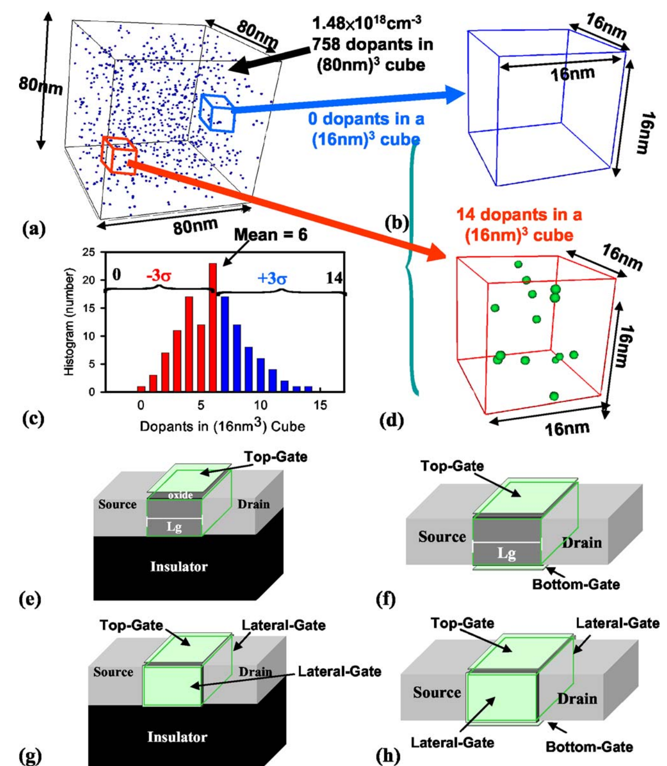

FIG. 1. (Color online) (a) Discrete dopants randomly distributed in 80 nm^3 cube with the average concentration of 1.48×1018 cm^{-3}. There will be 758 dopants within the cube, but dopants vary from 0 to 14 (the average number is 6) within its 125 subcubes of 16 nm^3 [plots of (b)–(d)]. These 125 subcubes are then equivalently mapped into device's channel region corresponding to (e) single gate, (f) double gate, (g) triple gate, and (h) (square shaped) surrounding gate for the dopant position/number-sensitive 3D simulation.

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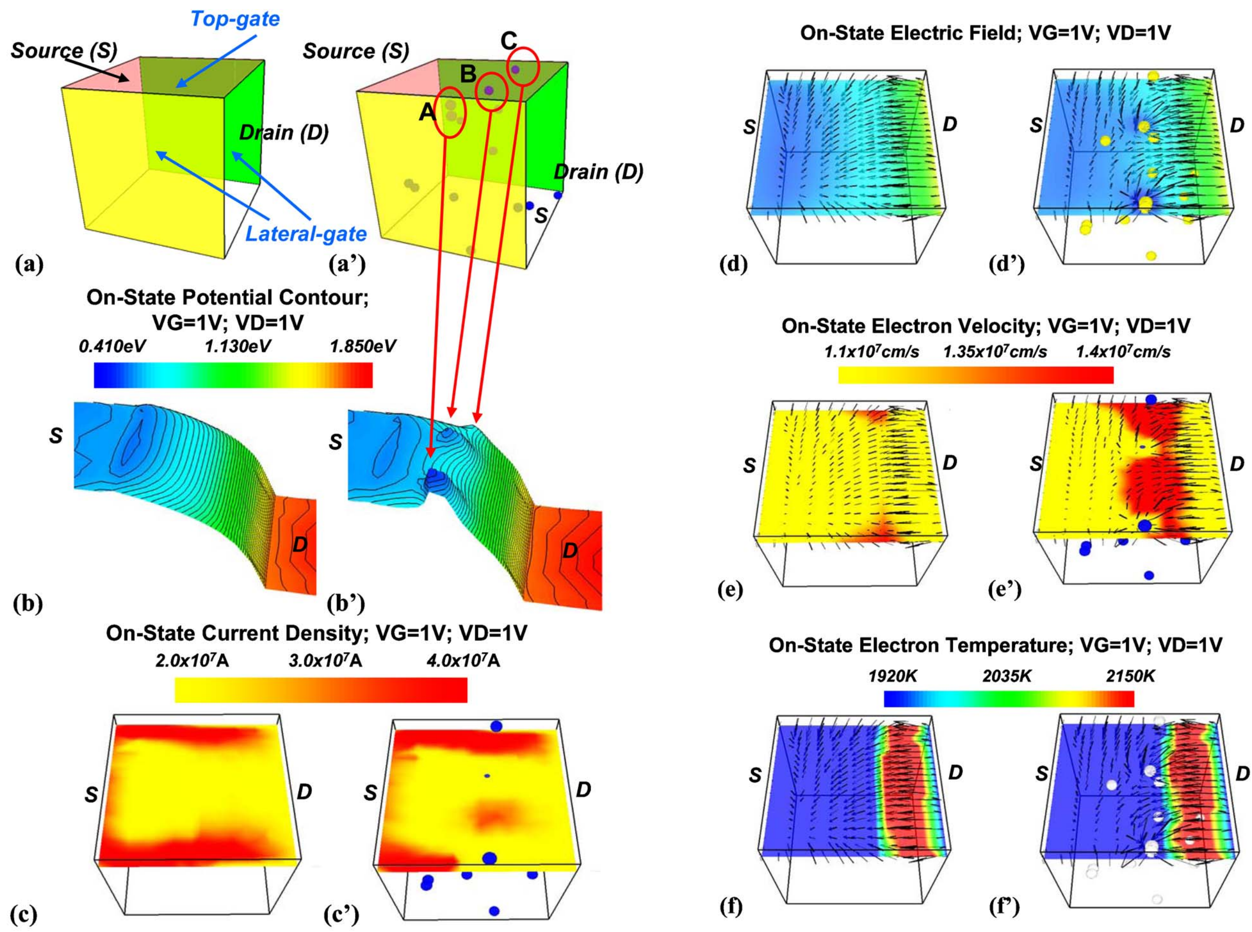

FIG. 2. (Color online) Comparison of the on-state potential contours [(b) and (b′)], the current density distributions [(c) and (c′)], the electric field [(d) and (d′)], the electron velocity [(e) and (e′)], and the electron temperature [(f) and (f′)] of the (a) the nominal case and (a′) discretely doped cases. The potential spikes (marked as A, B, and C) in (b′) are induced by corresponding dopants in (a′). All cross-sectional plots of the on-state current density distributions and off-state potential contours are extracted at 1 nm below the top-gate oxide.

region to investigate associated carrier transportation characteristics, concurrently capturing "dopant concentration variation" and "dopant position fluctuation." A statistically sound 3D "atomistic" device simulation is conducted using parallel computing system.[25–27] Based on statistically generated large-scale doping profiles, each device simulation is performed by solving a set of 3D hydrodynamic equations[27–30] with quantum corrections by the density gradient method.[31–34] In atomistic device simulation, the resolution of individual charges within a conventional drift-diffusion simulation using a fine mesh creates problems associated with singularities in the Coulomb potential.[35,36] Thus, the density gradient approximation is used to handle discrete charges by properly introducing the related quantum mechanical effects.[34] The intrinsic physical variation and characteristic fluctuations of the four studied devices are examined, and the mechanisms of fluctuation and immunity are also discussed. We notice that so far the fluctuations in device properties under various structures are limited to either drift diffusion or Monte Carlo simulations. And so the present work is unique. This article is organized as follows. Section II describes the analytic technique. Section III discusses the results and mechanism of discrete-dopant-induced fluctuation. Finally, conclusions are drawn.

II. STRUCTURE AND SIMULATION

The nominal channel doping concentration of these devices is 1.48×10^{18} cm^{-3}. They have a 16 nm gate and a gate oxide thickness of 1.2 nm. Outside the channel, the doping concentrations in the source/drain and background are 1.2×10^{20} and 1×10^{16} cm^{-3}, respectively. For the channel region, to consider the effect of a random fluctuation of the number and location of discrete channel dopants, 758 dopants are first generated in an 80 nm^3 cube, in which the equivalent doping concentration is 1.48×10^{18} cm^{-3}, as shown in Fig. 1(a). The 80 nm^3 cube is then partitioned into 125 subcuboids of 16 nm^3. The number of dopants may vary from 0 to 14 and the average number is 6, as displayed in Figs. 1(b)–1(d). These 125 subcubes are then equivalently mapped into the channel region of the device for discrete dopant simulation, as shown in Figs. 1(e)–1(h). All statistically generated discrete dopants are incorporated into the large-scale 3D device simulation, which is conducted using a parallel computing system.[25–27] According to this analyzing scenario, only channel dopants are treated discretely. The doping concentrations remain continuous in the source/drain region because the concentration of source/drain dopants is two orders of magnitude greater than that of channel dop-

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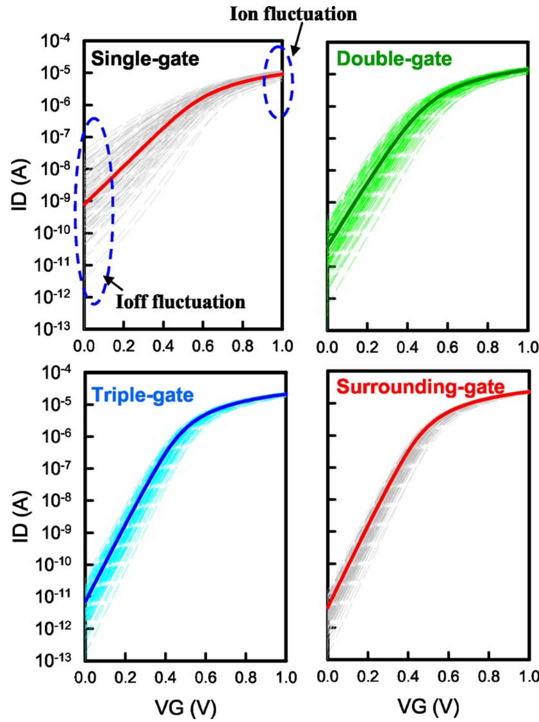

FIG. 3. (Color online) The I_D-V_G characteristics of the 500 discrete-dopant 16 nm single- and multiple-gate SOI devices, where the solid lines indicate the nominal case and the dashed lines indicate the discretely doped cases.

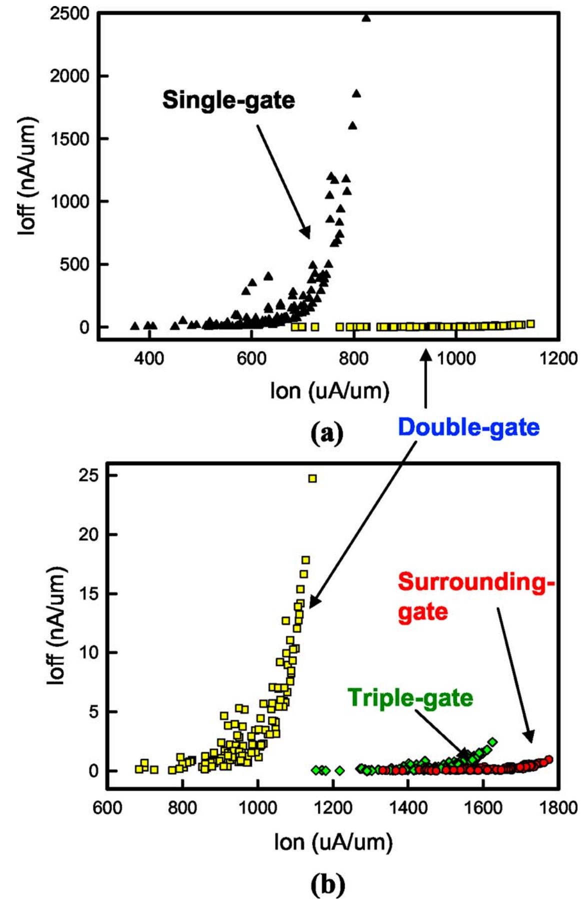

FIG. 4. (Color online) The on-off state current characteristics of the 500 discrete-dopant 16 nm single- and multiple-gate SOI devices. (a) Comparison between the single- and double-gate devices. (b) Comparison among the double-, triple-, and surrounding-gate devices.

ants. However, with this respect the present simulations only give qualitative results. Nevertheless, this approach allows us to focus on the study of characteristic fluctuations induced by the randomness of the number and position of dopants in the channel simultaneously. The statistically sound 3D atomistic device simulation technique is also computationally cost effective. The accuracy of the simulation technique was confirmed by comparing simulated fluctuation results with measurements of experimentally fabricated 20 nm devices elsewhere.[19] The threshold voltage of the four devices is adjusted by modulation of the work function and calibration to 350 mV in a unified study of characteristic fluctuations of the devices of interest.

III. RESULTS AND DISCUSSION

This section initially discusses the physical fluctuations that are induced by discrete dopants, and then the characteristic fluctuations and mechanism of immunity against fluctuations of multiple-gate SOI devices are studied.[19,20] The 3D hydrodynamic model[27–30] with quantum corrections by the density gradient method[31–34] is numerically solved to obtain the device properties, where the energy relaxation time for electrons and holes are 0.1 and 0.08 ps in both continuous and discrete dopant cases.[37] An energy-dependent mobility model is further adopted in the device simulations.[38]

Discrete-dopant-induced fluctuations, caused by local potential spikes, are determined by the corresponding dopants within the device channel. The potential spike alters not only the electric field and current conducting path but also the electron velocity, carrier mobility, and electron temperature distribution. Figure 2 depicts, for example, discrete-dopant-induced fluctuations of a triple-gate SOI transistor. All cross-sectional plots of the distributions of the on-state current density and the contours of the off-state potential are extracted 1 nm below the top-gate oxide. Figures 2(a) and 2(a′) refer to the nominal case (continuous doping is assumed) and the discretely doped case, respectively. The on-state potential contour and current density distribution of the discretely doped case, shown in Figs. 2(b′) and 2(c′), are investigated to elucidate the effect of discrete dopant on the potential and current distribution of the device. The potential spikes in Fig. 2(b′) are associated with the corresponding dopants (spikes A, B, and C) in Fig. 2(a′). The potential distribution near spike C does not vary significantly with the structure of the triple gate, which will be discussed in Sec. IV. Comparison of Figs. 2(c) and 2(c′) reveals that the current conducting path is disturbed and impeded by dopants in the channel. Changing the number and position of discrete dopants in the channel causes a significant potential variation and change in current. The current may avoid the high potential barrier region and pass through the valley between two potential spikes (such as spikes A and B). Additionally, the local field distribution, shown in Fig. 2(d′), is also perturbed significantly by discrete dopants. In the on-state condition (the gate voltage V_G=1 V; the drain voltage V_D =1 V), since the potential distribution near the dopant is relatively negative in the channel, the dopant acts as a center of a whirlpool-like electric field to repel electrons. As elec-

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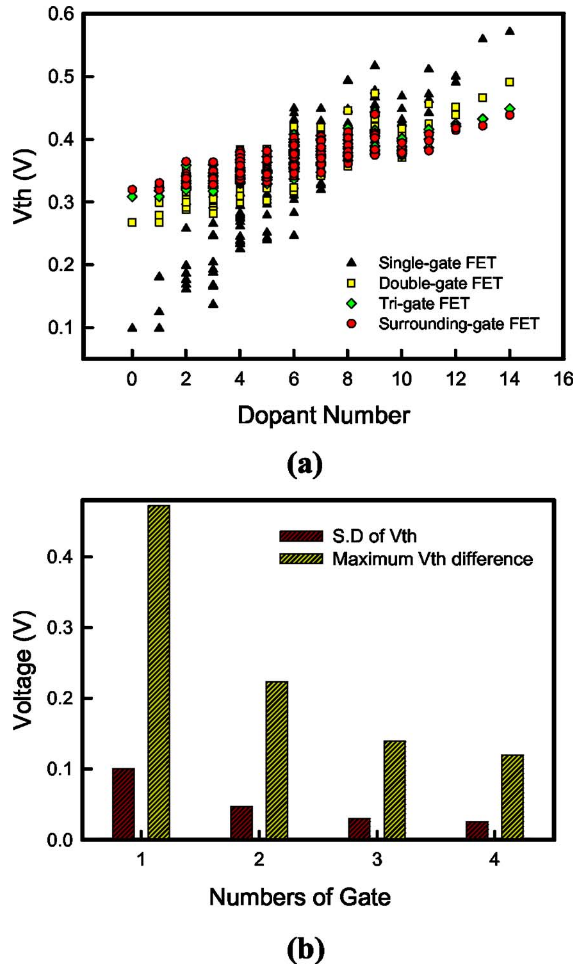

FIG. 5. (Color online) (a) Comparison of V_{th} fluctuation of the 16 nm single- and multiple-gate SOI MOSFETs. (b) Plots of the standard deviation (SD) and the maximum difference of V_{th} with respect to different gate number.

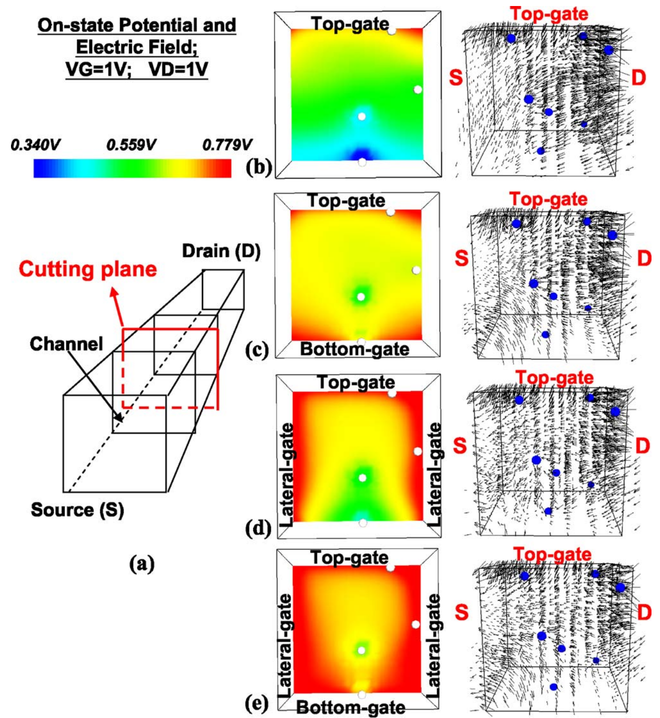

FIG. 6. (Color online) Plots of the on-state potential and 3D electric field distribution of the 16 nm SOI MOSFET with the (b) single- (c) double-, (d) triple-, and (e) surrounding-gate structure. The cross-sectional plots of the on-state potential distributions are extracted along the center of the device's channel, as shown in (a).

trons drift from source to drain, some of them encounter a negative electric field that is induced by the dopant. The lateral electric field between the source and the drain, combined with the repulsion of the dopants, twists the electron field and increases the electron velocity near the dopant, as shown in Figs. 2(e) and2(e′). This phenomenon explains why the distribution of the electron velocity remains the same to the left of the dopants at device's source. The fluctuation in the electron velocity also indicates a fluctuation of the distribution of electron temperatures, as plotted in Figs. 2(f) and 2(f′).

The characteristic fluctuations of multiple-gate SOI devices are also investigated. Figure 3 plots fluctuations of I_D-V_G for single- and multiple-gate SOI devices. The solid lines represent the nominal case and the dashed lines represent the discretely doped cases. The spread of the I_D-V_G curves shows the magnitude of the current fluctuation that is induced by discrete dopants. The average over all I_D-V_G characteristics of discrete cases do not coincide with the nominal case due to the discrete-dopant-position induced characteristic fluctuation.[39,40] The characteristics of the averaged discrete cases would nearly coincide with the nominal case for the smaller fluctuation of device with larger dimension.[41] The result shows that the single-gate device exhibits much larger current fluctuations than the multiple-gate devices. Figure 4 plots the corresponding on- and off-state current characteristics. For cases with similar on-state currents (I_{on}), the maximum fluctuation of the off-state current (I_{off}) declines as the number of gates increases; moreover, the maximum fluctuation of I_{off} in multiple-gate devices is within 20 nA/um, whereas the planar device (with a single gate) exhibits a much larger fluctuation of I_{off} (>2000 nA/um). Figure 5(a) statistically compares the threshold voltage fluctuations of the aforementioned devices. As expected, the multiple-gate device exhibits better immunity against fluctuation and the magnitude of the V_{th} fluctuation (both standard deviation and difference between maximum and minimum V_{th} declines as the number of gates increases, as plotted in Fig. 5(b). The standard deviations (SD) of single-, double-, triple-, and surrounding-gate devices are 102, 46.2, 30.9, and 25.5 mV, respectively. Calculations demonstrate that the fluctuations of V_{th} of the double-, triple-, and surrounding-gate devices are 2.2, 3.3, and 4 times smaller, respectively, than that of the planar SOI device. The equivalent channel doping concentration increases with the dopant number, substantially altering V_{th}, as shown in Fig. 5(a), and the on- and off-state currents, as plotted in Fig. 3. The magnitude of spread increases as the number of dopants increases. The discrete-dopant-position affects the fluctuation of characteristics in a different manner for a fixed number of dopants.

The mechanism of immunity of single- and multiple-gate devices against fluctuation is studied with reference to

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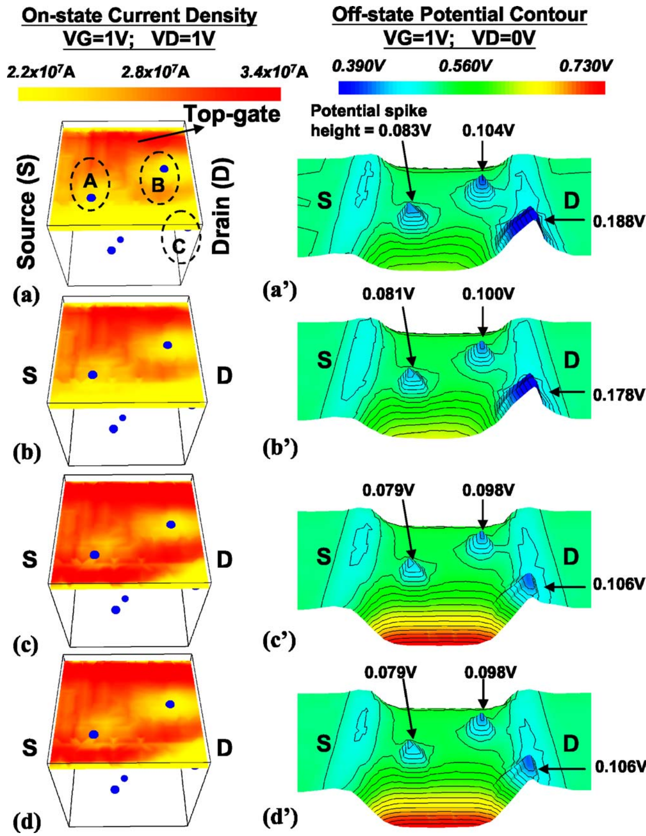

FIG. 7. (Color online) Plots of the on-state current density distributions [(a)–(d)] and the off-state potential contours [(a′)–(d′)] of the 16 nm SOI MOSFETs: [(a) and (a′)] single gate, [(b) and (b′)] double gate, [(c) and (c′)] triple gate, and [(d) and (d′)] surrounding-gate. The potential spikes in (a′)–(d′) are induced by corresponding dopants in channel [spikes A, B, and C shown in (a)]. The height of potential spikes is decreased as gate number is increased. All cross-sectional plots of the on-state current density distributions and off-state potential contours are extracted at 1 nm below the top-gate oxide.

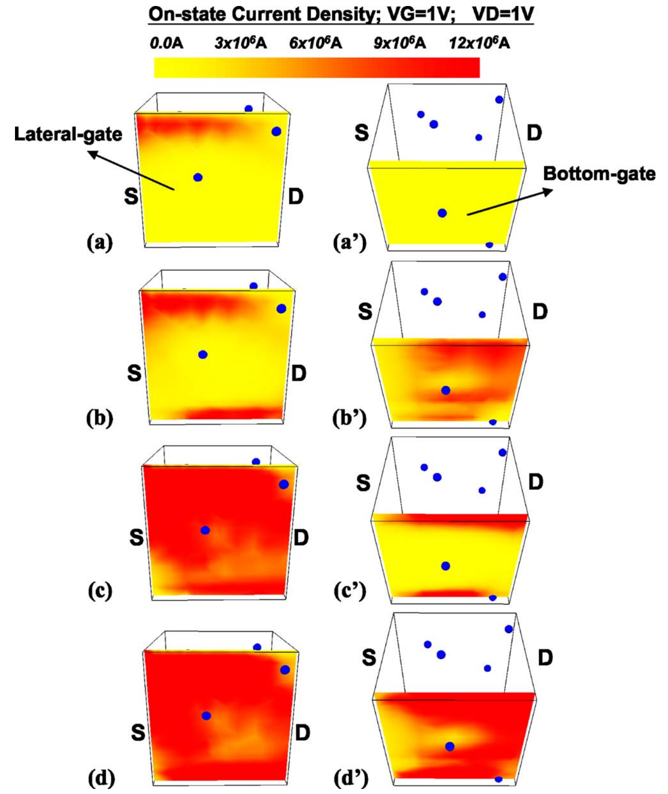

FIG. 8. (Color online) Plots of the lateral- [(a)–(d)] and bottom-gate [(a′)–(d′)] on-state current density distributions of the 16 nm devices [(a) single gate, (b) double gate, (c) triple gate, and (d) surrounding gate]. All cross-sectional figures are extracted 1 nm below the lateral- and bottom-gate oxides.

the extracted physical quantities. Figures 6(b)–6(e) plot the on-state potential along the center of the device's channel, shown in Fig. 6(a), and display 3D electric fields of single-, double-, triple-, and surrounding-gate devices, respectively. The potential and electric field of multiple-gate devices are more uniform than those of the planar device because the channel controllability is better than that of a planar device for a large gate-coverage ratio. Figure 7 compares the on-state current density, plotted in Figs. 7(a)–7(d), and the contour of the off-state potential, shown in Figs. 7(a′)–7(d′), for the 16 nm single-, double-, triple-, and surrounding-gate SOI devices, respectively. All cross-sectional plots of the on-state current density and the off-state potential are 1 nm below the top-gate oxide. As the gate-coverage ratio is increased, the on-state current density is increased and the heights of off-state potential spikes [A, B, and C in Fig. 7(a)] are reduced. The lateral-gate structure of triple- and surrounding-gate devices effectively suppresses the potential (spike C) and then increases the on-state current at the lower side of the channel, shown in Figs. 7(c) and 7(d). The lateral-gate of multiple-gate intrinsically enhances the controllability of dopant-induced fluctuations near the sidewall of the channel surface. It also accounts for why spike "C" in Fig. 2(a′) has a weaker influence on the potential distribution than spike "B." Figure 8 shows the lateral- and bottom-gate on-state current densities of the structures. Similarly, all cross-sectional plots are obtained 1 nm below the lateral- and bottom-gate oxides. Once current paths are impeded by discrete dopants on parts of channel surface, the well-gate-controlled multiple-gate structure bridges alternative conducting paths to prevent a significant fluctuation of the conduction current. Thus, the benefit of the superior vertical channel structure is that multiple-gate devices suppress potential fluctuation and provide a more stable conduction current than the planar device. As a result, the immunity against fluctuation in multiple-gate SOI devices results mainly from the uniform potential distribution and the fact that the current conduction area (multiple paths) is larger than that of a planar SOI device.

IV. CONCLUSIONS

This study investigated discrete-dopant-induced physical and electrical characteristic fluctuations in 16 nm FETs with various vertical channel structures using a 3D "atomistic" hydrodynamic simulation with quantum corrections by the density gradient method. Physical fluctuations, electrical characteristic fluctuations, and mechanism of immunity against fluctuations of multiple-gate SOI devices are studied. Under the same $V_{\rm th}$ for the four explored devices, multiple-gate devices provide a more uniform potential within the channel of the device and stabilize the current flow. The fluctuations of $V_{\rm th}$ of double-, triple-, and surrounding-gate SOI

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MOSFETs are 2.2, 3.3, and 4 times smaller, respectively, than that of the planar SOI device. An insight into the intrinsic fluctuation and the mechanism of immunity against fluctuation in multiple-gate SOI devices has been provided.

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