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ORIGINAL ARTICLE

A simulated model for cycle time reduction by acquiring optimal lot size in semiconductor manufacturing

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Abstract Cycle time reduction is one of the most critical issues in gaining a competitive advantage in wafer fabrication. People widely recognize that lot size reduction can effectively shorten production cycle time. Due to the constraints of conventional equipment and technology, this concept has not been widely applied in wafer fabrication. However, because of the invention of new technology, restrictions on equipment and processes have been reduced in recent years. Wafer lot sizing policy thus becomes an alternative in reducing cycle time. This study develops a simulation model which can acquire optimal lot size to reduce cycle time under different bottleneck loading environments. Simulation experiments based on realistic data from a Taiwan semiconductor fabricator are conducted. Sensitivity analyses of lot sizing impact upon cycle time reduction in wafer fabrication are performed as well. Numerical results demonstrate that the proposed model is sound in acquiring the optimal lot size for cycle time reduction in different loading scenarios. The model can help fabrication managers obtain optimal lot sizes in different bottleneck situations to effectively reduce product cycle time.

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1 Introduction

Cycle time reduction is one of the most important objectives in running today's businesses. It is especially true for highly competitive industries, such as the semiconductor industry. High value-added, high technology and wide usage characterize the semiconductor industry. This industry has become one of the fastest growing industries in the last decade. Wafer fabrication is perhaps the most complex modern manufacturing process.

A typical wafer fabrication process flow may contain 300–500 operation steps over 30–45 days to complete. The complicated operation requirements (reentrant flow, queue-time limit, batch/splitting operations, etc.) and shop uncertainties (machine breakdown, rework, and random yield) make its production planning and control activities very difficult. In addition, the overall capacity of wafer foundries in Taiwan has been rapidly expanded since 1996, and is estimated to account for 40% of the global wafer capacity recently. Market competitiveness is increasingly stringent due to the fast growing number of installed bases. How to improve customer service (on-time delivery with smaller order volume) and how to shorten cycle time have become the most critical issues in this environment. Although better scheduling methods, release and dispatching policies do help to achieve these goals, the reduction of lot size is another important alternative which has not been extensively studied in wafer fabrication.

Due to past equipment limitations and process technology, 24 wafers per lot was commonly adopted in wafer fabrication. Due to the progress in the advanced technology

[1], the lot size constraints on equipment and processes can be somewhat relaxed. However, wafer lot sizing policy is still fixed at the 24 wafers for one lot and putting in one cassette in most wafer fabrication. According to Just In Time (JIT) philosophy, a smaller lot size can speed up work-in-process (WIP) movement so that a shorter production cycle time will result from a lower WIP level. If the JIT concept, with a smaller lot sizing policy, could be implemented in wafer fabrication, it would be a great contribution in increasing the competitive advantage of wafer fabrication.

In the past, most research focussed on the development of dispatching and releasing rules to improve cycle time. With less restriction on the equipment, lot size reduction would be another alternative to shorten cycle time. Luss and Rosenwein [2] applied a linear programming (LP) model to a JIT environment to determine the proper batch size. Trigeiro et al. [3] presented the capacitated lot sizing problem (CLSP) algorithm, which considered setup time and capacity constraints to solve the batch size problem. They translated setup time into opportunity costs. Banerjee and Burton [4] used non-linear programming (NLP) in an economic ordering quantity (EOQ) model with regard to multi-stage WIPs. A constant machine process speed was assumed in their study. Moon [5] developed an approach for determining batch size using NLP to minimize the total costs for setup time, WIP, and product quality. He pointed out that this cost model would be more realistic in evaluating the investment for reducing setup time. Lee [6] combined the NLP and queuing model to determine the batch size of individual products. Carmon and Nahmias [7] focussed on single product wafer fabrication and obtained the best batch size through an NLP model with a stochastic distribution to serve the customers' needs. Ponnambalam and Reddy [8] provide a multi-objective algorithm which combines a genetic algorithm and a simulated annealing algorithm. The performance of this proposed algorithm is compared with some existing algorithms. Prasad and Chetty [9] propose a genetic algorithm (GA) as a heuristic for multilevel lot sizing, combined with the heuristic developed in this context, and invoking adaptive probabilities for crossover and mutation. The behaviour of the GA and other rules are compared with and without freezing the plan. Ouenniche and Boctor [10] present an efficient heuristic to solve the multi-product, multi-stage, economic lot-sizing problem. This method was compared to both the common cycle method and a reinforced version of the job-splitting heuristic. Connors et al. [11] describe a method based on a marginal allocation procedure which uses performance estimates from the queuing network model to determine the number of tools needed to achieve a target cycle time, with the objective being to minimize overall equipment cost. Ouenniche and Boctor [12] provide the two-group (TG) method to solve the multi-product, economic lot sizing and scheduling problem in flow shops.

Some scholars used simulation methodology to do the cycle time analysis. Byrne [13] proposed a framework in which a combined simulation and computer algorithm searched for the batch size for each individual product in a multi-product environment. The primary goal of his framework was to minimize the total production cost. Byrne and O'Grady [14] pointed out that different dispatching rules and setup costs would influence the best batch size determined by the cost model. Shanthakumar [15] derived the best batch size in a JIT environment using a simulation that included process capability and defect costs. Bonnin et al. [16] developed a design of experiments (DOE) based on dynamic simulation. They reduced cycle time by single-wafer or mini-batch strategy instead of traditional batch strategy. Nagaraj and Selladurai [17] provide a fuzzy logic model to calculate the economic batch sizes without changing the constraints of machine hour and labour productivity. Using Promodel, a simulation technique, the model was subjected to variable analysis and cost analysis and the results were compared. Savsar [18] proposes a simulation model for a JIT system in an assembly line for printed circuit boards (PCBs) to meet its final board inventory (FBI). The aim is to meet weekly scheduled demand on time to avoid additional cost of reshipments. Berkley investigates the effect of container size on average inventory and customer service levels in a two-card kanban system processing multiple part types. Simulation results show that smaller containers lead to smaller average total inventories [19]. Collins et al. [20] describe a generic 300 mm fabrication model containing 100 tool sets with 30 parallel tools in each set to simulation the environment of 300 mm semiconductor fabrication.

Most of the past studies regarding batch size concentrated on traditional manufacturing environments, with fixed demands and production rates. Most of these studies were focused on minimizing the production costs. Others considered product quality or minimized the lead time under some specific constraints. However, few researches analysed the impact of lot size and cycle time. This paper is motivated by a need of minimum effort to enhance the cycle time performance in manufacturing. Being different from the previous studies, the objective of this research is to develop a model which can find the optimal lot size for minimizing the cycle time under different bottleneck loading environments.

The remainder of this paper is organized as follows. Section 2 proposes the developed model. Simulation experiments based on realistic data from a Taiwan semiconductor fabrication are conducted in Sect. 3. Section 4 shows the experiment results and analysis.

Finally, conclusions are made in Sect. 5 with some future research directions.

2 Proposed simulated model

This paper proposes a simulated model for the analysis of lot sizing involved in deriving the optimal lot sizes under different bottleneck utilization conditions. The optimal lot size, which resulted in the minimal cycle time with respect to specific bottleneck utilization, is derived.

In this section, the lot size in one cassette is adjusted downward by one piece at a time from an initial lot size of 24 pieces. The details are discussed below. To obtain the optimal lot size, the steps of this model are presented in Fig. 1.

Step 1 Setting lot size factor under different conditions.
For each of the three bottleneck utilization conditions, the wafer releasing and dispatching rules are the same. For simplicity, but without loss of any generality, we assume the same dispatching rule for all types of machines.

Step 2 Execute simulation.
The simulation starts with initial parameters defined in step 1 at this stage.

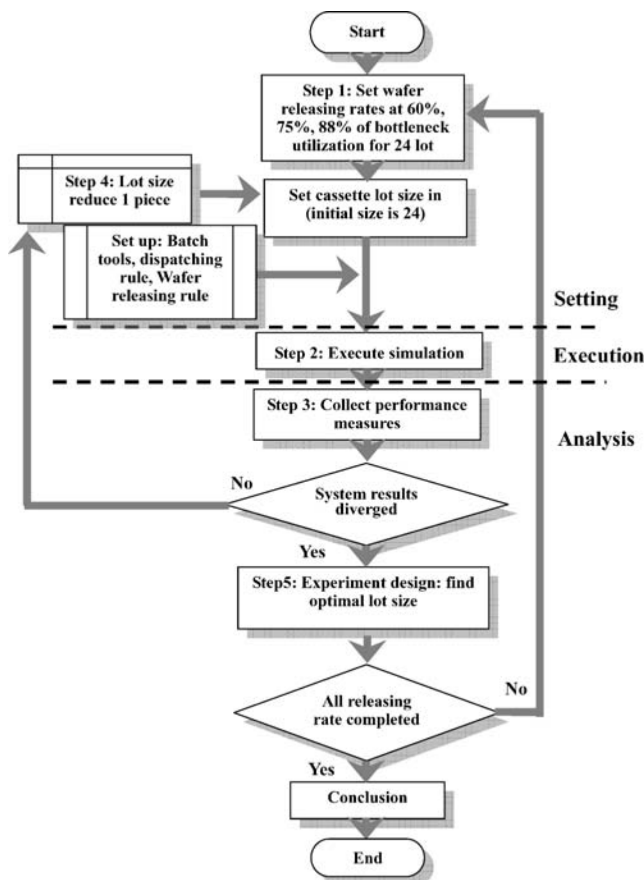

Fig. 1 Simulated model

Step 3 Collect data.
The performance measures including cycle time, WIP and utilization of bottleneck are collected. Since WIP and bottleneck utilization are the major impacts of cycle time, we monitor these three factors to check the changes.

Step 4 Reduce lot size by one piece of wafer and repeat from step 2.
The iterations from steps 2 to 4 repeat until the results of cycle time are divergent (i.e., the results are divergent when lot size has little change, and the cycle time increases dramatically) in simulation.

Step 5 Obtain the optimal lot size.
The optimal lot size for the minimal cycle time under each specific bottleneck loading level is derived.

When lot size is decreased, the WIP will become more balanced. Therefore, the bottleneck tool's utility will become higher than expected. For flexible dispatching and WIP unbalance impact, the bottleneck tool's utility could be different every day. Feedback from fabrication manufacturing managers points to a wafer releasing rate which could not be more than 88% of bottleneck utility. Here we define "wafer releasing rate" as the amount of daily wafer releasing to the fabrication divided by the average daily bottleneck tool's capacity. If wafer releasing rate is more than 88% of bottleneck utilization, the actual bottleneck utility will frequently exceed 100%. This result of managers' experience might be proven from simulation results in Sect. 4. When releasing rate is less than 60%, it is likely that no tools will have the chance to meet 100% utility; this means that no bottleneck will occur in this production line. To analyse the loading of bottleneck equipment, we set the value of 88% to be the upper loading level, and 60% to be the lower one. To compare the difference, we set the third loading level to be 70% (approximately the middle loading level between 88% and 60%). A total of three loading levels are set for bottleneck analysis.

3 Experimental design

The simulation is coded in "C" language followed by the structure of SLAM II, which is one of the popular event-oriented models of discrete simulation. For simplicity in modelling and analysis, some assumptions are made as follows:

1. To simplify the major issues, we will not include the analysis of cost in this study, since different cost assumptions will have different cost structure and will impact the results.

Table 1 Machine features

Machine type	Loading quantity	Process quantity	Process dependency	Ave. process time per lot	Machine category
A	One lot	Single wafer	Independent	$T=N_w*t_w$	Thin film
B	One lot	Single wafer	Dependent	$T=N_w*t_w+c$	Lithography
C	One lot	Single lot	Independent	$T=t_P$	Implanter
D	Several lots	Several lots	Independent	$T=t_P/N_l$	Furnace

T average process time per lot, N_w lot size, N_l quantity of lots, t_w single wafer processing time on bottleneck step within the machine, t_P machine processing time of one lot, c total processing time of all steps except the bottleneck one within the machine

2. Because a large fixed cost will take place when adjusting cassette lot size, continually changing lot size is infeasible and is not allowed.
3. Transportation time of lot delivery is neglected.
4. Hot lot and machine breakdown are not considered. Hot lot is defined as important lots for some special purposes, such as engineering verification, customers' special requests, etc. This kind of lot requires special handling.
5. Product mix will not vary during the simulated period.
6. Accessory resources (e.g., work force, transfer facility, wafer cassettes, etc.) are unlimited.
7. Characteristics of yields and reworks are not considered in this study.

Some machines can be operated in different processes. Different processes on one machine directly result in a different average processing time for each wafer or lot on that machine. This factor will also lead to cycle time fluctuation in determining lot sizing policy.

Semiconductor manufacturing has much different equipment. Gary and Costas introduce the semiconductor and manufacturing process and related equipment [21]. The features of changes in processing time on each machine due to different lot sizing policies are categorized as follows and summarized in Table 1:

1. Machine type A: one lot enters the machine at a time.
   Each individual wafer is processed independently. The machine (e.g., thin film machines) is capable of processing several wafers concurrently. The processing of one wafer does not depend upon the completion of other wafers so that the total processing time of the entire lot is proportional to the lot size.
2. Machine type B: one lot enters the machine at a time.
   Each individual wafer is processed accordingly. This type of machine processes several wafers simultaneously with a series of procedures. The processing time minus a constant is in proportion to the lot size. The lithography machine is this type of machine.
3. Machine type C: one lot enters the machine at a time.
   All wafers in a lot are processed together simultaneously. Instead of being proportional to lot size, the processing time is fixed. As compared to the previous two machine types, lot size reduction may result in a greater capacity loss on this type of machine. Lot size reductions involving these types of machines require greater attention. "Dry etching" and "implanter" are two examples of this type of machine.
4. Machine type D: several lots may enter the machine at a time.
   The processing time is fixed and is not related to the quantity of wafers and lots. In order to maximize the throughput, the turn ratio and utilization of this type of machine should be carefully analysed, like furnace machines.

The realistic data was simplified from the original data, which was provided by a wafer fabricator in Taiwan. The pertinent machine data and process flow data are given in Tables 2 and 3. One machine might operate different processes. A machine group consists of several of the same type of machines grouped together and set up to operate one special process function. During route process flow, a process function is called a "stage" which is widely used in the semiconductor industry.

Here, we assume X, Y, and Z are three different products with different process routes. The mix of products X, Y, and Z is 1:1:1 and each experiment scenario runs 30 times with common random number streams and conducts for 540 days. The first 180 days served as the warm-up period.

Table 2 Machine related data

Machine group	Number of machines	Process time (hr)	Fixed setup time (hr)	Machine type
1	9	0.85	0.02	B
2	9	5	0.05	D
3	10	4	0.05	D
4	8	0.5	0.02	A
5	10	2	0.02	A
6	5	0.76	0.02	A
7	8	1	0.02	C
8	6	1.5	0.05	A

Table 3 Route data of products

Stage #	Product X	Product Y	Product Z	Machine group	Stage #	Product X	Product Y	Product Z	Machine group
1	*	*	*	4	45	*			1
2	*	*	*	1	46	*			4
3	*	*	*	4	47	*			6
4	*	*	*	6	48		*	*	4
5	*	*	*	2	49		*	*	3
6	*	*	*	7	50	*	*		1
7	*			3	51	*	*		7
8	*			4	52	*	*		4
9	*			1	53	*	*		3
10	*			4	54	*	*	*	1
11	*			6	55	*	*		3
12		*	*	2	56	*	*		5
13		*	*	3	57	*	*		7
14	*	*		1	58	*			1
15	*	*		7	59		*	*	4
16	*	*		4	60	*	*	*	8
17	*	*		3	61	*	*		5
18	*	*	*	1	62	*	*	*	1
19	*	*	*	4	63	*	*	*	4
20	*	*	*	1	64	*	*	*	2
21	*	*	*	4	65		*		7
22	*	*	*	6	66	*	*	*	1
23	*	*	*	2	67	*	*	*	8
24	*	*	*	7	68			*	5
25	*			3	69	*	*	*	1
26	*			4	70	*	*	*	5
27	*			1	71	*	*	*	4
28	*			4	72	*	*		5
29	*			6	73	*	*		7
30		*	*	4	74	*			1
31		*	*	3	75		*	*	4
32	*	*		1	76	*	*	*	8
33	*	*		7	77	*	*		5
34	*	*		4	78	*	*	*	1
35	*	*		3	79	*	*	*	4
36	*	*	*	1	80	*	*	*	2
37	*	*	*	3	81		*		7
38	*	*	*	1	82	*	*	*	1
39	*	*	*	4	83	*	*	*	8
40	*	*	*	6	84			*	5
41	*	*	*	2	85	*	*	*	1
42	*	*	*	7	86	*	*	*	5
43	*			3	87	*	*	*	4
44	*			4					

* product would be processed in this stage

4 Analysis of results

The results of the simulation experiments are summarized in this section. The optimal lot sizes under different system loading levels are derived.

1. The optimal lot sizes under different wafer releasing rates can be obtained. The optimal lot sizes and their

Table 4 Cycle time reduction

Variables	Values		
Cycle time (lot size=24)	127.45	131.79	136.01
Optimal lot size	10	12	16
Cycle time (optimal lot size)	113.51	118.7	126.49
Percentage of reduction	10.94%	9.93%	7.00%

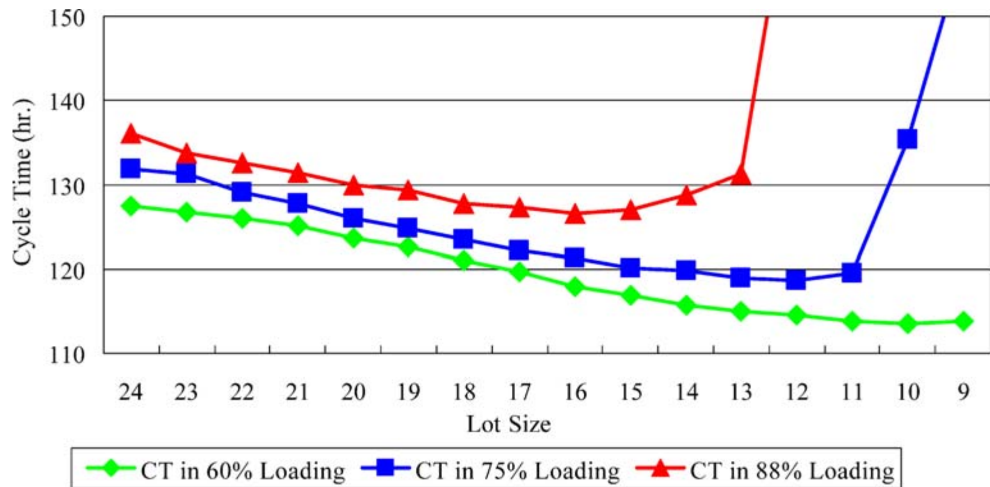

Fig. 2 Cycle time under different lot sizes

corresponding cycle times at three wafer releasing levels are shown in Table 4. As compared with the average cycle time at a lot size of 24, average cycle time reduction percentages are 10.94%, 9.93%, and 7.00% for the loading levels of 60%, 70% and 88%, respectively. The lower the system loading level, the smaller the lot size that can be implemented and the shorter the cycle time that can be obtained.

2. The lot size with the shortest corresponding cycle time is picked as the best one in this study. They are 10, 12, and 16 for wafer releasing levels at 60%, 75%, and 88% of bottleneck capacity, respectively (see Fig. 2). The cycle time of the corresponding optimal lot size is associated with the corresponding wafer releasing level. The curve of the cycle times to the corresponding lot sizes is plotted in Fig. 2. It can be seen that the greater the excess capacity, the smaller the lot size that can be applied, and the shorter the cycle time which can be obtained. The simulation results for whole system are shown in Table 5.
3. While the lot size becomes smaller, the bottleneck utilization will increase under the same wafer releasing rate, as shown in Fig. 3. This is because greater setup consumes more bottleneck capacity. This condition will influence the cycle time to become bigger.
4. The WIP drops as the bottleneck loading is reduced. The WIP increases drastically when the lot size is continually adjusted downward after reaching 10 and 12 for bottleneck loading of 75% and 88%, respectively, (see Fig. 4). This is because the C type machine, defined in Sect. 3, is overloaded. The C type machine thus becomes the new bottleneck for the entire system.

Table 5 Average cycle time under various bottleneck loading

	Cycle time			Actual bottleneck util.			WIP		
Bottleneck loading Lot size	60%	75%	88%	60%	75%	88%	60%	75%	88%
24	127.45	131.79	136.01	0.6097	0.7447	0.8732	1144.3	1443.6	1745.2
23	126.74	131.31	133.71	0.6136	0.7521	0.8766	1139.6	1440.7	1718.7
22	125.93	129.1	132.56	0.6213	0.7552	0.884	1138.2	1423.2	1712.8
21	125.15	127.71	131.41	0.6272	0.7618	0.8946	1135.4	1414.1	1703.5
20	123.6	125.96	129.89	0.6281	0.7635	0.8978	1119.7	1391.2	1681.2
19	122.65	124.81	129.28	0.6374	0.7786	0.9121	1122.2	1392.4	1689.6
18	121.04	123.42	127.77	0.6402	0.7815	0.913	1101.8	1370.1	1662.1
17	119.63	122.19	127.3	0.6491	0.791	0.9263	1097	1367.4	1668.3
16	117.97	121.32	126.49	0.6517	0.8003	0.9337	1084.2	1359.3	1660.3
15	116.89	120.17	127	0.6645	0.8089	0.9468	1077.8	1351.1	1672.4
14	115.76	119.78	128.8	0.6731	0.8197	0.9623	1069.2	1349.3	1699.2
13	114.92	118.96	131.18	0.6808	0.8287	0.9727	1063	1341.4	1732.9
12	114.47	118.7	170.93	0.6959	0.8451	0.9911	1064	1345.7	2268.7
11	113.86	119.48	*	0.7095	0.8631	*	1059.6	1356.2	*
10	113.51	135.29	*	0.7226	0.8836	*	1062.1	1543.4	*
9	113.84	*	*	0.7435	*	*	1067.1	*	*

* divergent results

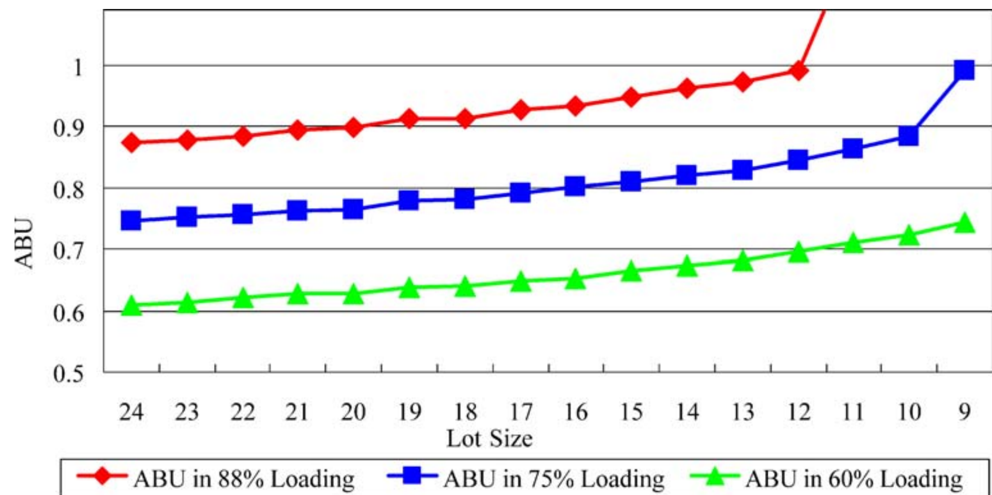

Fig. 3 Actual bottleneck utilization (ABU) under different lot sizes

This result indicates that a new bottleneck may emerge due to extra setups in reducing the lot size. In this kind of condition, the cycle time will increase drastically as well.

5. Some possible advantages and disadvantages of lot size reduction in wafer fabrication are summarized as follows.

Advantages:

(a) Reduced manufacturing cycle time.
(b) Lower WIP level, resulting from a shorter manufacturing cycle time.
(c) Increased on-time delivery due to smaller cycle time variance under a lower WIP level.
(d) Improved customer service because of a smaller allowable customer order volume.
(e) Increased capability of quick response to market demands and changes.
(f) Shorten the lead time of new products to market.
(g) Increased yield due to shorter manufacturing cycle time.
(h) Lower production risks and costs with less scrap and rework.

Disadvantages:

(a) Loss of capacity due to the increase in the number of fixed setups.
(b) More engineering experiments for tuning process parameters.
(c) Increased wafer lots with smaller lot sizes in the shop which complicates the dispatching decisions and increases the transporter load.
(d) Wasted specific batch equipment capacity (e.g. etcher).
(e) More inspections.

5 Conclusions

Differing from previous studies, this research conducts a thorough analysis of the effect of lot sizing for cycle time reduction in wafer fabrication. A simulation model is

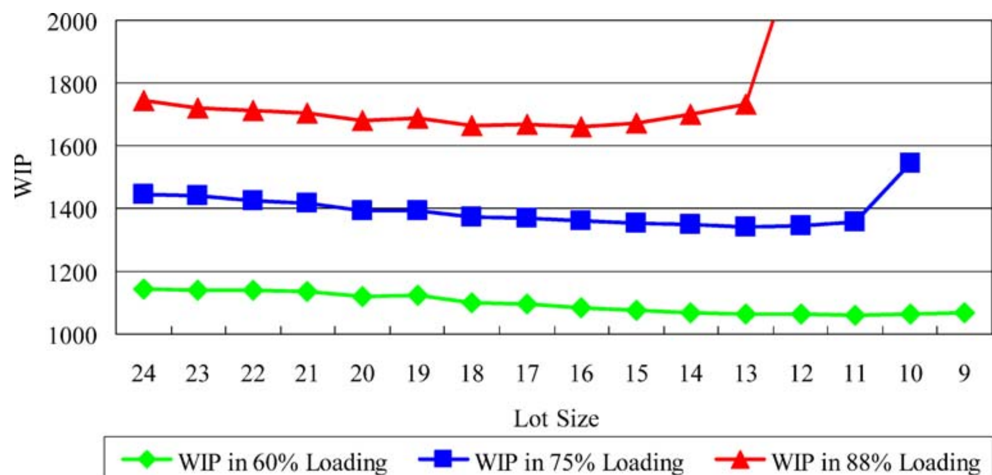

Fig. 4 WIP under different lot sizes

proposed. The optimal lot sizes under different loading levels are determined through simulation experiments. The sensitivity of each optimal lot size to bottleneck usage level variations is analysed as well. It is found that a smaller optimal lot size could be applied if greater excess bottleneck utilization existed, which would result in a shorter cycle time. Through the sensitivity analysis, the cycle time of the corresponding optimal lot size is shorter than that of the 24 piece wafer production system, within a specific range of demand (bottleneck utilization) variations. In a lower system-loading environment, the superiority of cycle time performance at the corresponding optimal lot size is sustained for a wider range of demand changes. The model can help fabrication managers obtain optimal lot sizes in different bottleneck situations to effectively reduce product cycle time.

It should be noted that the total processing time on batch machines in the case example was about 60% of the total raw processing time. As mentioned in Sect. 3, cycle time in a batch machine can not be improved through lot size policy. That is, the portion that the lot sizing policy can help in cycle time reduction is only 60% of the entire system. If the total processing time on batch machines can be further reduced, the improvement of cycle time will be much greater than that illustrated in this paper.

The approach and analysis of results were discussed in a forum with several industrial managers and their feedback was sound. Lot size changes may have a big impact for fabrication; but they still require more time to study impacts and actions needed for this method.

In this research, we conducted a study of lot size policies for cycle time reduction in wafer fabrication. Further research will indeed contribute to this highly competitive environment by applying this method to analyse 300 mm fabrication or following the global semiconductor standard to check the differences and impacts. Moreover, more realistic simulation models could be considered as well, such as lot transportation time, costs and inspection time.

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