行政院國家科學委員會專題研究計畫 成果報告

次32奈米多重閘極元件的特性分析與模式建立-變異性與微縮性，高頻類比特性，以及介觀現象的探討
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行政院國家科學委員會補助專題研究計畫 ■ 成 果 報 告
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次 32 奈米多重閘極元件的特性分析與模式建立

計畫類別：■ 個別型計畫　　□ 整合型計畫
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執行單位：國立交通大學電子工程學系

中　華　民　國　98　年　07　月　31　日

次 32 奈米多重閘極元件的特性分析與模式建立
Investigation and Modeling of Sub-32 nm Multiple-Gate SOI CMOS

計畫編號 : NSC 97-2221-E-009-162
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一、中文摘要

在本計畫中我們對次 32 奈米多重閘極 SOI CMOS 的元件特性作深入研究與模式建立。由於傳統 CMOS 在次 32 奈米製程的困難日增，多重閘極 SOI CMOS 元件提供了一種有利於 CMOS 微縮的解決之道。在本計畫中我們對 Schrodinger 方程式考慮短通道元件的位能井，利用求得的解析解來預測短通道環閘極(Gate-All-Around)元件的量子侷限效應。此外，針對多重閘極元件，在 56K 至 300K 溫度範圍間，比較並分析載子傳輸在重疊與非重疊閘源(汲)極結構中的差異。本計畫對次 32 奈米多重閘極元件所發展的元件模型，不僅對使用此前瞻技術的電路設計極為重要，也有益於此前瞻元件設計的最佳化。

關鍵詞 :
SOI CMOS，多重閘極，元件設計，電路設計，元件模型，載子傳輸，重疊/非重疊閘源(汲)極，量子侷限效應，奈米電子

Abstract

In this project we have conducted investigation and modeling of sub-32nm multiple-gate SOI CMOS. We have proposed an analytical model considering quantum confinement effects in short-channel gate-all-around MOSFETs under subthreshold region. In addition, we have conducted a comparative study of carrier transport characteristics for multi-gate FinFET MOSFETs with and without the nonoverlapped source/drain structure. Our study will be instrumental for ultra-scaled multi-gate device/circuit designs.

Keywords :
SOI CMOS, multiple gate, nanowire, device design, carrier transport, nonoverlapped, overlapped, quantum confinement, silicon nanoelectronics

二、計畫目的及研究方法

As the semiconductor industry is confronted with the difficulty of downsizing the transistor dimension, multiple-gate SOI is emerging as an important device structure for CMOS scaling [1]. In this project, we have conducted investigation and modeling for sub-32nm multi-gate SOI CMOS. This report describes our two main tasks regarding multi-gate research during this project:

Task I: Analytical Quantum Confinement Model for Short-Channel Gate-All-Around MOSFETs Under Subthreshold Region [9]

Task II: A Comparative Study of Carrier Transport for Overlapped and Nonoverlapped Multiple-Gate SOI MOSFETs [23]

Task I

Gate-All-Around (GAA) MOSFET is an ideal structure to provide superior electrostatic behavior and is recognized as an important candidate for ultimate CMOS scaling [2]-[4]. As the channel thickness of GAA MOSFETs scales down, the quantum confinement effects become significant. This two-dimensional confinement effect is often considered to be independent of the carrier flow direction (i.e., channel length direction). Thus, the quantum

confinement model for long-channel and undoped cylindrical GAA MOSFETs was proposed using the flat well approximation [4], [5]. For short-channel devices, however, the center of the potential well is altered by the source/drain coupling due to the short channel effect and the flat well approximation is no longer valid. An accurate quantum confinement model considering the short channel effects is crucial to GAA MOSFET design.

In this work, an analytical solution of Schrödinger equation for short-channel GAA MOSFET under the subthreshold region is proposed. The subthreshold behaviors represent the device electrostatic integrity that is important for ultra-scaled device design. Besides the lightly-doped GAA MOSFETs, our analytical model can also be used for heavily-doped devices.

Task II

Multi-gate silicon-on-insulator (SOI) MOSFET (MuGFET) structures provide superior electrostatic integrity needed for MOSFET scaling entering the deca- to nanometer regime [1]. For MuGFET device design, source/drain engineering is crucial because of the parasitic drain/source resistance [6] and the parasitic fringing/overlap capacitance that may limit circuit performance [7]. Two options in the source/drain engineering are the overlapped structure with light-doping-drain/source (LDD/LDS) and the nonoverlapped structure. Whether the various source/drain engineering will impact the carrier transport in nanoscale MuGFETs merits examination.

In this work, we conduct a systematic comparison of carrier transport between overlapped and nonoverlapped multi-gate SOI MOSFETs. The investigation has included measurements from T = 300 K to 56 K.

三、結果與討論

1. Analytical Quantum Confinement Model for Short-Channel Gate-All-Around MOSFETs Under Subthreshold Region [9]

Fig. 1 shows a schematic sketch of the GAA MOSFET structure. The eigen-energy and eigen-function of channel carriers are crucial to the quantum confinement effect, and they can be determined by solving the Schrödinger equation. The conduction band edge needed in the Schrödinger equation can be obtained from the channel potential solution of Poisson's equation. We have derived the channel potential solution for GAA MOSFETs in the subthreshold region [8], and the verification with the TCAD simulation is shown in Fig. 2. The channel potential solution can be further reduced to the parabolic form to simplify the solution of the Schrödinger equation. Thus, the Schrödinger solutions for short-channel GAA MOSFETs under the subthreshold region can be analytically derived [9]. Using the calculated eigen-energies and eigen-functions, we can calculate the electron density in the channel. The impact of quantized eigen-energies and eigen-functions on the electron density is incorporated into the effective density of states for conduction band [10].

Fig. 3 shows the calculated quantized jth eigen-energy (E_j) and the square of jth eigen-function ($|\Psi_j|^2$) for lightly-doped long-channel GAA devices, and the results are verified with TCAD simulation that numerically solves the self-consistent solution of 3-D Poisson and 2-D Schrödinger equations [11]. It can be seen that E_j and the difference between two distinct eigen-energies increase with decreasing channel diameter (D). Due to the cylindrical symmetry in the θ direction, the E_2 and E_3 are degenerate because they correspond to the states of angular quantum number l = 1 and -1. Similarly, the E_4 and E_5 are degenerate. The results in Fig. 3 can also be predicted by the quantum confinement model using the flat

well approximation [4], [5]. For short-channel lightly-doped GAA devices, however, the conduction band edge E_C is lowered by source/drain coupling and is bended from a flat well to a parabolic-like well (Fig. 4). Since the E_C is not spatially constant for short-channel devices, we choose the E_C at the channel center (r = 0) as the reference energy. Fig. 4 shows that the E_j's can be correctly predicted by our analytical solution considering the short-channel potential barrier. Fig. 5(a) shows that the lowest eigen-energy (E_1) increases as channel length decreases. This eigen-energy shift results from the bending of E_C due to the short channel effect. Fig. 5(b) shows that the square of lowest eigen-function ($|\Psi_1|^2$) for short-channel lightly-doped device is more centralized to the channel center. This is because the E_C barrier at the channel center (r = 0) is lower than that near the insulator/channel interface (r = D/2), and the electron density becomes larger at r = 0. Fig. 6 shows that the E_1 increases with V_{DS}. In other words, the drain-induced-barrier-lowering (DIBL) increases the E_C bending and affects the quantum confinement effects.

Our analytical model can also be used to assess the impact of quantum confinement on heavily-doped GAA MOSFETs. Similar to the lightly-doped short-channel devices, the E_C of heavily-doped devices can be described by the parabolic form. In contrary to the upward bending of E_C in the lightly-doped case, the E_C bends downward for heavily-doped devices. Fig. 7 shows that the E_C for long-channel heavily-doped GAA device shapes the potential well near the interface (r = D/2). Therefore, we choose the E_C at r = D/2 as the reference energy for long-channel GAA devices. Fig. 8(a) shows that the E_1 of long-channel GAA devices increases with channel doping. This is because as the channel doping increases, the surface electric field increases and hence the bending of E_C at the interface is increased. As a result, the E_1 increases due to the stronger electrical confinement. Besides, it can be seen that for heavily-doped channel (e.g., $5\times10^{18}cm^{-3}$), the E_1 increases with increasing channel diameter, which is contrary to the lightly-doped case (e.g., $1\times10^{15}cm^{-3}$). This is because for heavily-doped devices, the electrical confinement becomes stronger with increasing channel diameter, as shown in Fig. 8(b).

Fig. 9 compares the electron density distribution calculated from the classical model [8] and the quantum confinement model. It can be seen from Fig. 9(a) that for lightly-doped short-channel GAA MOSFET, the electron density near the interface (r = D/2) predicted by the quantum confinement model is smaller than classical model. Fig. 9(b) shows that for heavily-doped long-channel GAA MOSFET, the peak electron density predicted by the quantum confinement model is away from the interface, while the classical model predicts the highest electron density at the interface. Fig. 10 compares the average electron density at $y = 0.5L_{eff}$ calculated from the classical model and the quantum confinement one for lightly-doped short-channel devices. It can be seen that the discrepancy becomes larger with reducing channel diameter.

In conclusion, we have proposed an analytical model for quantum confinement effects in GAA MOSFETs under the subthreshold region. The Schrödinger equation is solved considering the bended potential well of parabolic form. Our analytical model accurately predicts the impact of short-channel effects on the eigen-energy and eigen-function of GAA devices. This short-channel quantum-confinement model is crucial to the ultra-scaled GAA MOSFETs design.

2. A Comparative Study of Carrier Transport for Overlapped and Nonoverlapped Multiple-Gate SOI MOSFETs [23]

Fig. 11(a) shows a schematic view of the multi-gate SOI MOSFET investigated in this study. Note that the LDD/LDS implantation was performed for the overlapped structure [Fig. 11(c)] and was skipped for the nonoverlapped structure [Fig. 11(b)]. In this study, we compare these two types of devices based on the same effective source-drain length L_{eff} .

Current-voltage measurements ($I_{DS} - V_{GS}$) at V_{DS} =50mV under T =300K to 56K were performed for the overlapped device 1 with W_{fin} = 25nm and L_g = 80nm (Fig. 12) and for the nonoverlapped device 2 with W_{fin} = 25 nm and L_g = 30 nm (Fig. 13). Fig. 12 shows that the subthreshold swing S for the overlapped device 1 decreases with temperature. We have confirmed that the S–T characteristic follows the Boltzmann law $S = n(k_BT/q) \ln (10)$ with the body effect coefficient $n \approx 1.16$. The linear temperature dependence of S is a feature of fully depleted SOI [12] and has also been observed in trigate SOI MOSFETs [13]. For the nonoverlapped device 2, however, the linear temperature dependence of S can only be seen when temperature is higher than 223 K (Fig. 13). For temperature below 223 K, S is constant and does not follow the Boltzmann law. This suggests that for the nonoverlapped device 2, tunneling current dominates the fundamental limitation of leakage current instead of the thermal current [14]. We have noted that similar S behavior has been reported at T < 100 K for the planar nonoverlapped nMOSFET in [14]. It implies that the leakage current associated with thermionic emission is suppressed in our MuGFET. The insensitive temperature dependence of I_{DS} can also be found in the strong inversion region for the nonoverlapped device 2 (Fig. 13). In contrast to that of the overlapped device 1 (Fig. 12), the I_{DS} for V_{GS} > 0.6V is nearly independent on temperature. These results indicate that carrier transport in the strong inversion region is determined by the phonon-limited mobility for the overlapped device 1, but not for the nonoverlapped device 2. To further compare the carrier transport characteristics for overlapped and nonoverlapped devices, we have investigated channel conductance ($G_{DS} = I_{DS}/V_{DS}$) with low V_{DS}. Fig. 14 shows the measured G_{DS} versus V_{GS} characteristics for the overlapped device 3 with W_{fin} = 10 nm and L_g = 60 nm. Significant G_{DS} fluctuations can be seen at T = 56 K [Fig. 14(a)]. Similar G_{DS} fluctuations have been reported in [15] and attributed to the intersubband scattering. While the number of populated subbands increases with increasing V_{GS}, the intersubband scattering also increases with each new subband [16]. In other words, when V_{GS} increases, the G_{DS} increases due to new populated subbands and then decreases due to the mobility reduction (i.e., the increase of intersubband scattering). Thus, fluctuations can be seen in the $G_{DS} - V_{GS}$ characteristics. We have noted that the G_{DS} fluctuations almost occur at the same V_{GS}, such as the spike at $V_{GS} - V_T = 0.425$ V [Fig. 14(a)]. We have also noted that for the wider overlapped devices (i.e., device 1) with negligible subband splitting, the G_{DS} fluctuations can not be found.

For the nonoverlapped device 2 in the high V_{GS} regime, the G_{DS} increases with V_{DS} and temperature as can be observed in Fig. 15(a) and (b), respectively. Such V_{DS} and temperature dependence of G_{DS} are completely opposite to that of the overlapped device 3 (Fig. 14) and cannot be ascribed to the intersubband scattering effect. In addition, Fig. 15 also shows interesting fluctuations with negative differential resistance in the G_{DS}. Although the G_{DS} fluctuations in Fig. 15 were observed in the same measurement conditions as Fig. 14, one can safely state that it does not result from the intersubband scattering.

Fig. 16 shows the electronic potential calculated using ISE device simulation [17] for our nonoverlapped device. The nonoverlapped gate to source/drain regions act as the voltage-controlled potential barriers along the channel. Therefore, carrier transport from source to drain is significantly influenced by the barriers as illustrated in Fig. 16: directly tunneling (I_a), thermally associated tunneling (I_b), and thermionic emission (I_c). The contribution of these three mechanisms to I_{DS} depends on V_{GS} and temperature. For high V_{GS}, I_a is dominant. With decreasing V_{GS}, increased electronic potential diminishes I_a and thus I_b and I_c become important. In other words, I_{DS} in the subthreshold region results mainly from I_b and I_c for the nonoverlapped device. It is worth noting that carrier transport by I_c requires more thermal energy and may be suppressed under low temperature. Fig. 17 shows the temperature sensitivity of $I_{DS}(\Delta\log(I_{DS})/\Delta T)$ versus V_{GS} characteristics extracted from Figs. 12 and 13 under high and low temperatures. For the nonoverlapped device in the strong inversion region, the insensitive temperature dependence manifests the importance of I_a. On the other hand, the negative temperature dependence for the overlapped device in the strong inversion region indicates phonon scattering. In addition, it can be noted in Fig. 17(a) that $\Delta\log(I_{DS})/\Delta T$ significantly increases with decreasing V_{GS} for both overlapped and nonoverlapped devices. This suggests that in the high temperature regime the subthreshold current of the nonoverlapped device is dominated by I_c, similar to the overlapped device. When temperature decreases, however, the thermionic emission I_c is suppressed and the I_b component with weak temperature dependence becomes dominant. In other words, the suppression of I_c under low temperature is the main reason of S saturation for the nonoverlapped device. It should be noted that such mechanism of S saturation is different from lateral tunneling through the channel, as presented for ultrashort devices in [14] and [18].

Fig. 16 also shows an equivalent quantum well under the gate in the nonoverlapped device [14]. It is worth noting that the height of the voltage-controlled potential barriers in the nonoverlapped regions increases with V_{GS}. The consequence is the plausibility of electron-wave confined between the barriers. When the length of the quantum well, d, is smaller than the inelastic-scattering (e.g., phonon scattering) length, the phase-coherent electron wavefunction over the entire channel as well as quantum interference between coherent electronwaves occur. The quantum interference enhances the electron backscattering probability [19], [20] and thereby reduces the conductivity expected classically. Such quantum correction to the conductivity is the weak localization effect [19], [20] and logarithmically dependent on temperature as $\Delta\sigma = (pe^2/\pi h)\ln(T)$, where the value of p depends on the scattering process. When T = 56 K, the carriers at V_{DS} = 50 mV experience more heating (more phonon scattering) and thus less localization effect than those at V_{DS} = 1 or 2 mV. Therefore, the G_{DS} measured at V_{DS} = 50 mV is larger than that at V_{DS} = 1 or 2 mV (Fig. 15). From the G_{DS} data at V_{DS} = 2 mV under T = 56 K and 223 K in Fig. 15, we can estimate that $p \approx 1$, which is close to the results in [21] for the 2-D electron gas in Si MOSFETs.

The quantum-mechanical interference for an electron wave passing through a quantum well also results in oscillating transmission probability. Fig. 18 shows the calculated T_r for the quantum well in Fig. 16. The values of d and $(E - eV_p)$ used in Fig. 18 are based on our experiments. It is worth noting that the T_r oscillation becomes obvious with increasing V_{GS} as well as the depth of the quantum well. From the T_r calculation based on d = 30 nm and $(E - eV_p) = 0 - 5$ meV (Fig. 18), we can observe three transmission maxima due to constructive interference (i.e., $T_r = 1$) at $V_{GS} \approx$

0.2, 0.43, and 1 V. When ($E - eV_p$) increases, we observed smaller T_r oscillations and shifts in the corresponding transmission maximum. In other words, the electron energy distribution may result in group-like T_r oscillations as shown in the groups 1–3 of Fig. 18. We found that such group-like fluctuations can also be seen in the G'_m ($G'_m = dG_m/dV_{GS}$, $G_m = dI_{DS}/dV_{GS}$) characteristics in Fig. 19 as well as in the G_{DS} characteristics shown in Fig. 15(a). We have noted that nearly every peak in G'_m (Fig. 19) can correspond to the peak in G_{DS} [Fig. 15(a)]. It is worth noting that the G'_m oscillation of Group 3 is more significant and wider than that of groups 1 and 2, which is consistent with the simulation results in Fig. 18. Remind that both the potential barrier height in Fig. 16 and G_{DS} fluctuations in Figs. 15 and 19 increase with V_{GS}. For devices with the same size, similar G'_m oscillations can also be observed and have been presented in our previous study [22].

In conclusion, we have conducted a comparative study of carrier transport characteristics for MuGFETs with and without the nonoverlapped source/drain structure. For the overlapped devices, we observed Boltzmann law in subthreshold characteristics and phonon-limited behavior in the inversion regime. For the nonoverlapped devices, however, we found insensitive temperature dependence of I_{DS} in both subthreshold and inversion regimes. Our low-temperature measurements indicate that the intersubband scattering is the dominant carrier transport mechanism for narrow overlapped MuGFETs. For the nonoverlapped MuGFETs, the voltage-controlled potential barriers in the nonoverlapped regions may give rise to the weak localization effect (conductance reduction) and the quantum interference fluctuations.

四、計畫成果自評

In this project we have conducted investigation and modeling of sub-32nm multiple-gate SOI CMOS. We have presented an analytical model for quantum confinement effects in short-channel GAA MOSFETs under the subthreshold region. In addition, we have conducted a comparative study of carrier transport characteristics for multi-gate MOSFEs with and without the non-overlapped source/drain structure. Our study will be instrumental for ultra-scaled multi-gate device/circuit designs.

Our essential results for the multi-gate project have been disseminated through research reports in referred journals [9][23][27] and international conference proceedings [24]-[26] as well as used in education of our graduate students to become leading researchers in silicon-based nanoelectronics.

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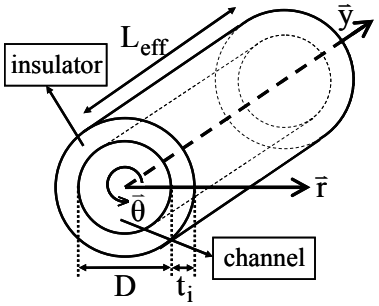

Fig. 1. Schematic sketch of the GAA structure investigated in this study. The origin point (r = 0, y = 0) is defined at the center of the channel/source junction.

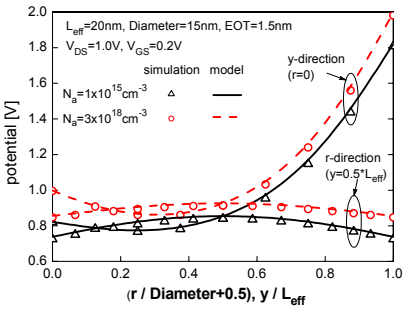

Fig. 2. Analytical potential distribution of GAA MOSFETs compared with TCAD simulation. A midgap workfunction 4.5eV is used.

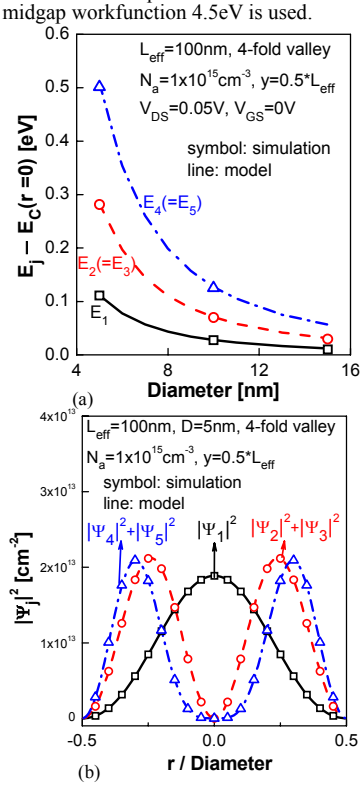

Fig. 3. (a) Quantized eigen-energies for long-channel lightly-doped GAA devices. (b) The square of wavefunctions corresponding to the eigen-energies of GAA device with D=5nm in (a).

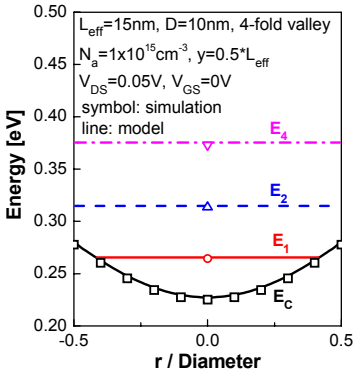

Fig. 4. Conduction band edge and quantized eigen-energies of a short-channel lightly-doped GAA device.

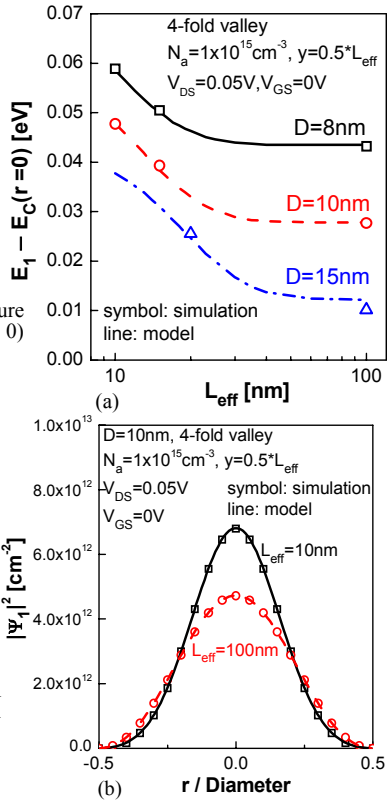

Fig. 5. (a) Channel length dependence of the first eigen-energy for lightly-doped GAA devices with various channel diameter. (b) Comparison of the square of first eigen-function for long-channel and short-channel GAA MOSFETs.

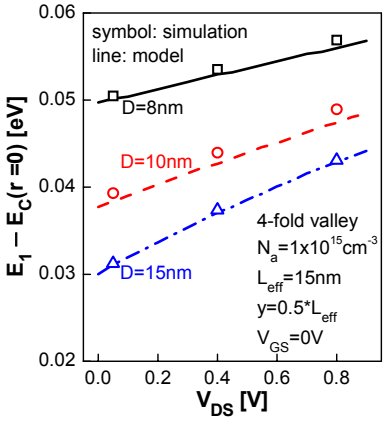

Fig. 6. Drain bias dependence of the first eigen-energy of short-channel lightly doped GAA devices with various channel diameter.

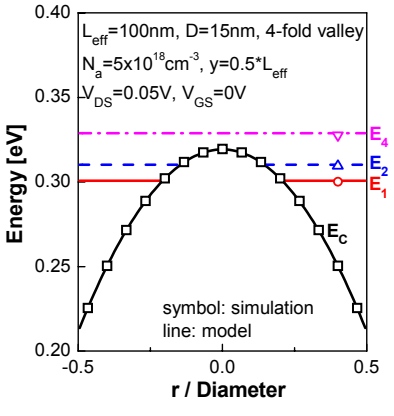

Fig. 7. Conduction band edge and quantized eigen-energies of a long-channel heavily-doped GAA device.

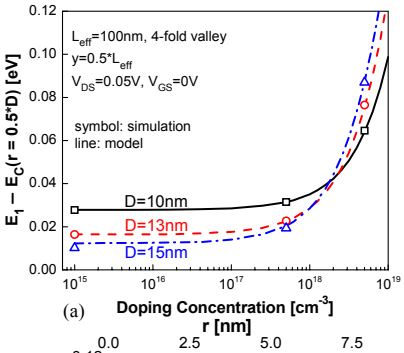

Fig. 8. (a) Impact of channel doping on the first eigen-energies of long-channel GAA devices with various channel diameter. (b) The first eigen-energies and conduction band edges of heavily-doped GAA devices with D = 13nm and D = 15nm, respectively.

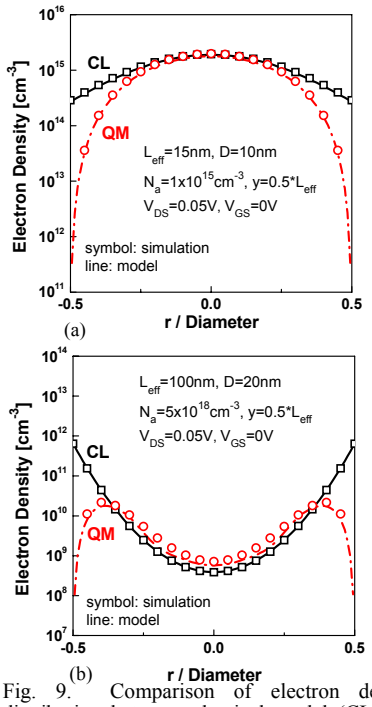

Fig. 9. Comparison of electron density distribution between classical model (CL) and quantum confinement model (QM). (a) Lightly-doped short-channel GAA device. (b) Heavily-doped long-channel GAA device.

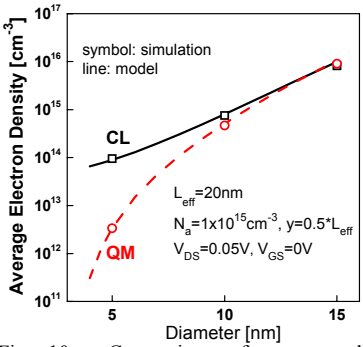

Fig. 10. Comparison of average electron density between CL model and QM model for lightly-doped short-channel GAA MOSFETs with various channel diameter.

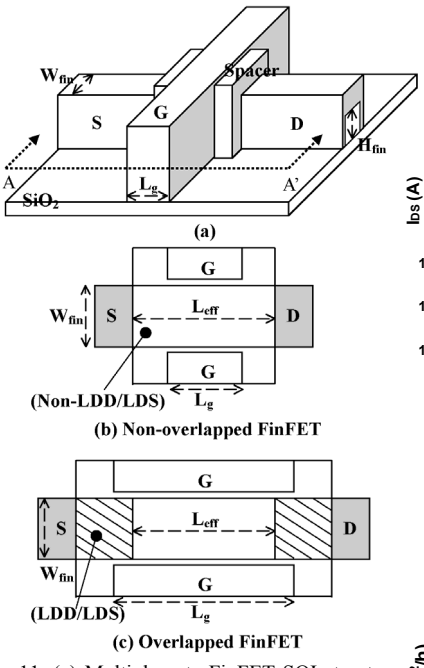

Fig 11. (a) Multiple-gate FinFET SOI structure investigated in this work and its cross-sectional AA' view along the channel direction showing (b) nonoverlapped gate to source/drain structure and (c) overlapped gate to source/drain structure.

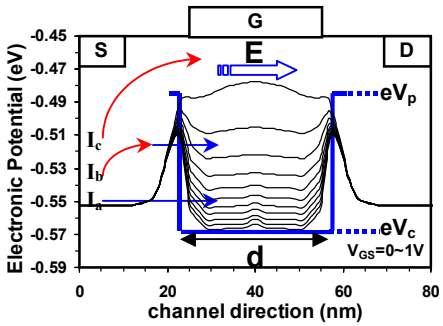

Fig 16. Calculated electronic potential for the nonoverlapped gate to source/drain structure at V_{GS} = 0V to 1 V. V_p : peak potential value in the nonoverlapped region. V_c : potential value at the channel center. E: carrier energy. d: width of the effective quantum well. I_a : direct tunneling through the potential barrier of the nonoverlapped region. I_b : thermally associated tunneling. I_c : thermionic emission.

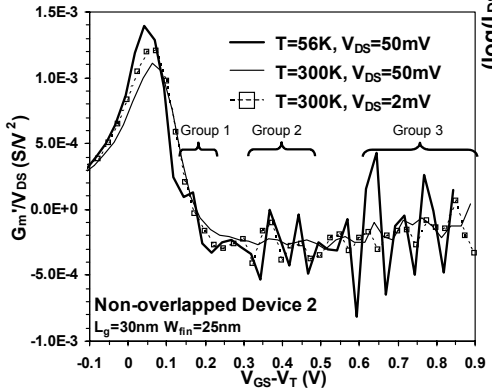

Fig 19. Measured G'_m/V_{DS} versus (V_{GS}–V_T) characteristics for the nonoverlapped device 2 with L_g = 30 nm and W_{fin} = 25 nm at various V_{DS} and temperature. ($G'_m = dG_m/dV_{GS}$ and $G_m = dI_{DS}/dV_{GS}$).

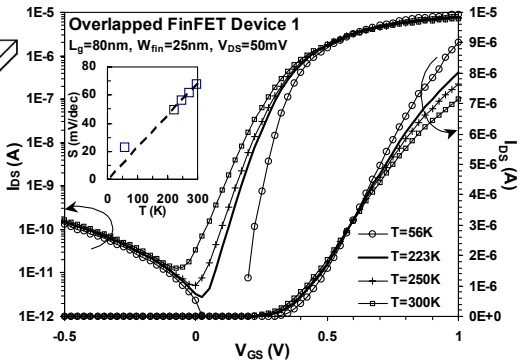

Fig 12. Measured I_{DS} versus V_{GS} at V_{DS} = 50 mV under T = 300 to 56 K for the overlapped FinFET device 1 with W_{fin} = 25 nm and L_g = 80 nm.

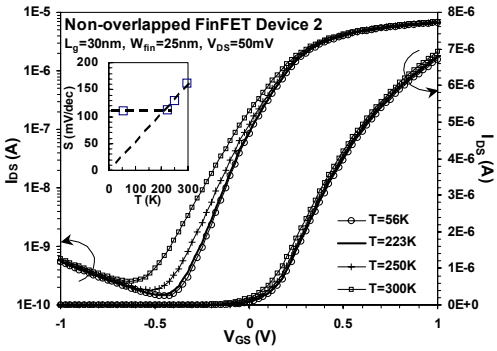

Fig 13. Measured I_{DS} versus V_{GS} at V_{DS} = 50 mV under T = 300 to 56 K for the nonoverlapped FinFET device 2 with W_{fin} = 25 nm and L_g = 30 nm.

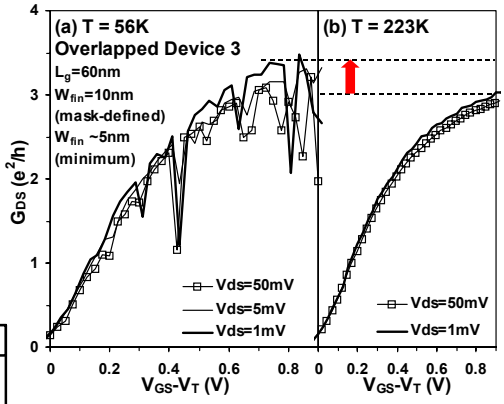

Fig 14. Measured channel conductance (G_{DS}) versus (V_{GS}–V_T) characteristics for the overlapped device 3 with L_g = 60 nm and W_{fin} = 10 nm at various V_{DS} under (a) T = 56 K and (b) T = 223 K.

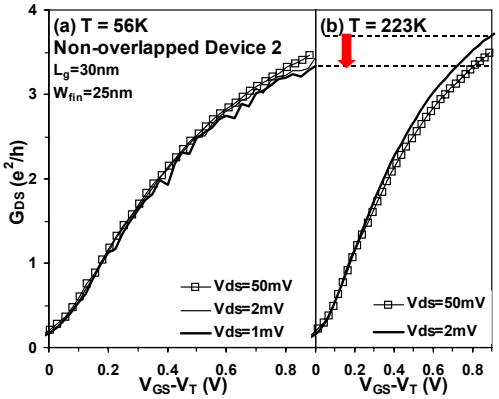

Fig 15. Measured G_{DS} versus (V_{GS}–V_T) characteristics for the nonoverlapped device 2 with L_g = 30 nm and W_{fin} = 25 nm at various V_{DS} under (a) T = 56 K and (b) T = 223 K.

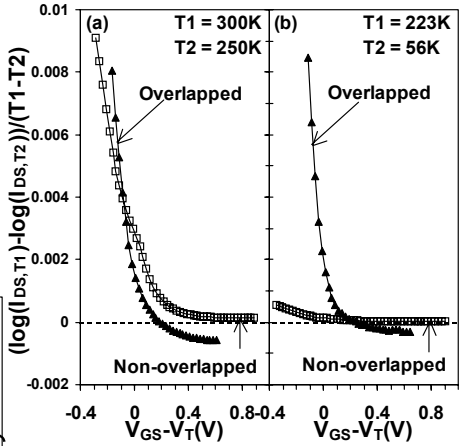

Fig 17. Measured temperature sensitivity of drain current ($\Delta \log(I_{DS})/\Delta T$) versus ($V_{GS} - V_T$) characteristics for overlapped and nonoverlapped devices under (a) high temperature, T = 300 to 250 K and (b) low temperature, T = 223 to 56 K.

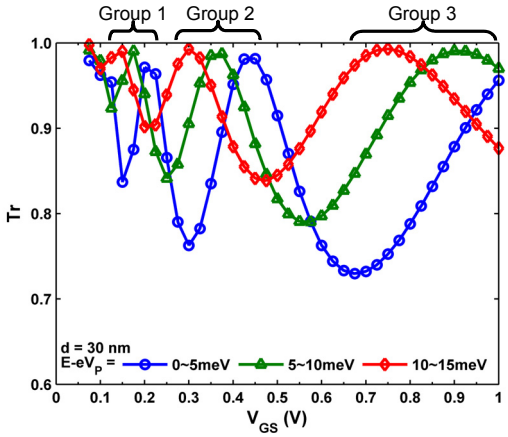

Fig 18. Calculated transmission probability T_r versus V_{GS} for d = 30 nm and E − eV_p = 0–5, 5–10, and 10–15 meV.

出席國際學術會議心得報告

計畫編號	NSC97-2221-E-009-162
計畫名稱	次 32 奈米多重閘極元件的特性分析與模式建立
出國人員姓名 服務機關及職稱	主持人: 蘇彬　國立交通大學電子工程學系
會議時間地點	June 13-17, 2009 Kyoto, Japan
會議名稱	2009 Silicon Nanoelectronics Workshop (June 13-14) 2009 Symposium on VLSI Technology (June 15-17)
發表論文題目	(1) Impact of Uniaxial Strain on Channel Backscattering Characteristics and Drain Current Variation for Nanoscale PMOSFETs (**VLSI Symposium**) (2) Investigation of Switching Time Variations for FinFET and Bulk MOSFETs using the Effective Drive Current Approach (**Silicon Nanoelectronics Workshop**) (3) Investigation of Mismatching Properties in Nanoscale MOSFETs with Symmetric/Asymmetric Halo Implant (**Silicon Nanoelectronic Workshop**)

一、參加會議經過

VLSI Symposium has long been recognized as one of the most important conferences in the VLSI field. This year, a total of 205 papers from 15 countries were submitted, and 82 papers were accepted by the conference. Our paper "*Impact of Uniaxial Strain on Channel Backscattering Characteristics and Drain Current Variation for Nanoscale PMOSFETs*" was presented at the Session 6A - Variability on June 16. The chairpersons were Dr. Masahara from AIST, Japan and Prof. T.-J. King from UC Berkeley. In this work, we used a novel generalized temperature-dependent method to examine the impact of uniaxial strain on backscattering characteristics in nanoscale PFETs. We showed that the backscattering coefficient can be reduced by the uniaxially-compressive strain. We further demonstrated that the strain technology can improve the drain current variation as well as the mismatching properties through the enhanced ballistic efficiency. Overall our presentation went pretty well.

Regarding the Silicon Nanoelectronics Workshop, it is one of the major international conferences in the area of nanoelectronics, bridging between the mainstream CMOS technology and the Si-based nanotechnology. This is the 14th workshop in series. The program has included 5 invited talks, 24 oral presentations, and 52 poster presentations. Our paper "*Investigation of Switching Time Variations for FinFET and Bulk MOSFETs using the Effective Drive Current Approach*" was oral presented at the Session 1 – Nano MOSFETs in the morning of June 13. The chairperson was Prof. T.-J. King from UC Berkeley. In this work, we investigated the switching time variation for FinFET and bulk MOSFETs using a novel

effective drive current approach in CMOS inverters. Our study indicated that for bulk MOSFETs, the switching time variation caused by line edge roughness (LER) may be larger than that caused by random dopant fluctuation (RDF). As for FinFET, although the impact of fin-LER is more crucial to the threshold-voltage variation, the relative importance of gate-LER increases as the switching time variation is considered. Our presentation went smoothly and attracted several questions. Besides, we had one poster presentation addressing the impact of asymmetric halo implant on the mismatching properties of nanoscale MOSFETs.

二、與會心得

From the presentations in the VLSI Symposium and Silicon Nanoelectronics Workshop, we can see several trends for the VLSI field. First, the 3D system integration technology is becoming increasingly important for future technology generations. This is because 3D integration may provide capabilities to integrate heterogeneous technologies as well as to improve the system power efficiency, as demonstrated by the Intel's high-performance floating point system prototype with 3D integrated SRAM. Besides the 3D integration, we can see the challenges facing CMOS lie mainly in *Performance*, *Power*, and *Variability*. To overcome these challenges, new materials (e.g., high-K dielectrics and Ge channel) and new device structures (e.g., FinFET and nanowire) are gaining more and more research efforts from both the industry and academia. Indeed, our 3 papers for the VLSI Symposium and Silicon Nanoelectronics Workshop this year have mainly addressed the problems related to *Variability*. We appreciate the support from National Science Council that makes our dissemination of research results in Kyoto possible, and we will keep working diligently in this important area.

Impact of Uniaxial Strain on Channel Backscattering Characteristics and Drain Current Variation for Nanoscale PMOSFETs

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Department of Electronics Engineering, National Chiao Tung University, Hsinchu, Taiwan
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Abstract—Using an improved temperature-dependent method, this paper clarifies that channel backscattering of nanoscale PMOSFETs can be reduced by the uniaxially compressive strain. For the first time, the electrostatic potential of the source-channel junction barrier has been experimentally characterized with strain and gate voltage dependence. We further demonstrate that the strain technology can improve the drain current variation as well as the mismatching properties through the enhanced ballistic efficiency. Moreover, the improvement shows gate length and drain voltage dependence.

I. Introduction

Channel strain engineering has been actively pursued to enable the mobility scaling of CMOS devices. As the gate length (L_g) scales into the nanoscale regime in which the carrier ballistic transport prevails [1-2], strain-induced enhancement becomes more complicated [3-4]. Characterizing nanoscale strained MOSFETs from the perspective of channel backscattering (r_{sat}) becomes crucial to strain engineering [4-6]. However, it has been reported that uniaxially compressive strain tends to increase the r_{sat} of PMOSFETs [5-6]. The reason is not clear and needs to be clarified. In addition, the impact of uniaxial strain on the drain current variation has rarely been known and merits investigation.

In this work, we examine the impact of uniaxial strain on backscattering characteristics in nanoscale PFETs and demonstrate that r_{sat} can be reduced by the uniaxially compressive strain. Besides, impacts of strain on the electrostatic potential of the source-channel junction barrier (Fig. 1) and the non-threshold-voltage drain current variation (Fig. 2) are experimentally investigated for the first time.

II. Channel Backscattering Characteristics

The strained devices were fabricated by state-of-the-art process-induced uniaxial strained-silicon technology featuring SiGe source/drain and compressive contact etch stop layer (CESL) (Fig. 1) [5-8]. Fig. 3 shows that the saturated drain current ($I_{d,sat}$) and the linear drain current ($I_{d,lin}$) of the strained device are improved by 2.1X and 2.9X as compared with its unstrained counterpart, respectively.

According to the channel backscattering theory [2-3], r_{sat} depends on the mean-free path λ and the critical length l as $r_{sat} = 1/(1+\lambda/l)$ [3]. To obtain r_{sat}, we extracted λ/l using the self-consistent method [9], in which λ/l and $(\beta_\mu-\beta_l)$ can be self-consistently determined by (1) & (2):

$$\frac{\lambda}{\ell} = \frac{-2\left(1+\left(\beta_\mu-\beta_l\right)-\gamma\right)}{\gamma-\left(\left(\partial I_{d,sat}/\partial T\right)/I_{d,sat}+\left(\partial V_{T,sat}/\partial T\right)/\left(V_{gs}-V_{T,sat}\right)\right)T}-2 \quad (1),$$

$$\frac{\lambda}{\ell} \propto \frac{2k_BT\mu_0}{q\upsilon_{therm}}\left(\frac{q}{k_BT}\right)^{\beta_l} \propto T^{1+\left(\beta_\mu-\beta_l\right)-\gamma} \quad (2),$$

where β_μ, β_l and γ are defined as the temperature sensitivity of the low-field mobility μ_0, the critical length l and the thermal velocity υ_{therm}, respectively [10,11]. Contrary to the pervious studies in [5,6,10,11], this self-consistent method [9] does not assume constant β_μ and β_l in the determination of λ/l and r_{sat} (e.g., β_μ = -1.5 and β_l = 1 in (1)). Fig. 4 shows significant discrepancy in the extracted λ/l between the self-consistent $(\beta_\mu-\beta_l)$ and $(\beta_\mu-\beta_l)$ = -2.5. Note that the temperature dependence of λ/l can satisfy the constraint of Eq. (2) for the self-consistent $(\beta_\mu-\beta_l)$, but not for $(\beta_\mu-\beta_l)$ = -2.5. Fig. 5 shows that the self-consistently extracted $(\beta_\mu-\beta_l)$ and r_{sat} are strongly dependent on V_{gs}. Note that the self-consistently extracted $(\beta_\mu-\beta_l)$ (Fig. 5(a)) presents more phonon-limited behavior (i.e., more temperature- sensitive) for the strained device, similar to the measured $I_{d,sat}$ in Fig. 3(a). However, the assumption of $(\beta_\mu-\beta_l)$ = -2.5 results in insensitive r_{sat}–V_{gs} dependence and completely opposite strain effects on r_{sat}.

The reduced r_{sat} in the compressive-strained PFET (r_{sat} for self-consistent $(\beta_\mu-\beta_l)$ in Fig. 5(b)) can be referred to the enhanced λ (Fig. 6(b)), which can be extracted from [3]

$$\frac{I_{d,lin}}{V_{ds}I_{d,sat}} = \frac{(V_{gs}-V_{T,lin})(q/2k_BT)(\lambda/(\lambda+L_g))}{(V_{gs}-V_{T,sat})((1-r_{sat})/(1+r_{sat}))} \quad (3).$$

Besides, we have confirmed that the enhancement of effective mobility μ and υ_{therm} (Figs. 6(c) and 6(a)) follows the relation of $\lambda \propto (2k_BT\mu_0/q\upsilon_{therm})$ [10], i.e., 1.9X (λ enhancement) ~ 3.3X (μ enhancement) / 1.5X (υ_{therm} enhancement). The strain effect on the enhancement of $1/m^*$ and the relaxation time τ can also be obtained: ~2.3X from (υ_{therm} enhancement)^2 and ~1.3X from (λ enhancement)/(υ_{therm} enhancement), respectively. In addition, we further extracted the critical length l by $r_{sat} = 1/(1+\lambda/l)$. Fig. 7(a) shows the potential $-k_BT/q$ vs. (l_T-l_{233K}) characteristics, which can be viewed as the potential gradient of the source-channel junction barrier (Fig. 1). It is clear that more backscattering events for the unstrained device with smaller λ raise the electrostatic potential to higher energy to maintain the same carrier density, as predicted in [12]. Moreover, the V_{gs} dependence of the potential gradient in Fig. 7(b) explains the V_{gs} dependence of r_{sat} for the self-consistent $(\beta_\mu-\beta_l)$ in Fig. 5(b).

III. Drain Current Variation & Ballistic Efficiency

A simple expression relating I_d of nanoscale MOSFETs to μ_0 has been derived by Lundstrom [3] as

$$\delta I_d/I_d = (\delta\mu_0/\mu_0)(1-B) \quad (4),$$

in which the sensitivity of I_d to μ_0 is determined by the ballistic efficiency B. Eq. (4) reveals that the impact of the μ_0 variation, $\sigma(\mu_0)/\mu_0$, on the $I_{d,sat}$ variation, $\sigma(I_{d,sat})/I_{d,sat}$, can be suppressed when the ballistic efficiency B is enhanced. To ensure that the V_T variation does not affect the following analysis, we have confirmed in Fig. 8 that the standard deviation of V_T, $\sigma(V_T)$, as well as the V_T variation, $\sigma(V_T)/V_T$, are similar between strained and unstrained devices. The linear dependence of $\sigma(I_{d,sat})/I_{d,sat}$ on $\sigma(\mu_0)/\mu_0$ presented in Fig. 9 follows the prediction of Eq. (4), in which the slope represents the degree of ballistic efficiency B. The reduced slope for strained PFETs (Fig. 9) can be explained by the B_{sat} enhancement ($B_{sat,strained}$-$B_{sat,unstrained}$) (Fig. 10). It is worth noting that the suppression of $\sigma(I_{d,sat})/I_{d,sat}$, the B_{sat} enhancement and the μ enhancement are more significant with decreasing L_g. Besides, we found that the B enhancement decreases with decreasing V_{ds} (Fig. 11), which may be referred to the relation of $B \sim \lambda/(L+\lambda)$ for low V_{ds}, i.e., the λ enhancement is not important for $\lambda/(L+\lambda)$ as $L >> \lambda$. Such V_{ds} dependence of the B enhancement results in the weak suppression in the $\sigma(I_d)/I_d$ vs. $\sigma(\mu_0)/\mu_0$ characteristics measured at V_{ds} = 0.3 V (Fig. 12).

Statistics on the mismatch in drain current (ΔI_d) and threshold voltage (ΔV_T) were analyzed for identical devices in a matching pair configuration on 60 dies (Fig. 13). Fig. 14 shows that the drain current mismatch in the high gate bias regime is dominated by the non-V_T mismatch. Moreover, improved matching performance for strained PFETs can be observed in Fig. 14 and Fig. 15. It is worth noting that the reduction of $\sigma(\Delta I_d/I_d)$ for strained PFETs (Fig. 15) is more significant for $|V_{ds}|$ = 1 V than for $|V_{ds}|$ = 0.05 V. This result can be understood from the V_{ds} dependence of the B enhancement (Fig. 11).

IV. Conclusion

Using an improved temperature-dependent method, we have shown that the r_{sat} of nanoscale PMOSFETs can be reduced by the uniaxially compressive strain. For the first time, the electrostatic potential of the source-channel junction barrier has been experimentally characterized with strain and V_{gs} dependence. We further demonstrate that the strain technology

can improve the drain current variation as well as the mismatching properties through the enhanced ballistic efficiency. Moreover, the improvement shows L_g and V_{ds} dependence.

ACKNOWLEDGEMENTS: This work was supported in part by the National Science Council of Taiwan under Contract NSC 97-2221-E-009-162, and in part by the Ministry of Education in Taiwan under ATU Program.

REFERENCE: [1] K. Natori, *JAP*, 76, 4879, 1994 [2] M. S. Lundstrom, *EDL*, 18, 361, 1997 [3] M. S. Lundstrom, *EDL*, 22, 293, 2001 [4] T. Skotnicki *et al.*, *TED*, 55, 96, 2008 [5] H.-N. Lin *et al.*, *EDL*, 26, 676, 2005 [6] H.-N. Lin *et al.*, *IEDM*, 141, 2005 [7] J. Kuo *et al.*, *TED*, 2009 [8] P.-N. Chen *et al.*,*TNANO*, 7, 538, 2008 [9] W. Lee *et al.*, *submitted to 2009 VLSI Symp*. [10] M.-J. Chen *et al.*, *IEDM*, 39, 2002 [11] M.-J. Chen *et al.*, *TED*, 51, 1409, 2004 [12] A. Svizhenko *et al.*, *TED*, 50, 1459, 2003

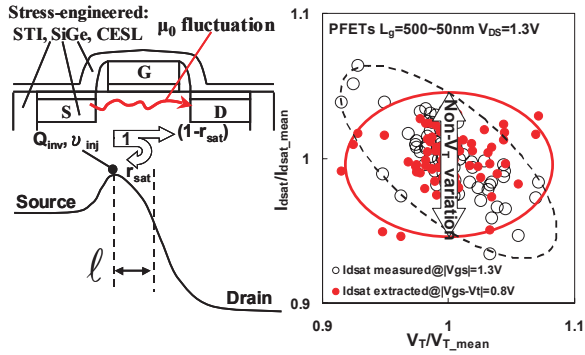

Fig. 1. The impact of uniaxially compressive strain on backscattering coefficients r_{sat} and I_d fluctuation is investigated.

Fig. 2. Normalized $I_{d,sat}$ vs. normalized V_T characteristics showing the impact of the non-V_T variation at high gate bias.

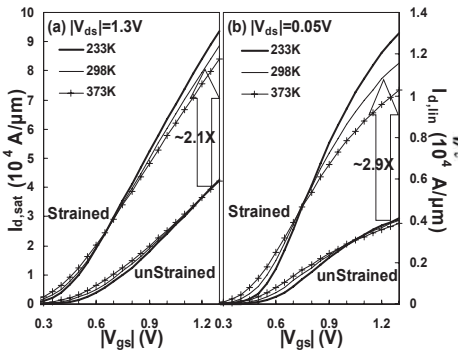

Fig. 3. Measured I_d vs. V_{gs} characteristics for 50-nm-L_g PMOSFETs with and without uniaxially compressive strain at T = 233~373 K for (a) $|V_{ds}|$ = 0.05 V and (b) $|V_{ds}|$ = 1.3 V.

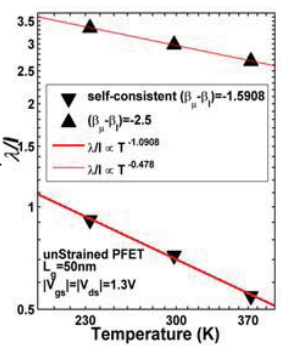

Fig. 4. Extracted λ/l vs. T characteristics showing the need of self-consistent (β_μ-β_l).

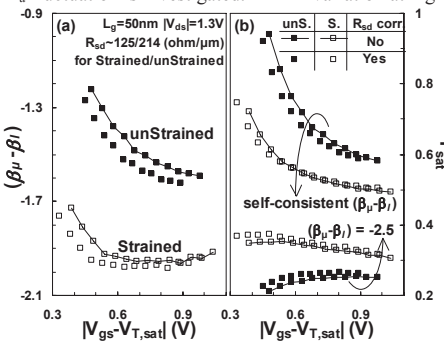

Fig. 5. Extracted (a) (β_μ-β_l) and (b) r_{sat} vs. V_{gs} characteristics for PFETs with and without uniaxially compressive strain. R_{sd} was corrected.

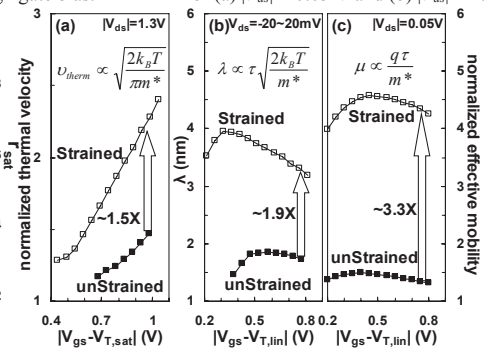

Fig. 6. Extracted (a) thermal velocity v_{therm}, (b) mean-free path λ and (c) effective mobility μ vs. V_{gs} characteristics for strained and unstrained PFETs.

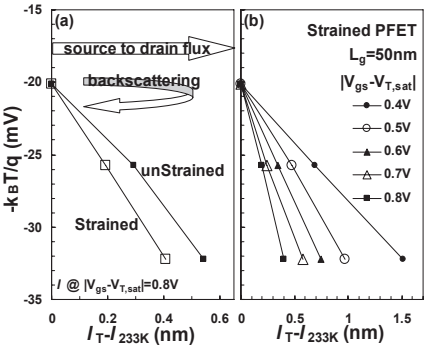

Fig. 7. Extracted potential $-k_BT/q$ vs. (I_T-I_{233K}) characteristics shows (a) the strain dependence and (b) the V_{gs} dependence.

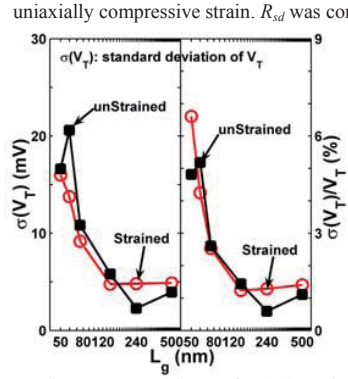

Fig. 8. Comparison of σ(V_T) and σ(V_T)/V_T for strained and unstrained PFETs.

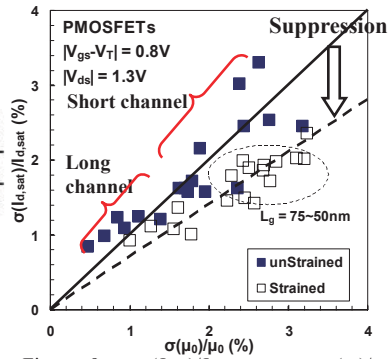

Fig. 9. $\sigma(I_{d,sat})/I_{d,sat}$ vs. $\sigma(\mu_0)/\mu_0$ characteristics for strained and unstrained PFETs with L_g = 50 ~ 500 nm at V_{ds} = 1.3 V.

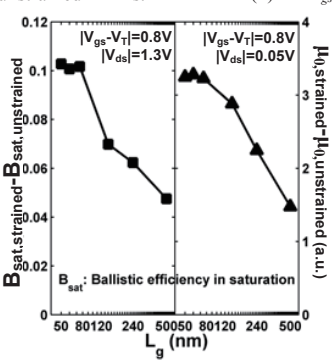

Fig. 10. B_{sat} enhancement and μ enhancement vs. L_g characteristics for strained and unstrained PFETs .

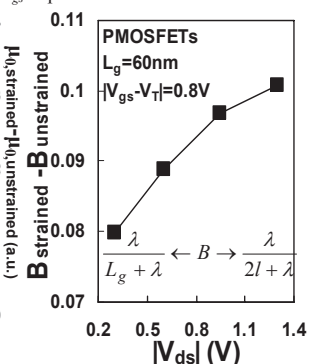

Fig. 11. V_{ds} dependence of the ballistic-efficiency enhancement. B is near $\lambda/(2l+\lambda)$ for high V_{ds} and $\lambda/(L_g+\lambda)$ for low V_{ds}.

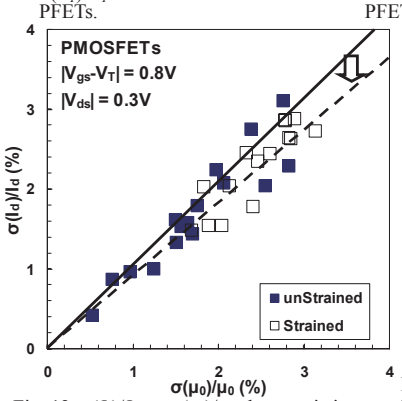

Fig. 12. $\sigma(I_d)/I_d$ vs. $\sigma(\mu_0)/\mu_0$ characteristics for strained and unstrained PFETs with L_g = 50 ~ 500 nm at V_{ds} = 0.3 V.

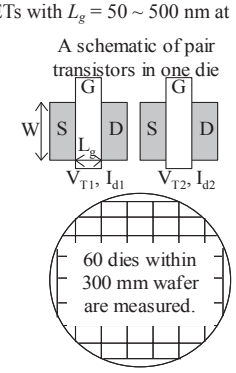

Fig. 13. Schematics of the pair transistors for mismatching measurements of ΔI_d and ΔV_T. $\Delta I_d = |I_{d1} - I_{d2}|$. $\Delta V_T = |V_{T1} - V_{T2}|$.

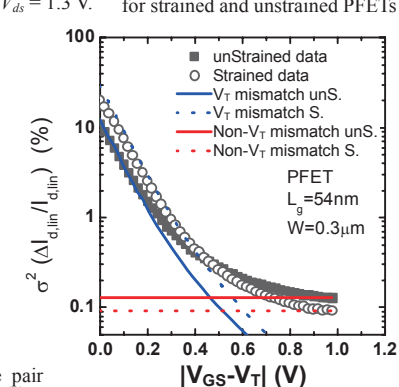

Fig. 14. Comparison of the measured $\sigma^2(\Delta I_d/I_d)$ with the mismatch model. $\sigma^2(\Delta I_d/I_d)$: variance of $\Delta I_d/I_d$.

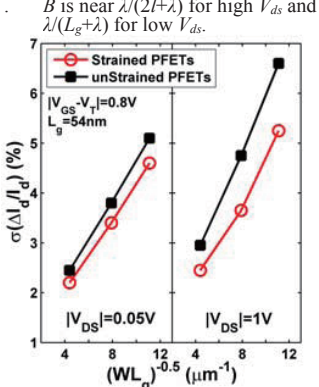

Fig. 15. Pelgrom plot of the standard deviation of normalized ΔI_d, $\sigma(\Delta I_d/I_d)$, for $|V_{ds}|$ = 0.05 V and 1 V.

Investigation of Switching Time Variations for FinFET and Bulk MOSFETs Using the Effective Drive Current Approach

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Introduction

With MOSFET scaling, the impact of random dopant fluctuation (RDF) and line edge roughness (LER) on the threshold voltage (V_{th}) variation for MOSFETs is growing and being extensively examined [1-4]. For logic circuits, the variation of signal switching time due to RDF and LER is especially important. Whether there is any gap between V_{th} and switching time variations merits investigation. In this work, we investigate the switching time variation for FinFET and bulk MOSFETs using the approach of effective drive current in CMOS inverters [5].

Methodology

We decouple the switching time (ST) variation into transition charge (ΔQ) variation and effective drive current (I_{eff}) variation. The ST can be defined as $\Delta Q / I_{eff}$ [6], where ΔQ is the transition charge between logic "ON" and "OFF" states. The ΔQ for an NFET can be calculated by Q_n ($V_{GS} = V_{DD}$, $V_{DS} = 0.05$ V) − Q_n ($V_{GS} = 0$V, $V_{DS} = V_{DD}$). The I_{eff} for an NFET can be approximated as [I_{DS} ($V_{GS} = V_{DD}$, $V_{DS} = 0.5V_{DD}$) + I_{DS} ($V_{GS} = 0.5V_{DD}$, $V_{DS} = V_{DD}$)] / 2 [5]. Therefore, in contrast to the time-consuming mixed-mode transient simulation, only DC simulation for a single device is needed to derive ΔQ and I_{eff}. More importantly, the effective current approach may provide physical insights in the assessment of the switching time variations.

To assess the RDF in bulk MOSFETs, we have carried out the atomistic device simulation using the Monte Carlo approach [2]. To avoid the charge trapping in the sharp Coulomb potential well and hence the mesh size dependences of the simulation results, we have employed the density gradient method in our atomistic simulation [7]. Fig. 1(a) shows a sample used in our RDF atomistic simulation for bulk devices. To assess the LER, the line edge patterns were derived using the Fourier synthesis approach [3], and then the Monte Carlo simulation was performed. Fig. 1(b) shows a sample used in the LER simulations for bulk devices. The multi-gate structure we study in this work is the lightly doped FinFET with aspect ratio = 2 [Fig. 2(a)]. The gate-LER and fin-LER are considered as independent variation sources for FinFET [4]. Fig. 2(b) and (c) show samples used in our Monte Carlo simulations for gate- and fin-LER for FinFET, respectively.

Results and Discussion

Bulk MOSFET

Fig. 3(a) compares the impacts of RDF and LER on the saturation threshold voltage ($V_{th,sat}$) variations of bulk MOSFETs. It can be seen that the standard deviation of $V_{th,sat}$ ($\sigma V_{th,sat}$) due to RDF is larger than that due to LER. Nevertheless, Fig. 3(b) shows that the standard deviation of ST (σST) due to LER is larger than that due to RDF. Since ST = $\Delta Q / I_{eff}$, the normalized standard deviation of ST (σST / μST) can be approximated as $|\sigma ST / \mu ST| \approx |\sigma\Delta Q / \mu\Delta Q - \sigma I_{eff} / \mu I_{eff}|$, where μST, $\mu\Delta Q$ and μI_{eff} are the mean values of ST, ΔQ and I_{eff}, respectively. Fig. 4 shows the $|\sigma ST / \mu ST|$, $|\sigma\Delta Q / \mu\Delta Q|$, and $|\sigma I_{eff} / \mu I_{eff}|$ (normalized standard deviation of ST, ΔQ and I_{eff}, respectively) caused by RDF and LER. It can be seen that the $|\sigma ST / \mu ST|$ due to RDF is roughly equal to the difference of $|\sigma I_{eff} / \mu I_{eff}|$ and $|\sigma\Delta Q / \mu\Delta Q|$ due to RDF. However, the $|\sigma ST / \mu ST|$ due to LER is roughly equal to the sum of $|\sigma I_{eff} / \mu I_{eff}|$ and $|\sigma\Delta Q / \mu\Delta Q|$ due to LER. The results in Fig. 4 can be explained as follows. The impact of RDF on MOSFETs stems from the variation of the effective channel doping ($N_{ch,eff}$). For devices with smaller $N_{ch,eff}$, the V_{th} is smaller and hence both I_{eff} and ΔQ are larger because they are roughly proportional to ($V_{GS} - V_{th}$). Thus, I_{eff} and ΔQ are positively correlated [Fig. 5(a)]. Therefore, $|\sigma ST / \mu ST|$ is roughly equal to the difference of $|\sigma\Delta Q / \mu\Delta Q|$ and $|\sigma I_{eff} / \mu I_{eff}|$ because the quantities of $\sigma\Delta Q$ and σI_{eff} have the same sign. In other words, the impacts of RDF on ΔQ and I_{eff} are mutually canceled and $|\sigma ST / \mu ST|$ is reduced.

The impact of LER on bulk MOSFETs results from the variation of the effective channel length (L_{eff}). For devices with shorter L_{eff}, the V_{th} is smaller because of the short channel effect and hence the I_{eff} is larger. As for ΔQ, devices with shorter L_{eff} possess smaller ΔQ because ΔQ is proportional to the gate area ($W \times L_{eff}$). Thus, I_{eff} and ΔQ are negatively correlated [Fig. 5(b)]. Therefore, $|\sigma ST / \mu ST|$ is roughly equal to the sum of $|\sigma\Delta Q / \mu\Delta Q|$ and $|\sigma I_{eff} / \mu I_{eff}|$ because the quantities of $\sigma\Delta Q$ and σI_{eff} have the opposite sign. In other words, the $|\sigma ST / \mu ST|$ is larger than either $|\sigma\Delta Q / \mu\Delta Q|$ or $|\sigma I_{eff} / \mu I_{eff}|$. Fig. 6 indicates that the relative importance of LER for switching time variation is larger as compared with that for V_{th} variation.

FinFET

Fig. 7(a) compares the impacts of gate-LER and fin-LER on $V_{th,sat}$ variations of FinFET. It can be seen that $\sigma V_{th,sat}$ due to fin-LER is larger than that due to gate-LER. Nevertheless, Fig. 7(b) shows that σST due to gate-LER is larger than that due to fin-LER. Fig. 8 shows the $|\sigma ST / \mu ST|$, $|\sigma\Delta Q / \mu\Delta Q|$, and $|\sigma I_{eff} / \mu I_{eff}|$ caused by gate-LER and fin-LER. The $|\sigma ST / \mu ST|$ due to gate-LER is roughly equal to the sum of $|\sigma I_{eff} / \mu I_{eff}|$ and $|\sigma\Delta Q / \mu\Delta Q|$. This is because I_{eff} and ΔQ due to gate-LER are negatively correlated [Fig. 9(a)]. However, the $|\sigma ST / \mu ST|$ due to fin-LER is roughly equal to the difference of $|\sigma I_{eff} / \mu I_{eff}|$ and $|\sigma\Delta Q / \mu\Delta Q|$. The impact of fin-LER on FinFET stems from the variation of the effective fin width (W_{fin}). For lightly devices with smaller W_{fin}, the V_{th} is larger because of the suppression of short channel effect [1] and hence the I_{eff} is smaller. As for ΔQ, devices with smaller W_{fin} possess smaller ΔQ because ΔQ is proportional to the gate area. Thus, the I_{eff} and ΔQ are positively correlated [Fig. 9(b)]. The impacts of fin-LER on ΔQ and I_{eff} are mutually canceled and $|\sigma ST / \mu ST|$ is reduced. Fig. 10 indicates that the relative importance of gate-LER for switching time variation is larger as compared with that for V_{th} variation.

Conclusions

We have investigated the impact of LER and RDF on switching time variations of bulk MOSFETs and FinFET using the effective drive current approach. The ST variation can be decoupled into ΔQ variation and I_{eff} variation. Our results indicate that for bulk MOSFETs, the ST variation caused by LER may be larger than that caused by RDF. Although RDF has been recognized as the main variation source to V_{th} variation, LER becomes more crucial to the ST variation of bulk MOSFETs. As for FinFET, although the impact of fin-LER is more crucial to V_{th} variation, the relative importance of gate-LER increases as the ST variation is considered. Our study may provide insights for device and circuit designs using advanced CMOS technologies.

Acknowledgement

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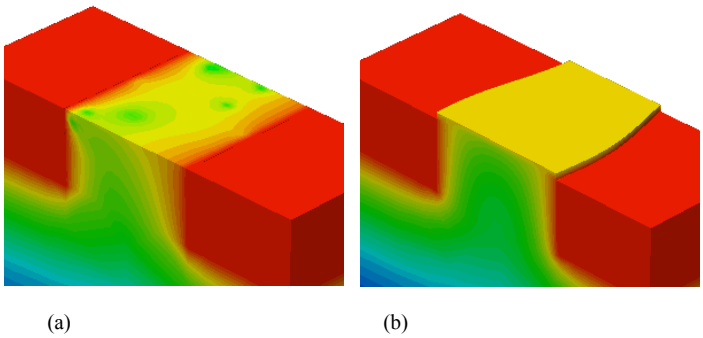
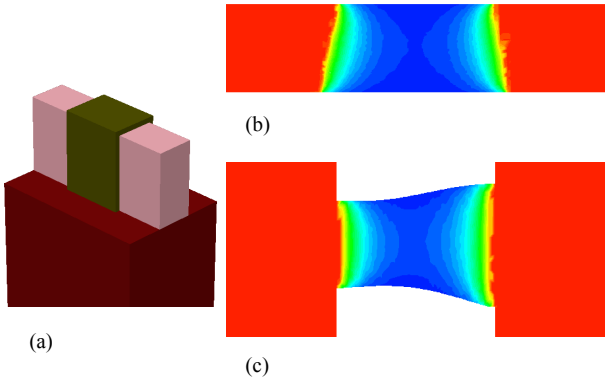


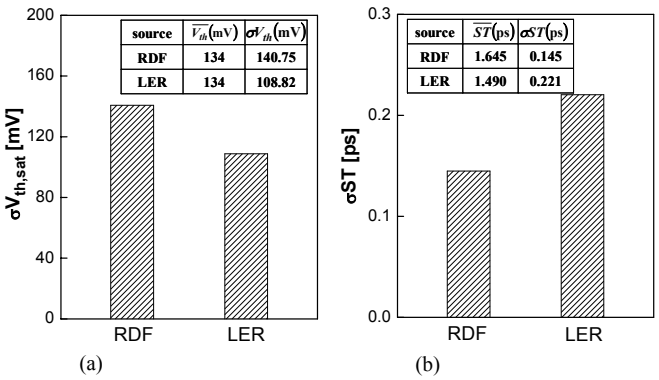
(a) (b)

Fig. 1. The simulated bulk devices in this study. (a) One of the samples with RDF and (b) one of the samples with LER.



(a) (b) (c)

Fig. 2. (a) The nominal FinFET structure with aspect ratio = 2. (b) One of the samples with gate-LER. (c) One of the samples with fin-LER.



(a) (b)

Fig. 3. (a) Comparison of the standard deviations of $V_{th,sat}$ due to RDF and LER in bulk MOSFETs. (b) Comparison of the standard deviations of ST due to RDF and LER in bulk MOSFETs.

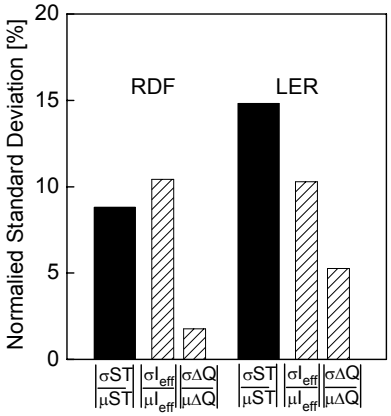


Fig. 4. The normalized standard deviations of ST, I_{eff} and ΔQ due to RDF and LER in bulk MOSFETs.

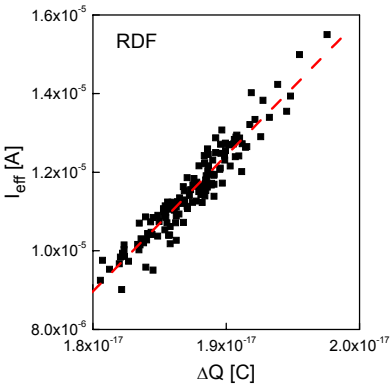


Fig. 5(a). The correlation of I_{eff} distribution and ΔQ distribution for bulk MOSFETs with RDF.

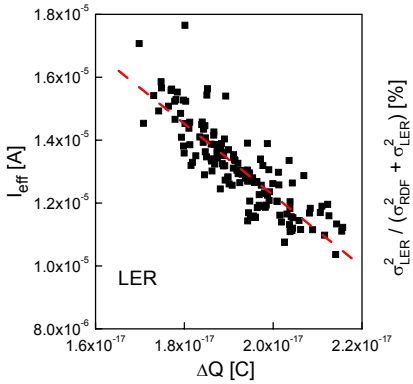


Fig. 5(b). The correlation of I_{eff} distribution and ΔQ distribution for bulk MOSFETs with LER.

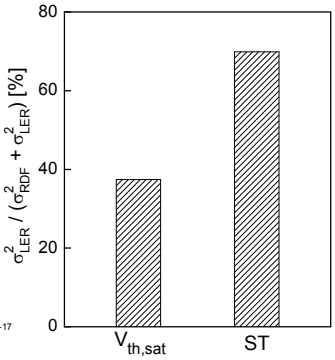
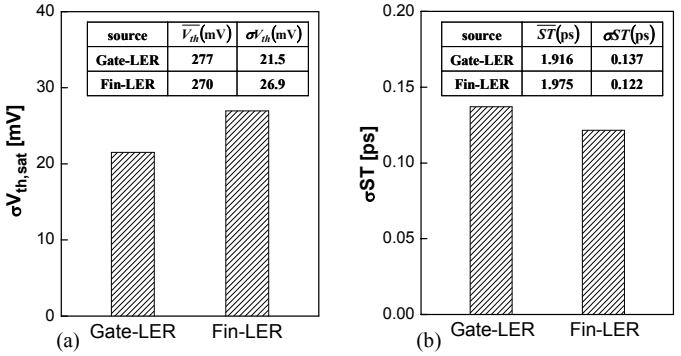


Fig. 6. The relative importance of $V_{th,sat}$ and ST variation caused by LER for bulk MOSFETs. Assume that RDF and LER are independent.



(a) (b)

Fig. 7. (a) Comparison of the standard deviations of $V_{th,sat}$ due to gate- and fin-LER in FinFET. (b) Comparison of the standard deviations of ST due to gate- and fin-LER in FinFET.

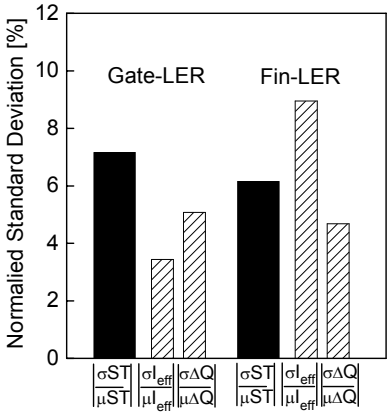
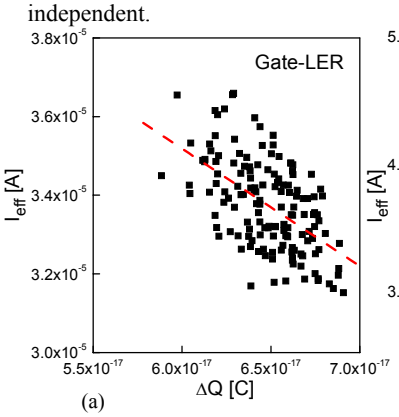
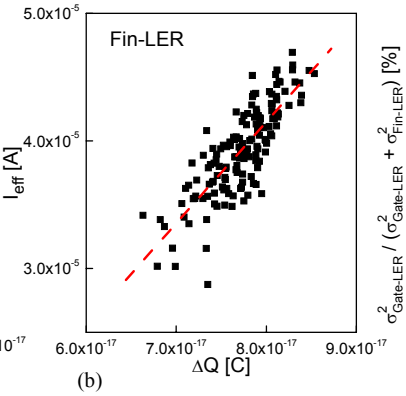


Fig. 8 The normalized standard deviations of ST, I_{eff} and ΔQ due to gate- and fin-LER in FinFET.



(a)



(b)

Fig. 9 The correlations of I_{eff} distribution and ΔQ distribution for FinFET with (a) gate-LER and (b) fin-LER.

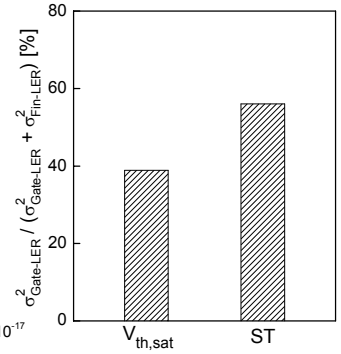


Fig. 10 The relative importance of $V_{th,sat}$ and ST variation caused by gate-LER for FinFET. Assume that gate-LER and fin-LER are independent.

Investigation of Mismatching Properties in nanoscale MOSFETs with Symmetric/Asymmetric Halo Implant

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Introduction

With the scaling of device dimensions, the device mismatching that stems from stochastic fluctuations is becoming a concern for nanoscale MOSFETs [1-3]. Especially, the high concentration halo/pocket implant raises a great concern to the threshold voltage mismatch caused by random dopant fluctuation (RDF) [4-7]. In addition, the asymmetric halo implant structure (with source-side only) has been proposed to suppress the drain-induced threshold shift (DITS) [8]. Nevertheless, the impact of asymmetric halo implant on device mismatching properties has rarely been examined and merits investigation. In this work, we investigate the mismatching properties of symmetric and asymmetric devices using experimental measurement and atomistic device simulation.

Measurement and Simulation

The mismatching properties were measured from identical devices in a matching pair configuration on 60 dies and 40 dies for bulk and partially depleted (PD) SOI devices, respectively. The threshold voltage (V_{th}) was determined by the constant-current method, and current factor (β) was determined by the maximum slope method.

To access the impact of symmetric/asymmetric halo implant on the RDF in MOSFETs, we have carried out the atomistic device simulation (from 150 samples) using the Monte Carlo approach [6]. To avoid the charge trapping in the sharp Coulomb potential well and hence the mesh size dependence of the simulation results, we have employed the density gradient method in our atomistic simulation [7].

Results and Discussion

A. Impact of Symmetric Halo Implant on V_{th} Mismatch

Fig. 1 (a) and (b) show the Pelgrom plot of measured V_{th} mismatch ($\sigma\Delta V_{th}$) for bulk PFETs and NFETs, respectively. The gate width W= 1μm and gate length L_{gate} ranges from 54nm to 1μm. From Fig. 1, it can be seen that the measured $\sigma\Delta V_{th}$ saturates to a finite value as L_{gate} increases, instead of linearly decrease with $(WL_{gate})^{-1/2}$. The deviation of the measured $\sigma\Delta V_{th}$ from the linear relationship between $\sigma\Delta V_{th}$ and $(WL_{gate})^{-1/2}$ expected from the RDF theory [9] implies a fluctuation source that remains as L_{gate} increases. This phenomenon can also be observed for the PD SOI devices shown in Fig. 2.

The anomalous V_{th} fluctuation present in Figs. 1 and 2 can be reproduced by the device simulation (Fig. 3). From the surface potential profile in Fig. 4, it can be seen that potential barriers exist in the halo regions. The potential barrier plays an important role in determining the device V_{th} and thus the V_{th} fluctuation [4, 10]. In other words, the V_{th} fluctuation of the halo-implanted device is mainly determined by the RDF in the halo-implanted region and is less sensitive to L_{gate} as L_{gate} increases.

B. Comparison of V_{th} Mismatch for Asymmetric and Symmetric Devices

While the symmetric device suffers from the DITS [8], the asymmetric halo implanted structure (with source-side implant only) has been proposed and shown higher immunity to DITS (Fig.5). Nevertheless, Fig. 6 indicates that the $\sigma\Delta V_{th}$ of the asymmetric device is larger than that of the symmetric device. The device simulation results in Fig. 7 also show larger V_{th} fluctuation for the asymmetric one. The larger V_{th} fluctuation present in the asymmetric device can be attributed to the smaller potential barrier region as compared with the symmetric counterpart, as demonstrated in Fig. 8.

C. Comparison of β Mismatch for Asymmetric and Symmetric Devices

Fig. 9 shows the measured Pelgrom plot of $\sigma(\Delta\beta)/\beta$ for symmetric and asymmetric devices. It can be seen that the $\sigma(\Delta\beta)/\beta$ of the asymmetric device is larger than that of the symmetric one. Fig. 10 further indicates that the larger $\sigma(\Delta\beta)/\beta$ results from the larger $\sigma(\Delta\beta)$ present in the asymmetric device. To further understand the enhanced $\sigma(\Delta\beta)$ in the asymmetric device, we have performed low frequency noise measurements. This is because carrier mobility fluctuations show their presence in the low frequency noise characteristics. Through a careful extraction, we found that the Hooge parameter [11], which represents the degree of mobility fluctuations, is larger for the asymmetric device as compared with the symmetric one (Fig. 11). It is plausible that the larger $\sigma(\Delta\beta)$ results from the larger mobility fluctuation present in the asymmetric device.

Conclusions

We have investigated the mismatching properties in nanoscale MOSFETs with symmetric/asymmetric halo implant. We show that the V_{th} mismatch is mainly determined by the RDF in the halo-implanted region, and the V_{th} mismatch for the asymmetric device is larger than that of the symmetric one. Besides, the asymmetric device shows larger $\sigma(\Delta\beta)/\beta$ which results from larger $\sigma(\Delta\beta)$. It is plausible that the larger $\sigma(\Delta\beta)$ results from larger mobility fluctuation present in the asymmetric device.

Acknowledgement

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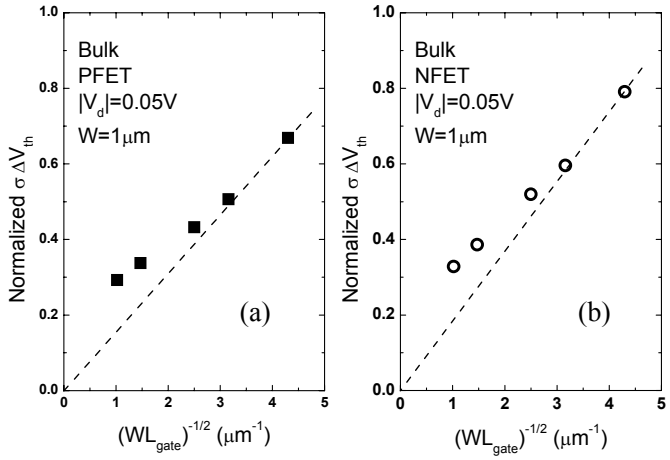

Fig. 1 Pelgrom plot of measured $\sigma\Delta V_{th}$ for (a) bulk PFET and (b) bulk NFET.

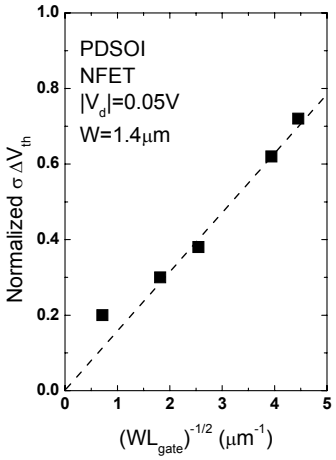

Fig. 2 Pelgrom plot of measured $\sigma\Delta V_{th}$ for PD SOI NFET.

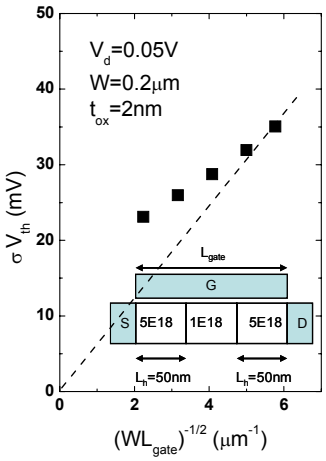

Fig. 3 Pelgrom plot of simulated σV_{th} for bulk NFET. The simulated device structure is shown in the inset.

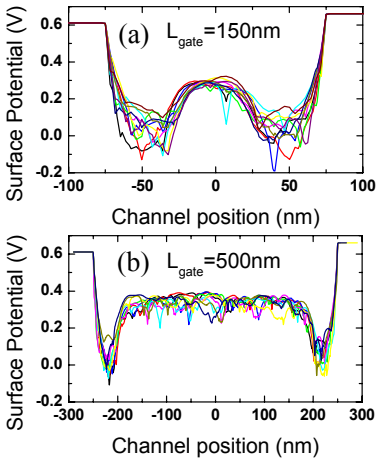

Fig. 4 Surface potential along the channel (from 10 samples) for (a) L_{gate}=150nm and (b) L_{gate}=500nm.

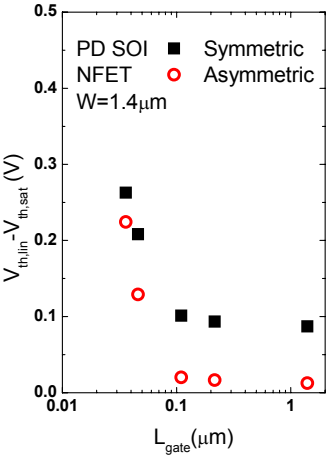

Fig. 5 Measured $V_{th,lin}$-$V_{th,sat}$ versus L_{gate} for symmetric and asymmetric halo-implanted devices.

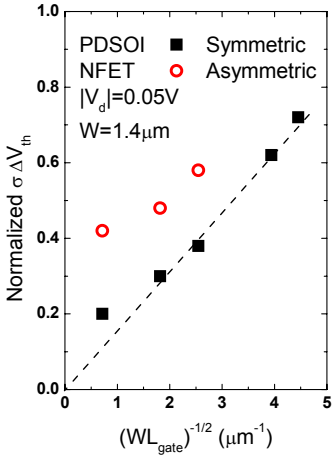

Fig. 6 Pelgrom plot of measured $\sigma\Delta V_{th}$ for the symmetric and asymmetric devices.

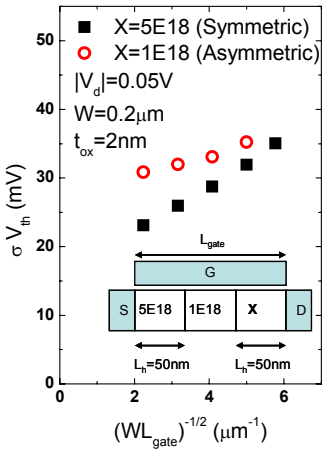

Fig. 7 Pelgrom plot of simulated $\sigma\Delta V_{th}$ for the symmetric and asymmetric devices. The simulated device structure is shown in the inset.

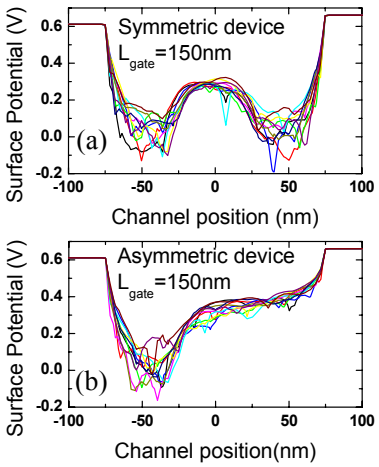

Fig. 8 Surface potential along the channel (from 10 samples) for (a) symmetric, and (b) asymmetric devices.

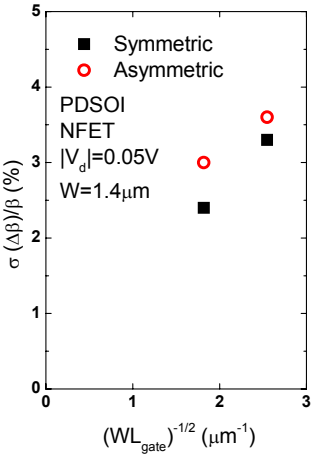

Fig. 9 Pelgrom plot of $\sigma(\Delta\beta)/\beta$ showing larger $\sigma(\Delta\beta)/\beta$ for the asymmetric device.

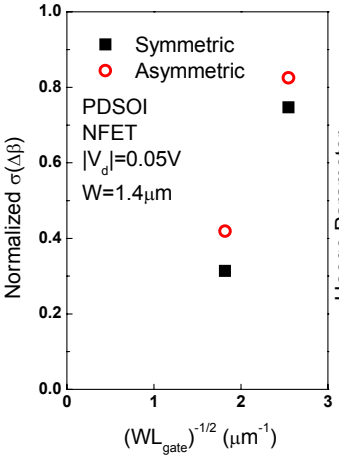

Fig. 10 Pelgrom plot of $\sigma(\Delta\beta)$ for the symmetric and asymmetric devices.

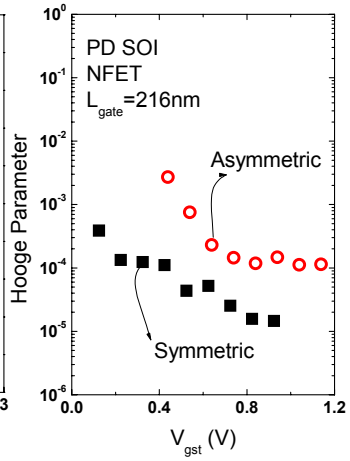

Fig. 11 Hooge parameter versus $|V_{gst}|$ for the symmetric and asymmetric devices with L_{gate} =216nm.