Investigation of Impact Ionization in InAs-Channel HEMT for High-Speed and Low-Power Applications

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***Abstract*—An 80-nm InP high electron mobility transistor (HEMT) with InAs channel and InGaAs subchannels has been fabricated. The high current gain cutoff frequency (f_t) of 310 GHz and the maximum oscillation frequency $(f_{\max})$ of 330 GHz were obtained at $V_{\mathrm{DS}} = 0.7$ V due to the high electron mobility in the InAs channel. Performance degradation was observed on the cutoff frequency (f_t) and the corresponding gate delay time caused by impact ionization due to a low energy bandgap in the InAs channel. DC and RF characterizations on the device have been performed to determine the proper bias conditions in avoidance of performance degradations due to the impact ionization. With the design of InGaAs/InAs/InGaAs composite channel, the impact ionization was not observed until the drain bias reached 0.7 V, and at this bias, the device demonstrated very low gate delay time of 0.63 ps. The high performance of the InAs/InGaAs HEMTs demonstrated in this letter shows great potential for high-speed and very low-power logic applications.**

***Index Terms*—Gate delay time, high electron mobility transistors (HEMTs), impact ionization, InAs-channel.**

I. Introduction

With the ultimate limit for the scaling of Si devices for device-performance improvement being approached, planar III–V compound semiconductor field effect transistors (FETs) have been identified as one of the most attractive devices for nanoelectronic applications. The excellent RF performance has been demonstrated by InAlAs/InGaAs high electron mobility transistors (HEMTs) on InP substrate [1]. Generally, higher electron mobility and velocity can be realized by the increase of the indium content in the InGaAs channel, which makes InAs-channel heterostructure FETs (HFETs) well suitable for low-power and high-speed logic applications due to the extremely high electron mobility of more than 30 000 $\mathrm{cm}^2/\mathrm{V} \cdot \mathrm{s}$ [2], [3].

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However, high indium-content devices usually suffer from serious kink effect, low breakdown voltage, and high output transconductance caused by the electron–hole pair generation created by impact ionization. This phenomenon is even more remarkable for InAs/AlSb structures because of the lack of hole confinement due to type II alignment [2]. In general, the output conductance limits the achievable gain and the breakdown voltage and has a direct impact on the power performance of such devices [4], [5].

In this letter, the impact-ionization behavior in the RF and digital performances of the InAs HEMT with $\mathrm{In_{0.53}Ga_{0.47}As}$/InAs/$\mathrm{In_{0.53}Ga_{0.47}As}$ composite channel structure was investigated. Owing to the $\mathrm{In_{0.53}Ga_{0.47}As}$ subchannels with a higher energy bandgap, the InAs/$\mathrm{In_{0.53}Ga_{0.47}As}$ heterostructure obtains a lower gate leakage current and a higher breakdown voltage. The effect of impact ionization on the device performance will also be discussed, with the optimum bias conditions determined through complete dc and RF characterizations.

II. Device Fabrication

The HEMT structure was grown on 2" semi-insulating InP substrate by molecular beam epitaxy. The structure from bottom to top consisted of a 600-nm-thick $\mathrm{In_{0.52}Al_{0.48}As}$ buffer layer, a 3-nm-thick $\mathrm{In_{0.53}Ga_{0.47}As}$ lower subchannel, a 5-nm-thick InAs channel layer, a 3-nm-thick $\mathrm{In_{0.53}Ga_{0.47}As}$ upper subchannel, a 3-nm-thick $\mathrm{In_{0.52}Al_{0.48}As}$ spacer layer, a Si δ-doped (sheet density of $4 \times 10^{12}\ \mathrm{cm}^{-2}$) layer, a 5-nm-thick $\mathrm{In_{0.52}Al_{0.48}As}$ barrier, a 5-nm-thick InP etching stop layer, and a 40-nm-thick Si-doped $\mathrm{In_{0.53}Ga_{0.47}As}$ cap $(2 \times 10^{19}\ \mathrm{cm}^{-3})$. The InP etching stop layer was used to improve the selectivity of wet chemical recess etch and provide semiconductor surface passivation on each side of the gate to reduce the trapping effect on the InAlAs surface [6]. With the use of the InP etching stop layer, the lateral recess length was easy to control, and the RF performance was improved [7].

The mesa isolation was done by wet chemical etch. Source and drain ohmic metals were formed with 240-nm-thick Au/Ge/Ni/Au and alloyed by rapid thermal annealing at 250 °C for 30 s. As a result of the highly Si-doped cap, a low ohmic contact resistance (R_c) of 0.025 $\Omega \cdot$ mm and a sheet resistance (R_{sh}) of 35.3 $\Omega/\square$ were obtained by using the transmission line model method. The T-shaped gate lithography was carried out in 50-keV JEOL electron beam lithography system (E-beam). The gate recess was performed by wet chemical etching using succinic acid-based solution. The Ti/Pt/Au gate metal was formed by evaporation and lift off. The gate length of 80 nm was estimated by scanning electron microscopy. Devices were passivated using a 100-nm-thick plasma-enhanced

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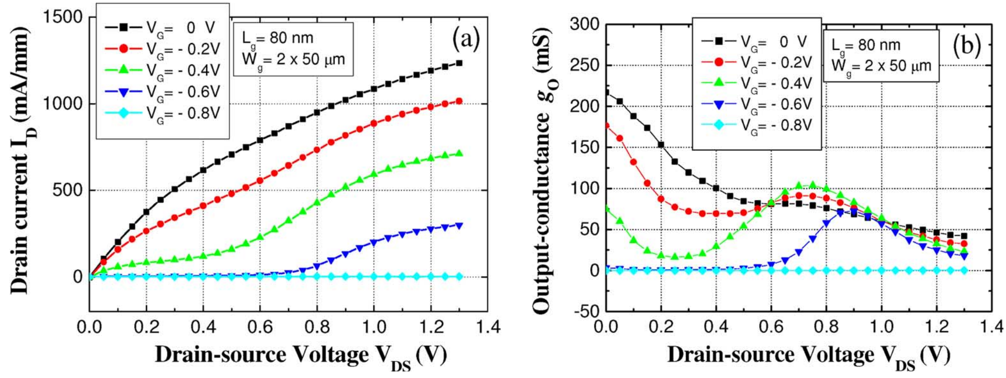

Fig. 1. Output characteristics of a 0.08 μm $\times$ 100 μm InAs/InGaAs HEMT. (a) Drain current I_D as a function of drain bias V_D with different gate voltage V_G from 0 to -0.8 V. (b) Normalized output conductance g_o as a function of V_D.

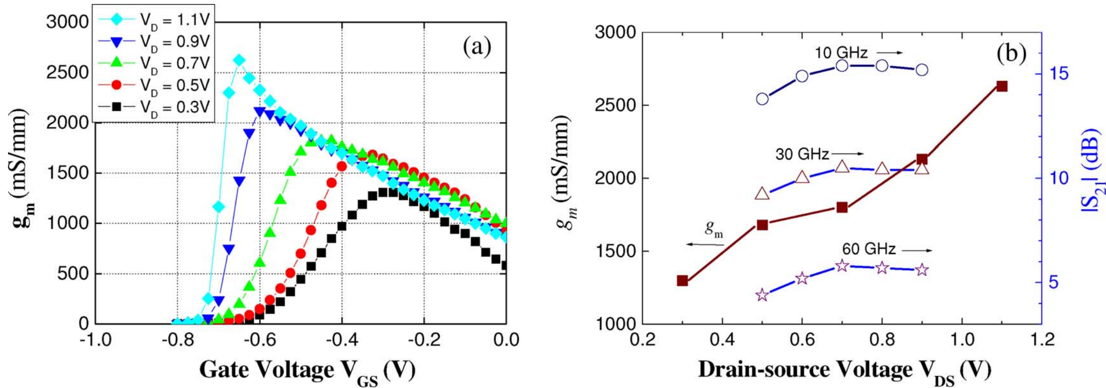

Fig. 2. (a) DC transconductance g_m of a 0.08 μm $\times$ 100 μm device as a function of V_G with different drain voltage V_D. (b) Plot of $|S_{21}|$ measured at 10, 30, and 60 GHz and g_m versus drain–source voltage of 0.08 μm $\times$ 100 μm.

chemical-vapor-deposition silicon nitride film. Finally, the air-bridges were formed with 2 μm of plated Au.

III. Results and Discussion

Fig. 1(a) shows the current–voltage (I–V) characteristics of the 80-nm gate HEMT device with a 2×50 μm gate width. As observed from the figure, this device can be well pinched off with a threshold voltage of -0.7 V and demonstrates a high breakdown voltage with a low gate leakage current. Additionally, a relatively high drain–current density of 700 mA/mm was observed at a low $V_{\rm DS}$ of 0.5 V, primarily due to the superior electron transport properties in the InAs channel. It is noted from the I–V curve that the drain current tends to increase at a constant slope for $V_{\rm DS} > 0.7$ V. This is mainly due to the existence of impact ionization as evidenced by the hump occurred in the vicinity of $V_{\rm DS} = 0.7$ V that was observed in the output conductance measurement, as shown in Fig. 1(b). Fig. 2(a) shows the dc transconductance (g_m) as a function of gate voltage (V_G) at different $V_{\rm DS}$ from 0.3 to 1.1 V. The device exhibits high g_m values, with a peak of 1600 mS/mm at $V_{\rm DS} = 0.5$ V and 2630 mS/mm at $V_{\rm DS} = 1.1$ V. The drastic increase in peak g_m values for $V_{\rm DS} > 0.7$ V is mainly due to the additional electron–hole pairs generated by impact ionization in the channel. Electrons merely flow in the channel, which adds to the channel current, and increase the transconductance. However, if the resulting holes are unconfined by band lineup, the holes will leave the channel and flow into the negatively bias Schottky gate either to cause an increase in the gate leakage current or to accumulate below the gate (or channel) area, contributing to a higher gate-to-source capacitance. A record-high ON-state breakdown voltage ($BV_{\rm DS}$, defined at 1-mA/mm gate current) of 1.75 V was measured at $V_G = -0.8$ V, indicating a good hole confinement achieved by such a channel structure [4], [5], [8].

To investigate the effect of impact ionization on the RF performance, the S-parameter of the 2×50 μm device was measured using Cascade Microtech on-wafer probing system with a vector network analyzer from 1 to 110 GHz. A standard load–reflection–reflection–match calibration method was used to calibrate the measurement system. Fig. 2(b) shows the measured $|S_{21}|$ (in decibels) at various frequencies as functions of drain voltage. DC transconductance g_m, as a function of drain voltage, is also included in the figure. It is clear that, despite the monotonic increasing trend of g_m with the drain voltage, $|S_{21}|$ tends to saturate at a constant level for drain biases higher than 0.7 V. The primary reason was that the impact ionization occurred at drain biases higher than 0.7 V and the generated electrons cannot catch up with the field modulation at RF frequencies. The gate current plotted as a function of gate voltage, as shown in Fig. 3(a), further manifests the impact-ionization phenomenon occurred when $V_{\rm DS}$ was higher than 0.7 V. It also shows better gate leakage performance as compared to the Sb-based InAs-HFETs [8], [9]. To further investigate such phenomenon, the pad parasitic effects were carefully deembedded through the S-parameter measurements, and the intrinsic device parameters were extracted and listed in Table I. The extracted RF g_m values at different bias levels are also

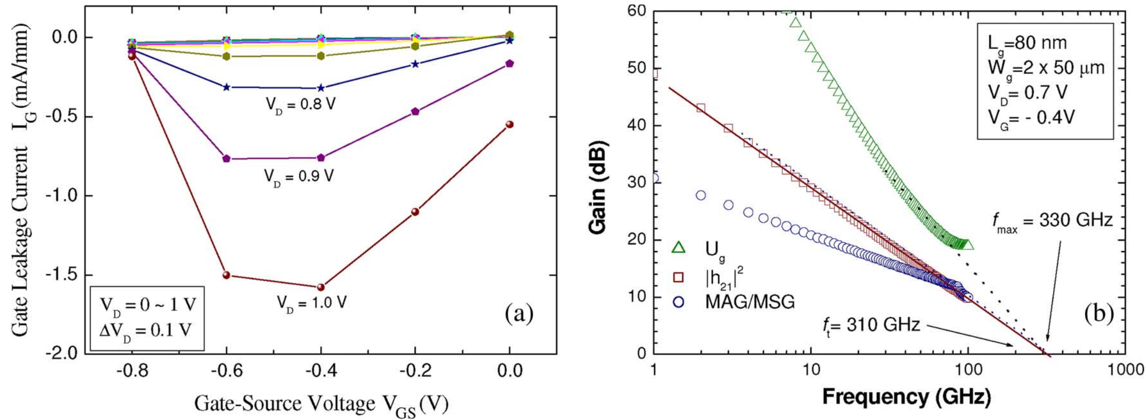

Fig. 3. (a) Gate current I_G plotted as a function of V_G at different V_D from 0 to 1 V, 0.1 V per step. (b) Typical current gain $|h_{21}|$, MAG/MSG, and U_g as a function of frequency of a 0.08 μm × 100 μm InAs/InGaAs HEMT. The V_{DS} is 0.7 V, and the V_G is −0.4 V.

TABLE I
EXTRACTED INTRINSIC PARAMETERS OF A 0.08 μm × 100 μm InAs/InGaAs HEMT WITH DIFFERENT DRAIN–SOURCE VOLTAGE V_{DS} FROM 0.5 TO 0.9 V

V_{DS}	0.5V	0.6V	0.7V	0.8V	0.9V
C_{GS} (fF)	53.0	62.1	73.2	78.4	88.3
C_{GD}(fF)	35.0	24.8	23.1	20.0	18.3
RF g_m (mS/mm)	1380	1480	1870	1620	1550
f_t (GHz)	250	272	310	239	232

listed in the table. It can be observed that the drastic increase in C_{GS} at higher drain bias levels, together with the decrease in RF g_m caused by impact ionization, severely degrades the cutoff frequency f_t, resulting in the peaked f_t value of 310 GHz at $V_{\mathrm{DS}} = 0.7$ V.

Complete dc and RF analysis for the investigation of the effect of impact ionization on the device reveal that the device should be biased at $V_{\mathrm{DS}} = 0.7$ V for optimum performance. Current gain $(|h_{21}|^2)$, Mason's unilateral gain (U_g), and MAG/MSG as a function of frequency are plotted in Fig. 3(b). The intrinsic f_T and $f_{\max}$ obtained for the 2×50 μm device are 310 and 330 GHz at $V_{\mathrm{DS}} = 0.7$ V, exhibiting better performance than other InAs-channel devices with InAlAs or Sb-based barrier [8], [10] and comparable to the performance of InGaAs-channel HEMTs with high In concentration [1], [11], [12]. To characterize such device for high-speed logic applications, the gate delay time (CV/I), according to the definition in [13], was calculated to be 0.63 ps at the optimum bias $V_{\mathrm{DS}} = 0.5$ V. This excellent intrinsic device speed of the InAs/InGaAs HEMT shows great potential for logic applications compared to the state-of-the-art planar and nonplanar Si logic transistors.

IV. CONCLUSION

In this letter, a high-performance InAs/InGaAs HEMT was demonstrated. High ON-state breakdown voltage BV_{DS} of 1.75 V and very low gate leakage current were obtained by using $In_{0.52}Al_{0.48}As$ barrier layer and $In_{0.53}Ga_{0.47}As/InAs/In_{0.53}Ga_{0.47}As$ composite channel structure. The effect of impact ionization on the device performance has been investigated through complete dc and RF characterizations which determine the optimum drain bias voltage of 0.7 V. High current gain cutoff frequency (f_t) of 310 GHz and maximum oscillation frequency $(f_{\max})$ of 330 GHz with a very low gate delay time of 0.63 ps were achieved at the optimum drain voltage of 0.7 V. With the high gain and high speed at low drain voltage, such devices show tremendous potential in future high-speed and low-power logic applications.

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