High-Performance and Low-Temperature-Compatible p-Channel Polycrystalline-Silicon TFTs Using Hafnium-Silicate Gate Dielectric

Ming-Jui Yang, Chao-Hsin Chien, *Associate Member, IEEE*, Yi-Hsien Lu, Guang-Li Luo, Su-Ching Chiu, Chun-Che Lou, and Tiao-Yuan Huang, *Fellow, IEEE*

***Abstract*—In this letter, high-performance p-channel polycrystalline-silicon thin-film transistors (TFTs) using hafnium-silicate ($HfSiO_x$) gate dielectric are demonstrated with low-temperature processing. Because of the higher gate-capacitance density, TFTs with $HfSiO_x$ gate dielectric exhibit excellent device performance in terms of higher I_{ON}/I_{OFF} current ratio, lower subthreshold swing, and lower threshold voltage (V_{th}) albeit with slightly higher OFF-state current. More importantly, the mobility of TFTs with $HfSiO_x$ gate dielectric is 1.7 times that of TFTs with conventional deposited-SiO_2 gate dielectric.**

***Index Terms*—Hafnium silicate ($HfSiO_x$), high dielectric constant (high-κ), polycrystalline-silicon thin-film transistors (poly-Si TFTs).**

I. Introduction

POLYCRYSTALLINE-SILICON thin-film transistors (poly-Si TFTs) have been widely used in active-matrix liquid-crystal display because of their superior performance [1]. Recently, the feasibility of integrating the entire system on the panel is being actively pursued [2]. For this goal, the display-driving circuits require high-performance TFTs capable of operating at lower voltages while delivering higher drive currents. Although thinning down the gate oxide can increase the drive current of TFTs, it results in higher gate leakage current [3]. In order to preserve the physical dielectric thickness while increasing the gate capacitance, several new high-κ materials, including Al_2O_3, Ta_2O_5, and HfO_2, were proposed [4]–[6]. Among them, the κ value of Al_2O_3 films is only ~7; therefore, its improvement is not sufficient [7]. On the other hand, due to its narrow band gap, a thicker Ta_2O_5 film is necessary to reduce the gate leakage current of TFTs [8], thus limiting the gate-capacitance increase. Recently, hafnium dioxide (HfO_2) was also applied to TFTs due to its high-κ value (14–20) and wide band gap. Even though poly-Si TFTs using HfO_2 gate dielectric show better performance in many aspects, the higher gate leakage current due to poly-crystalline HfO_2 films and the degraded mobility arising from additional scattering remain to be resolved [6]. In this letter, we studied $HfSiO_x$ as the gate dielectric for p-channel poly-Si TFTs, and we found that the transistors exhibit higher I_{ON}/I_{OFF} current ratio, smaller subthreshold swing (SS), lower V_{th}, and higher mobility over those with conventional deposited-SiO_2 dielectric.

II. Device Fabrication

First, 550-nm-thick thermal oxide was grown on Si wafers in furnace to simulate the glass substrate. Then, a 100-nm-thick amorphous-silicon layer was deposited by the dissociation of SiH_4 gas in a low-pressure chemical vapor deposition (LPCVD) system at 550 °C. Subsequently, solid-phase crystallization was performed at 600 °C for 24 h in N_2 ambient to induce the recrystallization of amorphous silicon. Individual active regions were then patterned and defined. After cleaning, different gate dielectrics, all of which were 60 nm in thickness, were deposited. Specifically, both HfO_2 and $HfSiO_x$ films were deposited by atomic vapor deposition using an AIXTRON Tricent system at a substrate temperature of 500 °C. The conventional oxide was prepared by LPCVD with tetra-ethyl-oxy-silane precursor at 700 °C to serve as the control sample. Afterward, all wafers received a 300-nm-thick amorphous silicon deposition by LPCVD at 550 °C to serve as the gate electrode. The gate electrodes were patterned, and the source, drain, and gate regions were doped by a self-aligned boron-ion implantation at a dosage and an energy of 5×10^{15} ions/cm^{-2} and 15 keV, respectively. After source/drain formation, dopant activation was executed at 600 °C for 24 h in N_2 ambient. Finally, metallization and sintering were performed to complete the fabrication. For the device measurements, a Keithley 4200 semiconductor characterization system, an HP 4156A

Manuscript received May 17, 2007; revised July 9, 2007. This work was supported in part by the National Science Council, Taipei, Taiwan, R.O.C., under Contract 95221E009313. The review of this letter was arranged by Editor J. Sin.

M.-J. Yang and C.-H. Chien are with the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C. They are also with the National Nano Device Laboratory, Hsinchu 300, Taiwan, R.O.C. (e-mail: chchien@mail.ndl.org.tw).

Y.-H. Lu and T.-Y. Huang are with the Department of Electronics Engineering and Institute of Electronics, National Chiao Tung University, Hsinchu 300, Taiwan, R.O.C.

G.-L. Luo is with the National Nano Device Laboratory, Hsinchu 300, Taiwan, R.O.C.

S.-C. Chiu and C.-C. Lou are with the MSSCORPS Company, Ltd., Hsinchu 30072, Taiwan, R.O.C.

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Digital Object Identifier 10.1109/LED.2007.904901

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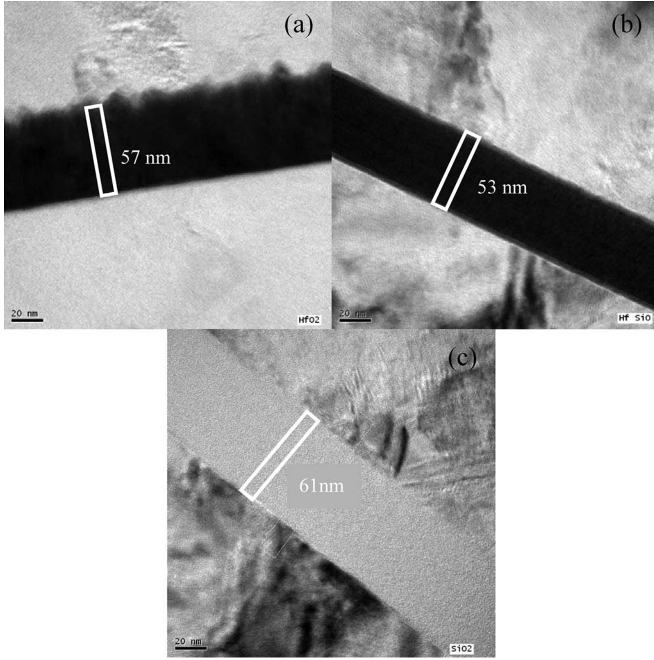

Fig. 1. Cross-sectional TEM pictures of TFTs using (a) HfO_2, (b) $HfSiO_x$, and (c) deposited-SiO_2 gate dielectrics.

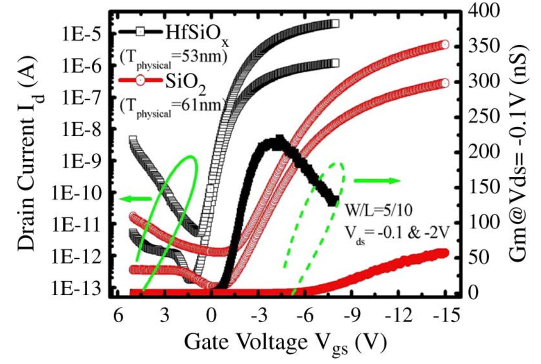

Fig. 2. Transfer characteristics of TFTs using $HfSiO_x$ or deposited SiO_2 as gate dielectric.

TABLE I
SUMMARY OF DEVICE PARAMETERS OF TFTs USING DIFFERENT GATE DIELECTRICS AT $V_{\rm ds} = -0.1$ V

Gate dielectric	I_{on}/I_{off} ratio ($@V_{ds}$= -2V)	S. S. (V/Dec)	V_{th} (V)	μ_{FE} (cm^2/V-sec)	EOT (nm)
HfO_2 ($T_{physical}$ = 57nm)	4.86E6 (V_{gs}= -8V)	0.30	0.45	12.04	15.7
$HfSiO_x$ ($T_{physical}$ = 53nm)	4.12E6 (V_{gs}= -8V)	0.37	-0.91	27.45	25.5
LPCVD SiO_2 ($T_{physical}$ = 61nm)	3.56E6 (V_{gs}= -15V)	1.06	-6.85	15.82	46.5

precision semiconductor parameter analyzer, and an Agilent 4284A precision LCR meter were used. The field-effect mobility, which was extracted from the maximum transconductance (G_m), and the SS were measured at $V_{\rm ds} = -0.1$ V. The threshold voltage was defined as the gate voltage at which the drain current reached a normalized drain current of $I_{\rm ds} = (W/L) \times 10^{-8}$ A at $V_{\rm ds} = -0.1$ V. TFTs with $W/L = 5\ \mu$m/10 μm were measured, where W is the drawn channel width, and L is the drawn channel length.

III. RESULTS AND DISCUSSION

Fig. 1 shows the cross-sectional transmission electron microscopy (TEM) images of the HfO_2, $HfSiO_x$, and deposited-SiO_2 films with physical thicknesses of 57, 53, and 61 nm, respectively. The interfacial layers formed between the HfO_2/Si and $HfSiO_x$/Si surfaces are about 3 nm. It can be seen that the $HfSiO_x$ film depicts amorphous structure, contrary to the polycrystalline structure seen in HfO_2 film, which is conducive to a smoother surface at both the top and the bottom interfaces. This result is consistent with our X-ray-diffraction spectroscopy data (not shown).

Fig. 2 shows transfer characteristics of TFTs with $HfSiO_x$ and SiO_2 at $V_{\rm ds} = -0.1$ and -2 V. The measured data and the extracted device parameters are summarized in Table I. Obviously, TFTs with high-κ dielectrics depict much better performance than TFTs with conventional deposited SiO_2 except for the OFF-state leakage current. In addition to the better gate dielectrics/poly-Si interface quality [5], the thinner equivalent oxide thickness with the same physical thickness of high-κ dielectrics could explain the lower $V_{\rm th}$ and significantly improved SS [9], [10]. Previously, the authors had reported that the $V_{\rm th}$ and SS factors are sensitive to the density of deep states near the midgap [11]. As the density of states decreases, $V_{\rm th}$ and SS decrease. Fig. 3 shows the plots of density of states versus $E{-}E_{\rm fb}$ of poly-Si TFTs with different gate dielectrics. These results are extracted from the transfer characteristics that were measured at 25 °C, 50 °C, 75 °C, 100 °C, and 125 °C [12]. It can be seen that high-κ dielectrics show lower density-of-state values. Even though the SS and the $I_{\rm ON}/I_{\rm OFF}$ current ratio of TFTs with $HfSiO_x$ are slightly worse than those of TFTs with HfO_2, we believe that $HfSiO_x$ is still more suitable than HfO_2 for the gate dielectric of future poly-Si TFTs. The reasons are as follows. First, $HfSiO_x$ has smaller leakage current and larger breakdown field than HfO_2 due to the amorphous nature of $HfSiO_x$ after processing. In particular, the value of gate leakage current density decreases from 7.60E-8 to 4.70E-9 A/cm^2 at $V_{\rm gs} = -10$ V, and the breakdown field increases from -4 to -7 MV/cm (data not shown) for $HfSiO_x$ compared with HfO_2. Second, TFTs with $HfSiO_x$ show 0.73 times improvement in hole mobility, over the conventional TFTs using deposited-SiO_2 dielectric, rather than degraded mobility for the case of TFTs with HfO_2. According to the previous reports [13]–[15], we speculated that the degraded mobility of TFTs with HfO_2 dielectric was due to the additional Coulomb scattering caused by the charges in the HfO_2 dielectric.

In order to further clarify the mechanism of OFF-state current, the activation energies of the different gate dielectrics were calculated from the $I_d - V_{\rm gs}$ curves obtained at 25 °C, 50 °C, 75 °C, 100 °C, and 125 °C. The dependence of activation energy on $V_{\rm gs}$ with $V_{\rm ds} = -0.1$ V is shown in Fig. 4. It can be seen that TFTs with HfO_2 have the lowest minimum leakage current due to their highest activation energy. However, with increasing $|V_{\rm gs}|$ in the OFF-state regime, the activation energy of TFTs with HfO_2 decreases drastically which causes the OFF-state current to increase rapidly. Although TFTs with $HfSiO_x$ show slightly

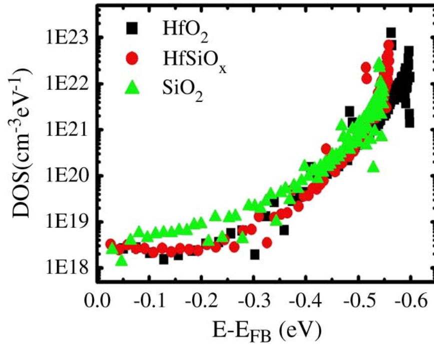

Fig. 3. Density of states extracted from transfer characteristics ($V_{\rm ds} = -0.1$ V) of poly-Si TFTs using different gate dielectrics.

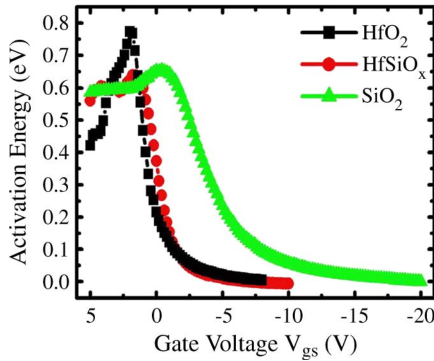

Fig. 4. Channel activation energy obtained from temperature dependence of transfer characteristics ($V_{\rm ds} = -0.1$ V) of poly-Si TFTs using different gate dielectrics.

higher minimum leakage current than TFTs with HfO_2, the OFF-state current can be improved due to the slowly decreasing activation energy of TFTs with $HfSiO_x$. Regarding the leakage mechanism of poly-Si TFTs [16]–[19], the OFF-state current, which is related to Frenkel–Poole emission mechanism, is strongly dependent on the peak electric field $E_{\rm pk}$ at the drain junction and is dominated by the vertical electric field at the interface, then

$$I_{\rm FE} \propto \exp\left(\sqrt{E_{\rm pk}}\right)$$
$$E_{\rm pk} = \frac{(V_{\rm gs} - V_{\rm ds} - V_{\rm fb})\varepsilon_{\rm gate\ dielectric}}{(T_{\rm gate\ dielectric}\varepsilon_{\rm Si})}$$

where $\varepsilon_{\rm Si}$ and $\varepsilon_{\rm gate\ dielectric}$ are the permittivities of Si and gate dielectric, respectively, $V_{\rm fb}$ is the flat-band voltage, and $T_{\rm gate\ dielectric}$ is the physical thickness of the gate dielectric. Poly-Si TFTs using high dielectric-constant gate dielectric will exhibit higher peak electric filed, causing a rapidly increasing OFF-state current.

IV. Conclusion

In this letter, high-performance p-channel poly-Si TFTs using hafnium-silicate gate dielectric are demonstrated using low-temperature processing. Higher $I_{\rm ON}/I_{\rm OFF}$ current ratio, smaller SS, lower threshold voltage, and higher mobility than those with conventional deposited-SiO_2 gate dielectric are achieved. Our results suggest that $HfSiO_x$ is a potential candidate for the gate-dielectric material of future high-performance poly-Si TFTs.

Acknowledgment

The authors would like to thank M.-H. Lee and Dr. H.-C. Lin for the support of computer software.

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