A Program-Erasable High-κ $Hf_{0.3}N_{0.2}O_{0.5}$ MIS Capacitor With Good Retention

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***Abstract*—We describe a programmable-erasable MIS capacitor with a single high-κ $Hf_{0.3}N_{0.2}O_{0.5}$ dielectric layer. This device showed a capacitance density of $\sim$6.6 fF/μm^2, low program and erase voltages of +5 and −5 V, respectively, and a large ΔV_{fb} memory window of 1.5 V. In addition, the 25 °C data retention was good, as indicated by program and erase decay rates of only 2 and 6.2 mV/dec, respectively. Such device retention is attributed to the deep trapping level of 1.05 eV in the $Hf_{0.3}N_{0.2}O_{0.5}$.**

***Index Terms*—Capacitor, dynamic random access memory (DRAM), erase, high-κ, nonvolatile memory (NVM), program.**

I. Introduction

CAPACITORS are essential devices for various analog, RF, and DRAM functions [1]–[8] in circuits. It is also desirable to have a program-erasable nonvolatile memory (NVM) function [9]–[17] to integrate low-cost embedded Flash memory into CMOS technology. To address these issues, we have previously described a program-erasable AlN MIS capacitor, which used a charge-trapping mechanism [9]–[11]. Although small degradation was achieved at room temperature and much better than a SiN MIS device [17], the data retention at 100 °C was poor due to charge detrapping. Recently, an HfNO metal–oxide–nitride–oxide–semiconductor (MONOS) NVM with a lower N content (< 10%) has been demonstrated with a record low program/erase (P/E) voltage, at a speed of 100 μs [16]. In this paper, we describe an improved device that incorporates a high-κ $Hf_{0.3}N_{0.2}O_{0.5}$ with a large N content of 20%, where a deeper trapping energy and/or a smaller band offset are expected from increasing the N% [14]–[16]. A large memory window, with a flat-band voltage difference (ΔV_{fb}) of 1.5 V, was measured under ±5-V and 1-ms P/E conditions. Furthermore, the data retention showed very small P and E decay rates (2 and 6.2 mV/dec, respectively) at 25 °C and still good at 100 °C with small values of 104 and 116 mV/dec, respectively [11]–[16]. The better high-temperature retention than that of AlN MIS capacitor was due to the deep trapping energy of the $Hf_{0.3}N_{0.2}O_{0.5}$.

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II. Experimental Details

The MIS devices were formed by sputter-depositing a $\sim$29-nm-thick $Hf_{1-x-y}N_xO_y$ dielectric on Si substrate, under mixed O_2 and N_2 with controlled O_2/N_2 flow ratio. After a postdeposition annealing, a TaN layer was deposited and patterned to form the top electrode. Finally, the devices were given a rapid thermal annealing at 900 °C for 30 s to evaluate the thermal stability. X-ray photoelectron spectroscopy (XPS) was used to determine that the composition was $Hf_{0.3}N_{0.2}O_{0.5}$. The HfNO for NVM [16] is different from that used as a CMOS gate dielectric [18], [19]: the former is optimized for large charge trapping, with a high N content, whereas the latter requires a small N% to improve the high-temperature stability to give a low trap density. The HfNO with N = 20% is chosen by considering the increasing trapping energy with N% increase, but which is low enough to prevent metallic conduction. The formed HfNO shows good reproducibility by controlling the O_2/N_2 flows during reactive sputtering from an Hf target [16]. Even better reproducibility can be reached by atomic layer deposition. The fabricated 100 × 100 μm devices were characterized by I–V and C–V measurements. A pulse generator was used for the P/E study.

III. Results and Discussion

In Fig. 1(a) and (b), we show the C–V characteristics and ΔV_{fb} time dependence of the high-κ $Hf_{0.3}N_{0.2}O_{0.5}$ MIS capacitors, respectively. The devices showed a capacitance density of 6.6 fF/μm^2 and a κ value of $\sim$22. The $|V_{fb}|$ increases with P/E time, as does ΔV_{fb} with increasing P/E voltage. This suggests that the V_{th} shift mechanism is caused by charge trapping. We found a switching speed of $\sim$1 ms due to the rapid increase in ΔV_{fb} between 0.1 and 1 ms and the approximate saturation for times from 1 to 100 ms. From the ΔV_{fb} shift for P/E conditions of ±5 V for 1 ms, a memory window of 1.5 V was measured, which is larger than that of an AlN device [9] and is comparable with certain silicon–oxide–nitride–oxide–silicon

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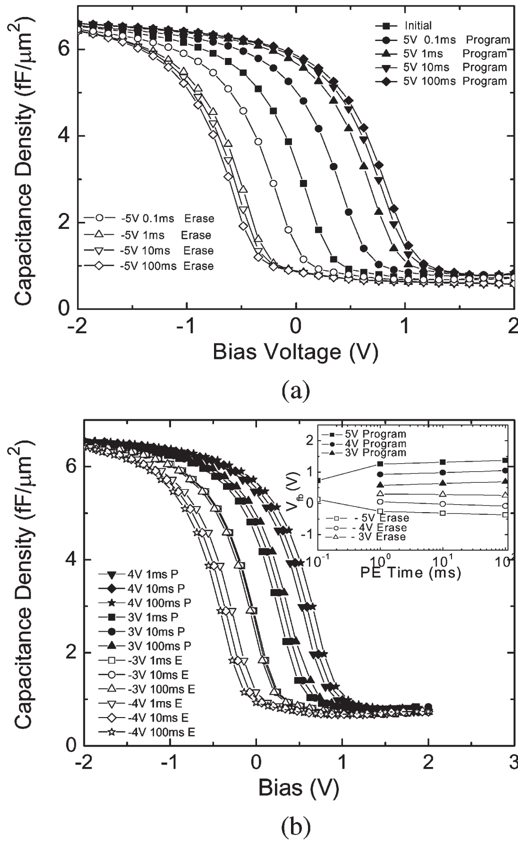

Fig. 1. (a) C–V characteristics of the $\mathrm{Hf_{0.3}N_{0.2}O_{0.5}}$ MIS capacitor after applying a ±5-V P/E voltage for various periods from 0.1 to 100 ms. (b) C–V for various P/E voltages from ±3 to ±5 V, as a function of the P/E time. The insert shows the $V_{\mathrm{fb}} - P/E$ time plot.

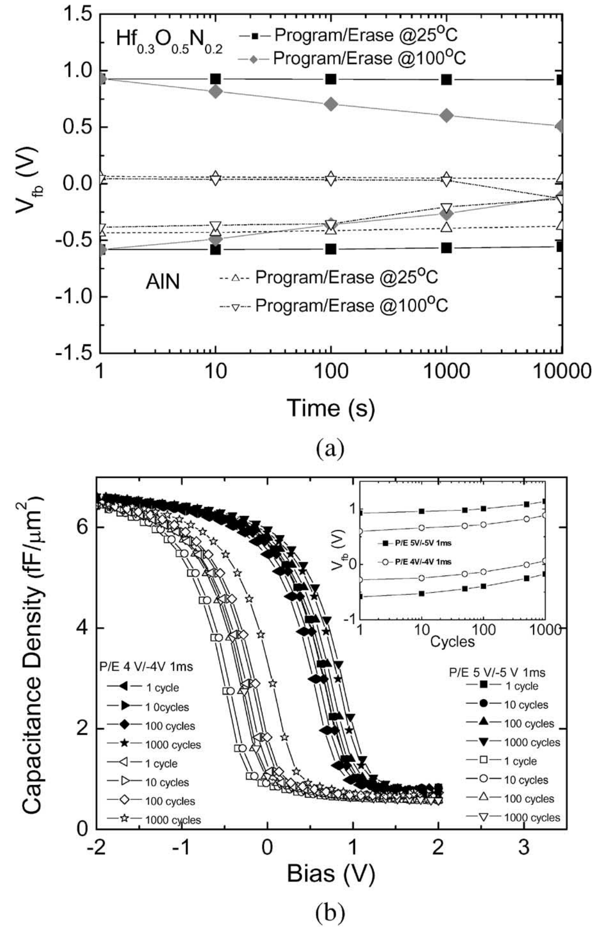

Fig. 2. (a) Retention characteristics at 25 °C and 100 °C of the $\mathrm{Hf_{0.3}N_{0.2}O_{0.5}}$ MIS capacitor, measured to 10 000 s, after a 1-ms ±5-V P/E writing pulse. (b) Cycling characteristics of the $\mathrm{Hf_{0.3}N_{0.2}O_{0.5}}$ MIS capacitor. Data for an AlN MIS capacitor are shown for comparison in (a). The insert in (b) shows the variation of V_{fb} with cycling.

NVM [13] data. Note that both the 6.6 fF/μm^2 capacitance density and the 9× tunability are larger than those for current varactors made in IC foundries [20] (typically only 1.3 fF/μm^2 density and 2.1× tunability) and are comparable with values for advanced varactors [21], [22]. The 5-V operation voltage is also useful for certain I/O circuits and is suitable for RF IC.

Fig. 2(a) and (b) shows the retention and cycling characteristics. The retention data indicate P and E decay rates of only 2 and 6.2 mV/dec, respectively, at 25 °C. At 100 °C, still good P and E decay rates of 104 and 116 mV/dec, respectively, are obtained [11]–[13]. Moreover, the retention of this $\mathrm{Hf_{0.3}N_{0.2}O_{0.5}}$ device is significantly better than that of an AlN MIS capacitor, which had a closed memory window at 10 000 s at 100 °C. A memory window of 1.3 or 0.9 V was preserved under ±5 or ±4 V, 1-ms P/E for 10^3 cycles, respectively, which indicates the good device characteristics. Note that the use of a higher N% in HfNO did not degrade the erase speed and reliability. From previous T-Supreme and Medici simulation, the erase mechanism is primary due to hole injection from the Si channel [15]. Therefore, the cycling stress reliability is comparable with our results for AlN. We note that the cycling characteristics can be improved by adding a thin tunnel oxide at the HfNO/Si interface, similar to MONOS [14]–[17] and double-tunneling TaN/Al203/SiN/Si02/Si (TANOS) cases [25].

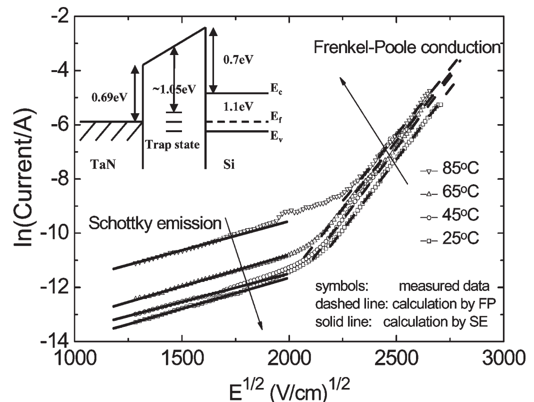

Fig. 3. $\ln(J) - E^{1/2}$ plot, using the measured I–V of a $\mathrm{TaN/Hf_{0.3}N_{0.2}O_{0.5}/Si}$ MISFET device, where the electron injection is from the Si. Calculated data using both SE and FP conduction models are included. The inserted figure shows the band diagram of the $\mathrm{Hf_{0.3}N_{0.2}O_{0.5}}$ MISFET devices, where the barrier height and trap energy were obtained from SE and FP fits to the measured data.

We plot the $\ln(J) - E^{1/2}$ relation in Fig. 3 using the measured I–V data from MISFET device, where the electron injection is from the Si under inversion. The linear

$\ln(J) - E^{1/2}$ relations fit a Schottky emission (SE) or Frenkel–Poole (FP) conduction [8] model at 25 °C, 45 °C, 65 °C, and 85 °C. In the expression

$$J \propto \exp\left[(\gamma E^{1/2} - q\varphi_{b,t})/kT\right], \quad \gamma = \left(q^3/\eta\pi\varepsilon_0\kappa_\infty\right)^{1/2}. \quad (1)$$

$\eta = 1$ for the FP case and 4 for the SE case, which implies different slopes (γ) in a $\ln(J) - E^{1/2}$ plot. The extracted low-field SE barrier height $q\varphi_b$ and high-field FP trap energy $q\varphi_t$ are plotted in the inserted figure. The data give a small SE barrier height of 0.7 eV and a dominant FP trap energy of 1.05 eV. The small barrier height, deep trap energy, and the corresponding better retention data suggest that the trap energy is deeper than that in our previous AlN MONOS [14], [15]. The merits of using the $\ln(J) - E^{1/2}$ relation for extracting the trap energy and barrier height are its accuracy ($< 6 \sim 12\%$ error for changing dielectric thickness by more than 2× [23]) and its simple experimental setup, compared with methods that require both high-resolution XPS and reflection electron energy loss spectroscopy [24].

IV. Conclusion

We have demonstrated a program-erasable $Hf_{0.3}N_{0.2}O_{0.5}$ MIS capacitor with good 100 °C data retention and high 6.6 fF/μm^2 density. This new capacitor should find wide applications for analog, RF, DRAM, and low-cost embedded Flash memory.

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