

行政院國家科學委員會補助專題研究計畫成果報告

高度微縮金氧半電晶體應變工程及物理機制之研究

Strain Engineering and its Physical Mechanisms in Highly Scaled MOSFETs

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一、中文摘要

本計畫為期三年，針對應變矽技術重要議題進行研究，如應力量測、雜質擴散、通道背向散射、表面缺陷密度、微觀物理、以及製程演進等。第一年將進行下列項目(針對佈局引致應力的 n 型金氧半電晶體且特性尺度低至 40 奈米左右): (1)量測閘極介電層穿隧電流以反推通道內部應力。同一元件上的載子遷移率和臨界電壓將一併萃取，也將萃取通道背向散射係數; (2)量測邊緣直接穿隧電流以得到特定應力下所造成的橫向擴散; (3)使用低頻雜訊量測技術萃取出介面缺陷密度，也將提出並量化物理模式；(4)運作嶄新串聯電阻萃取方法，並檢驗串聯電阻所造成的影響; 以及(5)進行計算電洞能帶結構在不同應力大小及方位下的重要物理參數值。第二年除繼續強化前一年研究品質外，亦將進行下列項目(針對佈局引致應力的 p 型金氧半電晶體且特性尺度低至 40 奈米左右): (1)量測閘極介電層穿隧電流以反推通道內部應力大小。同一元件上的載子遷移率和臨界電壓將一併萃取，也將萃取通道背向散射係數; (2)量測邊緣直接穿隧電流決定橫向擴散; (3)使用低頻雜訊量測技術萃取出介面缺陷密度，強化物理模式; 以及(4)進行金屬閘高 K 介電層電晶體完整的應變下電性量測: 次臨界電流、閘極電流、邊緣電流、基座電流、載子遷移率、臨界電壓、介電層與矽介面缺陷密度等，並與物理模式作一關聯。第三年除繼續強化前兩年研究品質外，亦將進行下列項目(針對佈局技術製造應力電晶體且特性尺度可望至 32 奈米以下): (1)量測其閘極介電層電流反推通道內部應力大小。同一元件上的載子遷移率和臨界電壓將一併萃取，也將萃取通道背向散射係數; (2)量測邊緣電流以得到特定應力下所造成的橫向擴散; (3)使用低頻雜訊量測技術萃取出元件的介面缺陷密度; 以及(4)繼續強化電性量測與金屬閘高 K 介電層電晶體物理模式的關聯，並建立通道內部應力之物理模式。最終我們將整合所有不同實驗條件下萃取的應力值嘗試提出一個三維應力物理模式。此模式的驗證將與文獻數據作一比較，並嘗試納入介電層與矽介面的缺陷密度物理模式，機械應力下雜質擴散物理模式，次臨界電流物理模式，閘極電流物理模式，邊緣電

流物理模式，基座電流物理模式，載子遷移率物理模式，臨界電壓物理模式等，以為應變工程實際所用。

關鍵詞:

應變，應力，金氧半電晶體，擴散，奈米，散射，穿隧，介電層，缺陷

英文摘要

This is a three-year project dedicated to the strained silicon engineering in highly scaled MOSFETs concerning the stress measurement, dopant diffusion, channel backscattering, interface states, microscopic physics, and aggressively scaled process technologies. In the first year, the following items will be carried out (primarily on n-MOSFETs with the layout induced stress and with the feature size down to 40 nm or so): (1) measurement of channel stress via the gate tunneling current; also extracted are the carrier mobility and threshold voltage, as well as the channel backscattering coefficient, on the same devices; (2) measurement of dopant diffusion near the source/drain corner via edge direct tunneling; (3) measurement of interface states via the low-frequency noise, along with the quantified physical models; (4) with the novel series resistance extraction method, the effect of series resistance will be highlighted; and (5) calculation of the important physical parameters for the hole's band structures under the stress magnitude and orientation. The goal of the second year is that we will further strengthen the quality of the works in the first year. Besides, we will explore the additional items (primarily on p-MOSFETs with the layout induced stress and feature size down to 40 nm or so): (1) measurement of channel stress via gate direct tunneling; also extracted on the same devices are the carrier mobility and threshold voltage, as well as the channel backscattering coefficient; (2) measurement of lateral diffusion via edge direct tunneling; (3) measurement of the interface states using the low-frequency noise along with the enhanced physical models; and (4) comprehensive electrical measurements for metal-gate/high-K strained MOSFETs, such as subthreshold current, gate current, edge current, substrate current, carrier mobility, threshold voltage, and interface states, along with a linkage to the underlying physical models. As to the third year, we will also enhance the quality of the works over the past two years. In addition,

the following items will be conducted (primarily on the layout induced stress and with the feature size expected down to 32 nm and beyond): (1) measurement of channel stress via gate current; also extracted on the same devices are the carrier mobility and threshold voltage, as well as the channel backscattering coefficient; (2) measurement of lateral diffusion via edge current; (3) measurement of the interface states using the low-frequency noise along with the updated physical models; and (4) elaborating on the relation between electrical characteristics and physical mechanisms underlying the metal-gate/high-K strained MOSFETs. Eventually, we will integrate all experimentally determined stress values with the aim of constructing a 3-D stress physical model. The validity of the 3-D model will be compared with literature data while the followings will be incorporated as well: the interface states physical model, the stress induced dopant diffusion physical model, the subthreshold current physical model, the gate current physical model, the edge current physical model, the substrate current physical model, the carrier mobility physical model, the threshold voltage physical model, etc. The resulting integration tool can find practical applications in the areas of strain engineering.

Key Words:

Strain, Stress, MOSFETs, Diffusion, Nano, Scattering, Tunneling, Dielectric, Defects

二、緣由與目的

應變矽技術最近已被廣泛應用在奈米 CMOS 製程技術中。主要有二種不同的方法在製程中加入應力：(1) 在矽鍍基板上長出磊晶矽原子層；以及(2) 利用製程步驟本身及材料性質差異製造應力，如：淺塹渠絕緣、覆蓋層、矽化物或者矽鍍源汲極等。至目前為止，針對機械應力的重要性有兩個主要的探討方向。其一是晶圓在生產過程所感受的機械應力會增強或減緩雜質的擴散，也因此影響最終摻雜在元件之中分佈的情形。在做了上述這些製程的改變後，檢驗應變矽元件表面特性及閘級介電層的健全度是否受到影響是很重要的。另一方面，機械應力也可改變元件的能帶結構，因之改變了電晶體特性，諸如載子遷移率、熱載子造成的可靠度問題、臨界電壓和閘極直接穿隧電流等。

憑仗這幾年的努力，我們已在應變矽技術領域產出重要成果：

(1) 利用閘極直接穿隧電流估算應變矽金氧半場效電晶體通道應力大小

能夠定量的推斷出元件結構內部的應力大小及應力的種類(如：壓縮應力、伸張應力)是必要的。目前已經有三種評估元件結構內部應力的方法被提出：(1) 彎曲晶圓夾具，(2) 精密的應力模擬，及(3) 拉曼光譜。但是利用電晶體電性改變來推斷內部應力大小及種類的方法仍未被提出過。然而，值得一提的是經由外部施加應力造成的閘極直接穿隧電流改變已經被深入的探討過了。另一方面，根據最近的研究，形變能係數已經可由實驗萃取而得，並且和理論計算所預測的值一致。因此，在形變能係數已知的情況下，利用閘級穿隧電流來反推元件內部應力大小已經變成一個可行的方案。研究細節可參考我們發表的相關文獻：

- C. Y. Hsieh and M. J. Chen, "Measurement of channel stress using gate direct tunneling current in uniaxially stressed n-MOSFETs," *IEEE Electron Device Letters*, vol.

28, pp. 818-820, Sept. 2007.

(2) 應力製程微觀物理

我們在產製下世代受應力電子元件 Strain Engineering 領域針對 Uniaxial Strain 下 Impurities (為目前國際上高度挑戰卻也爭議性極大的題目) 在 Silicon 的高溫特殊擴散行為提出前所未有、創新微觀物理模式並獲得實驗強力支持。且藉由成熟的元件製程模擬，所謂的 TCAD(製程電腦輔助設計)，可以延伸到實際元件的應用。研究細節可參考我們發表的相關文獻：

- M. J. Chen and Y. M. Sheu, "Effect of uniaxial strain on anisotropic diffusion in silicon," *Applied Physics Letters*, Vol. 89, pp. 161908-1-181908-3, Oct., 2006.

- Y. M. Sheu, S. J. Yang, C. C. Wang, C. S. Chang, L. P. Huang, T. Y. Huang, M. J. Chen, and C. H. Diaz, "Modeling mechanical stress effect on dopant diffusion in scaled MOSFETs," *IEEE Trans. Electron Devices*, vol. 52, pp. 30-38, January 2005.

(3) 藉由邊緣直接穿隧電流量測在機械應力下雜質的擴散情況

能夠擁有從電性量測反推元件因生產過程而增強或是減低雜質擴散的能力是不可或缺的。傳統上，這是由 TCAD 來達成。我們提出了一個電性的方法，稱之為邊緣直接穿隧電流的方式，可直接地決定在源極及汲極的局部機械應力對摻雜在通道中橫向的擴散。研究細節可參考我們發表的一篇長文：

- C. Y. Hsieh and M. J. Chen, "Electrical measurement of local stress and lateral diffusion near source/drain extension corner of uniaxially stressed n-MOSFETs," *IEEE Trans. Electron Devices*, vol.55, pp. 844-849, March 2008.

(4) 量測應變矽 MOSFETs 閘級介電層與矽介面的缺陷密度

在做了應變製程的改變後，檢驗應變矽元件表面特性及閘級氧化層介面的健全度是否受到影響是很重要的。而我們最近進行的應變矽 MOSFETs 元件的 1/f 低頻雜訊量測正好可以作為此一議題深入分析的有效工具。研究細節可參考我們發表的相關文獻：

- M. P. Lu, W. C. Lee, M. J. Chen, "Channel-width dependence of low-frequency noise in process tensile-strained n-channel metal-oxide-semiconductor transistors," *Applied Physics Letters*, vol. 88, pp. 063511-1—063511-3, Feb. 2006.

- C. Y. Hsieh, Y. T. Lin, T. H. Liang, W. C. Lee, J. B. Bouche, and M. J. Chen, "Effect of STI mechanical stress on p-channel gate oxide integrity," *IEEE Semiconductor Interface Specialist Conference*, p.5, 2007 (Arlington).

我們另有其他貢獻於應變矽技術領域者：

在國際上，從事應變矽技術的研究者在 *IEEE Symposium on VLSI Technology* 國際會議上引用了我們的成果。給予三例：

- H. Tsuno, K. Anzai, M. Matsumura, S. Minami, A. Honjo, H. Koike, Y. Hiura, A. Takeo, W. Fu, Y.

Fukuzaki, M. Kanno, H. Ansai, and N. Nagashima, "Advanced analysis and modeling of MOSFET characteristics fluctuation caused by layout variation," *IEEE Symposium on VLSI Technology*, p. 204, 2007.

- V. Barral, et al., "Will strain be useful for 10nm quasi-ballistic FDSOI devices? An experimental study," *IEEE Symposium on VLSI Technology*, p. 128, 2007.

- H. N. Lin, et al., "The impact of uniaxial strain engineering on channel backscattering in nanoscale MOSFETs" *IEEE Symposium on VLSI Technology*, p. 174, 2005.

我們培育出應變矽技術的頂尖人才。給予兩例：

- 許義明博士: 2007 年畢業(with Ph.D. Dissertation entitled "Layout Dependent Effect on Advanced MOSFETs") 即成為 TSMC RD Manager. TCAD and Device Engineering 領域權威, 曾發表多篇 IEDM 及 Symposium on VLSI Technology 會議論文。

- 黃煥宗博士: TSMC 32/22 奈米 RD 技術經理; 2003-2005 年選派為 Scientist to Freescale Company, USA. 曾發表多篇 IEDM 及 Symposium on VLSI Technology 會議論文; 今年就以第一作者領銜一篇 IEDM 論文:

H. T. Huang, et al., "45nm high-k/metal-gate CMOS technology for GPU/NPU applications with highest PFET performance," *IEEE IEDM Tech. Dig.*, p. 285, 2007.

然而, 應變矽技術領域至深且廣, 現階段已湧現諸多議題:

(1) 串聯電阻對應力量測之影響

源汲極串聯電阻會造成額外的電位降, 減少本質電壓, 並且降低驅動能力。當通道長度減少的時候, 串聯電阻所佔比例也越大, 這將使驅動電流降低的問題將會越來越嚴重。因此源汲極串聯電阻將對上面提到的應力量測產生不可忽視的誤差, 特別是在小於 100 奈米的應變矽奈米尺寸金氧半電晶體中。但問題是產業標準的 Shift and Ratio 方法已經很久不採用了。

經過長久的努力我們最近已經提出了一個新的方法來萃取串聯電阻, 並經由實驗驗證, 且不需要考慮閘極或通道長度。這個方法是在一個載子遷移率(mobility)保持定值的電壓區間內操作, 而不需要考慮臨界電壓調整及摻雜擾動所造成的不同通道摻雜濃度。這個方法和以往不同之處在於它不需透過許多不一樣通道長度的元件和 C-V 實驗去萃取串聯電阻, 利用此新方法可以在單顆元件上簡易的萃取串聯電阻。研究細節可參考我們發表的相關文獻:

- D. W. Lin, M. L. Cheng, S. W. Wang, C. C. Wu, and M. J. Chen, "A constant mobility method to enable MOSFET series resistance extraction," *IEEE Electron Device Letters*, vol. 28, pp. 1132-2234, December, 2007.

(2) P-MOSFET 應力量測

由於 Holes 本身的 Band Structures 就極特殊, 雖然我們已有能計算 Hole Direct Tunneling 的論文發表:

- K. N. Yang, H. T. Huang, M. J. Chen, Y. M. Lin, M. H. Yu, S. M. Jang, C. H. Yu, and M. S. Liang, "Edge hole direct tunneling in off-state ultrathin gate oxide p-channel MOSFETs," *IEEE International Electron Devices Meeting (IEDM) Technical Digest*, pp. 679-682, Dec. 2000 (San Francisco).

- K. N. Yang, H. T. Huang, M. C. Chang, C. M. Chu, Y. S. Chen, M. J. Chen, Y. M. Lin, M. H. Yu, S. M. Jang, C. H. Yu, and M. S. Liang, "A physical model for hole direct tunneling current in p+ poly-gate pMOSFETs with ultrathin gate oxides," *IEEE Trans. Electron Devices*, pp. 2161-2166, Nov. 2000.

但關鍵處卻卡在 $k \cdot p$ 方法的不易, 因之我們尚未執行 P-MOSFET 應力量測。最近, 與中興大學張書通教授的合作取得 $k \cdot p$ 程式, 經初步檢驗即與文獻上數據符合, 因之此種障礙已被解決。

(3) 應變矽之通道背向散射研究

在通道背向散射(即波動導向的下世代奈米元件物理)領域, 我們這幾年完成了大量的實驗工作, 改進了原先的理論模式, 發表了一系列相關論文, 以 2002 IEDM 最為代表性:

- M. J. Chen, H. T. Huang, K. C. Huang, P. N. Chen, C. S. Chang, and Carlos H. Diaz, "Temperature dependent channel backscattering coefficients in nanoscale MOSFETs," *IEEE*

IEDM Technical Digest, pp. 39-42, Dec. 2002.

雖然如前所述從事應變矽技術的研究者在 *IEEE Symposium on VLSI Technology* 國際會議上引用了我們的此篇論文以萃取通道背向散射係數, 但我們自信可以產出更好的成果, 只是需要更為充裕的時間以及更多的應變數據。

(4) 應變與表面缺陷密度之物理關聯

我們已能並已經測量出應力下的 MOSFETs 表面缺陷密度但相關物理機制尚待量化建立。部分原因是實驗樣本數不足。另外需從純粹理論物理期刊如 *Physical Review Letters* 等尋找相似物理機制。

(5) 製程之演進

目前應變矽技術已演進入第三代(詳見於上述黃煥宗博士 2007 年 IEDM 論文)。展望未來數年, 應變矽技術將演進為 non-planar stress, 即三維化(通道長度方向, 通道寬度方向, 以及垂直於通道平面方向)。另一方面, 我們剛從工業界取得 High-K/metal gate strained MOSFETs 以及 capping layer 覆蓋層 induced stress 晶片, 尚未展開研究。

因之, 向國科會提出為期三年專題計畫書, 針對上述議題進行研究, 期盼能再度對攸關下世代奈米 CMOS 半導體產業的應變矽技術領域作出實質的貢獻。

三、研究方法與成果

方法:

進行下列項目:

(1) 利用閘極直接穿隧電流估算應變矽 n 型金氧半場效電晶體通道應力大小

我們將從工業界取得針對幾組利用佈局技術製造單軸應力(縱向或橫向)的 n-MOSFETs 元件(down to 40 nm), 並且自行製作在不同長晶方向晶圓上的不同通道方向元件, 量測其閘極介電層傳導帶電子穿隧電流。透過已知的製程參數、文獻上已發表的形變位能係數, 以及我們的閘極穿隧電流物理模型, 可以從量測到的穿隧電流對閘極電壓的關係曲線反推通道內部應力大小。之後我們也會將此方法應用到使用覆蓋層技術製造應力的元件上。為檢驗此方法的準確性, 同元件上的載子遷移率和臨界電壓將一併萃取, 並將其得到之壓電係數及能帶位移和文獻比較。佈局技巧與通道應力改變的關係將一併驗證。我們也將萃取通道背向散射係數並與通道應力作一關連。

(2) 藉由邊緣直接穿隧電流量測在機械應力下雜質的擴散情況

對於因佈局技術而造成縱向或橫向應力的 n-MOSFET, 次臨界電流將以閘極邊緣到淺塹渠絕緣之間間隙的函數呈現, 期可藉由能帶改變推測出源極及汲極的應力大小。萃取出來的局部應力會和在反轉時之閘極穿隧電流、載子遷移率與臨界電壓之量測做一量化比較。此外, 萃取出來的應力和閘極邊緣到淺塹渠絕緣間距離的關係將用來檢驗佈局技巧的有效性。在累積區時所量測之邊緣直接穿隧電流可直接得到閘極和源極與汲極的重疊面積。尤其是, 對於特定應力下所造成橫向擴散數值會具體地和製程模擬結果做比較。

(3) 量測應變矽 n-MOSFETs 閘極介電層與矽介面的缺陷密度

我們將萃取元件工作在線性區時的臨界電壓及低電場載子遷移率, 並使用低頻雜訊量測技術, 在頻率 3Hz 到 100kHz 及準平衡條件($V_D = 0.05V$)下, 以閘極過驅動

電壓作為參數，量測元件的 $1/f$ 低頻雜訊。下列公式即所謂載子遷移率-數量擾動模型將被使用在輸入參考電壓雜訊功率頻譜密度量測上。根據低頻雜訊量測即可萃取出元件的介面缺陷密度。同時我們也將提出並量化幾個元件內部應力造成介面缺陷密度改變的物理根源，例如：在閘極介電層氧化時，介面應力的鬆弛及伸張應變可減少單位面積矽原子密度，使二氧化矽和矽原子之間的晶格常數不匹配問題獲得改善。

(4) 檢驗串聯電阻對上述議題所造成之影響

運作我們的嶄新串聯電阻萃取方法，應用在上述幾個議題中，並檢驗它所造成的影響。

(5) $k \cdot p$ 程式執行及物理模式建立

進行 $k \cdot p$ 程式執行以萃取出 Holes Band Structures 在不同應力大小及方位下的重要物理參數值，並將之置於我們已有的 Hole Direct Tunneling 物理模式以為 P-MOSFET 應力量測預作準備。

成果：

- (1) 利用閘極直接穿隧電流估算應變矽 n 型金氧半場效電晶體通道應力大小，同元件上的載子遷移率和臨界電壓一併萃取，得到之壓電係數及能帶位移和文獻比較。佈局技巧與通道應力改變的關係一併驗證。通道背向散射係數與通道應力作一關連。
- (2) 邊緣直接穿隧電流量測在機械應力下雜質擴散，對於特定應力下所造成橫向擴散數值具體和製程模擬結果比較。

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7. W. H. Lee and M. J. Chen, "Gate direct tunneling current in uniaxially compressive strained nMOSFETs: A sensitive measure of electron piezo effective mass," *IEEE Trans. Electron Devices*, vol. 58, pp. 39-45, Jan. 2011.
8. M. J. Chen, C. C. Lee, and K. H. Cheng, "Hole effective masses as a booster of self-consistent six-band $k \cdot p$ simulation in inversion layers of pMOSFETs," *IEEE Trans. Electron Devices*, vol. 58, pp. 931-937, April 2011.
9. C. Y. Hsu, H. G. Chang, and M. J. Chen, "A method of extracting metal-gate high-k material parameters featuring electron gate tunneling transition," *IEEE Trans. Electron Devices*, vol. 58, pp. 953-959, April 2011.
10. M. J. Chen and C. Y. Hsu, "Evidence for a very small tunneling effective mass ($0.03 m_0$) in MOSFET high-k (HfSiON) gate dielectrics," *IEEE Electron Device Letters*, accepted and to appear in April issue of 2012.
11. M. J. Chen, L. M. Chang, S. J. Kuang, C. W. Lee, S. H. Hsieh, S. C. Chang, and C. C. Lee, "Temperature-oriented mobility measurement and simulation to assess surface roughness in ultrathin-gate-oxide (~ 1 nm) nMOSFETs and Its TEM evidence," *IEEE Trans. Electron Devices*, accepted and to appear in April issue of 2012.
12. M. J. Chen and W. H. Lee, "Evidence for the fourfold-valley confinement electron piezo-effective-mass coefficient in Inversion layers of $\langle 110 \rangle$ uniaxial tensile strained (001) nMOSFETs," *IEEE Electron Device Letters*, accepted and in press, 2012.

(3) 量測應變矽 n-MOSFETs 閘極介電層與矽介面缺陷密度，量化元件內部應力造成介面缺陷密度改變的物理根源。

(4) 檢驗串聯電阻造成之影響。

(5) 應力大小及方位下 $k \cdot p$ 程式執行及應變物理模式建立。

四、結論與討論

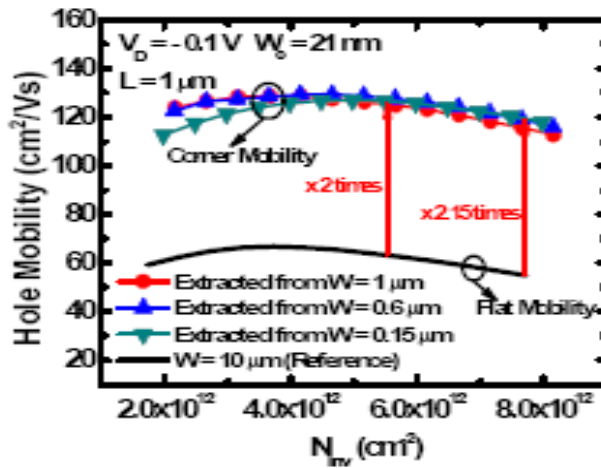
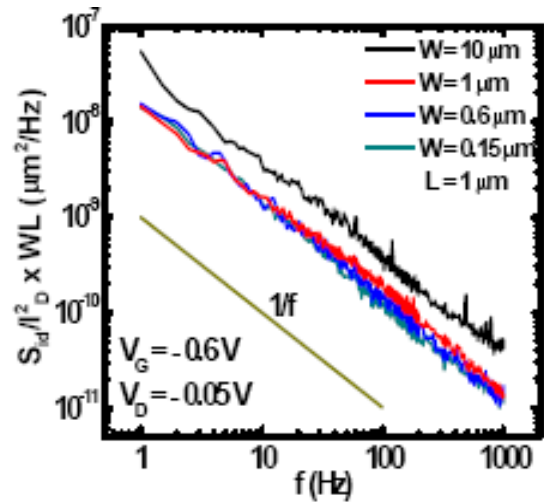
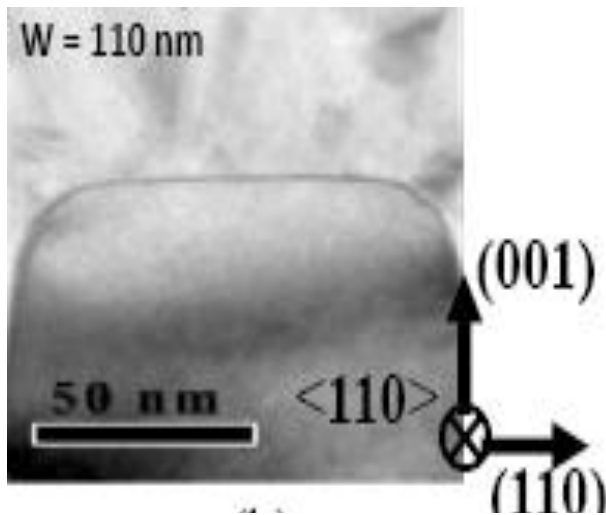
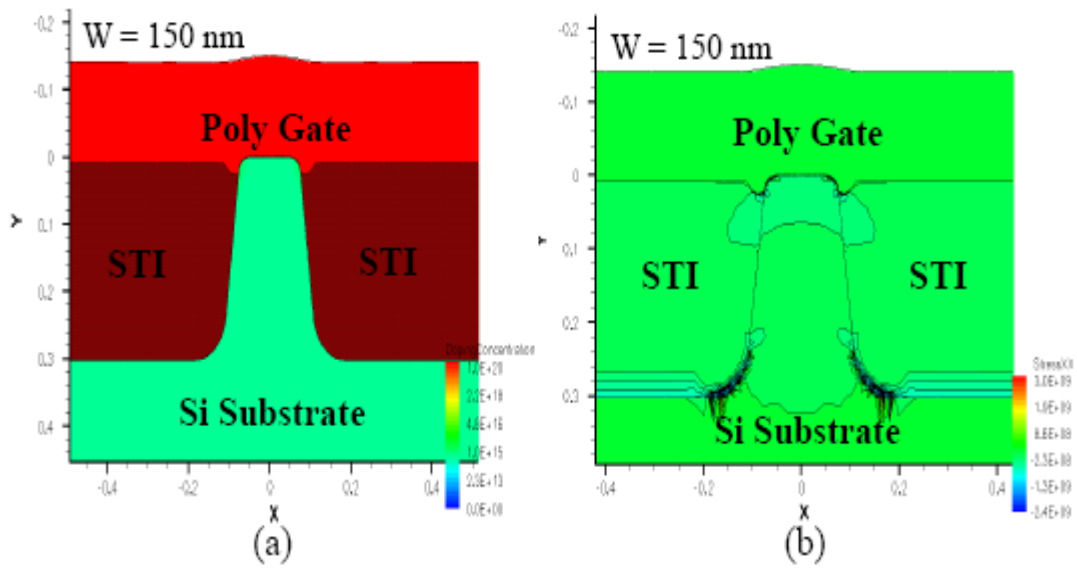
1. 發表 IEEE T-ED 期刊論文 6 篇, IEEE EDL 期刊論文 5 篇及 IEEE 會議論文 1 篇(見下參考文獻)。

2. 產生主要創新技術:

- Advanced Quantum Strain Tunneling and Mobility Simulators (Suitable for the Effects of Strain, Substrate and Channel Orientations, Temperature, n- and p-type Channel, etc.)
- Self-Consistent $k \cdot p$ Simulation Booster for Strained FETs
- Embedded-SiGe Technology
- Novel FUSI Gate Technology
- Novel HKMG Material Parameter Extraction Method
- High Mobility Sidewall Corner Structure
- Tunneling as Sensitive Monitor of Strain

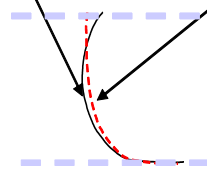
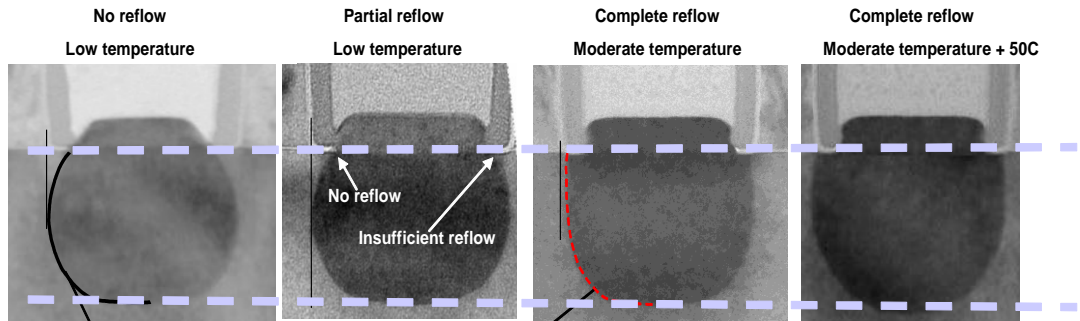
3. 2011 年產生三位博士, 林大文, 謝振宇和許智育。林大文和謝振宇現分別為台積電 RD 20 奈米部門經理及資深工程師; 許智育則為台積電 RD 14 奈米部門主任工程師。

High-Mobility Sidewall Corner Structure

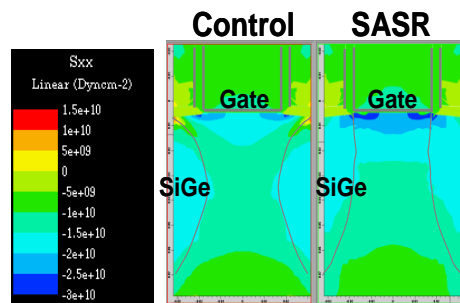


Embedded-SiGe Technology

(a)

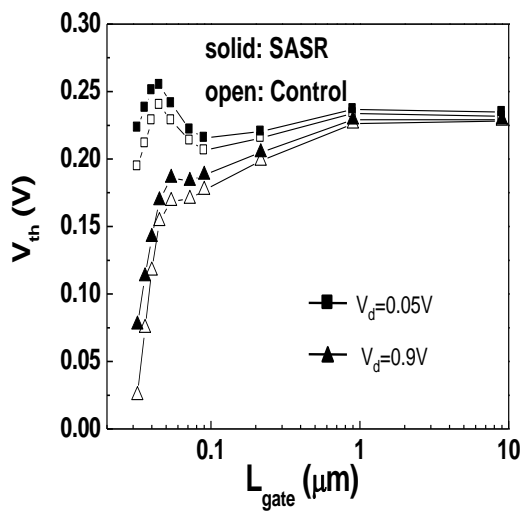


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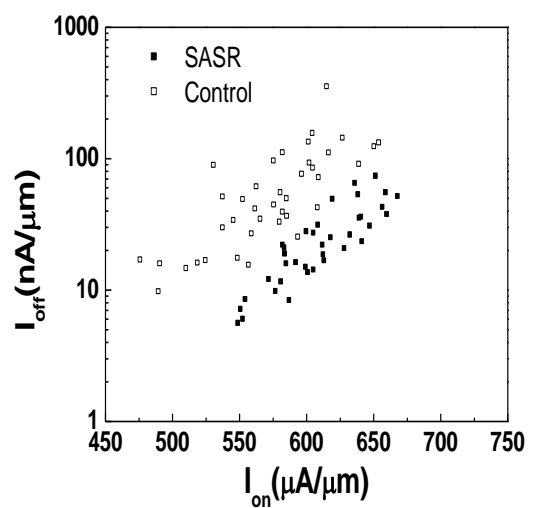


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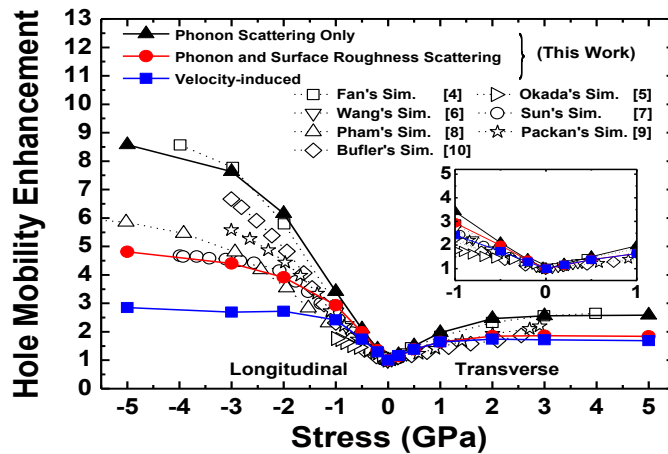
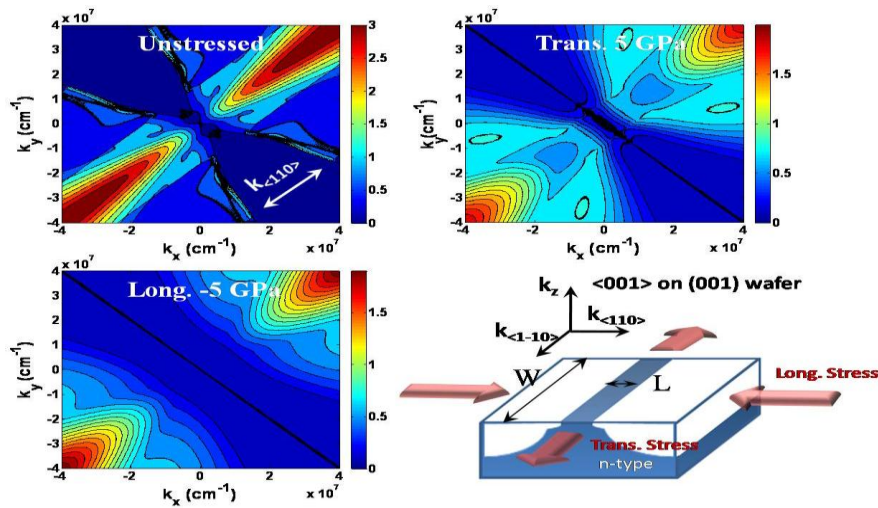
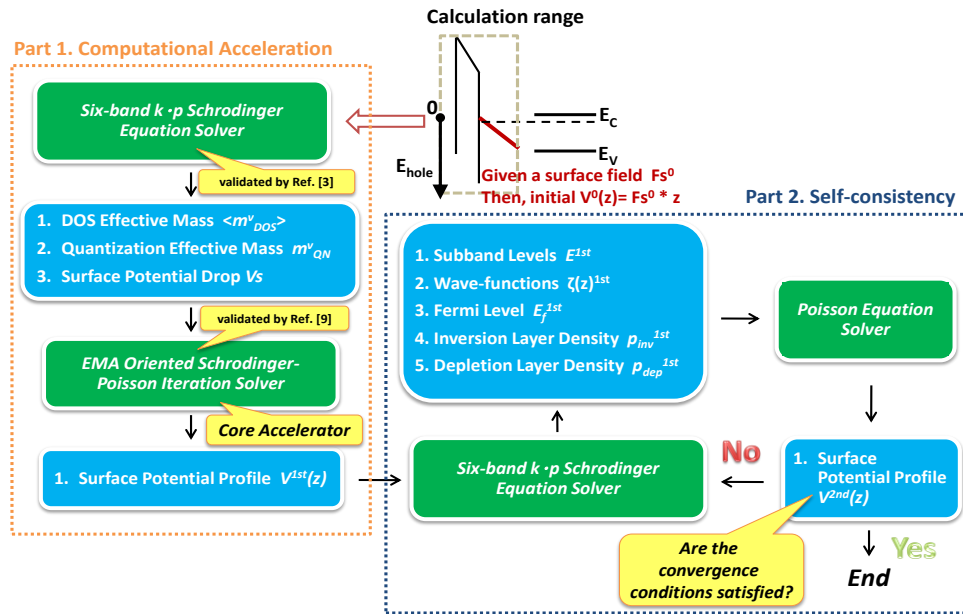
(a)



(b)

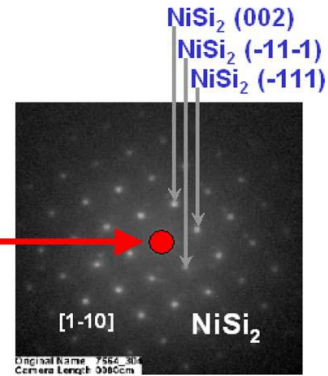


Advanced Quantum Strain Simulator

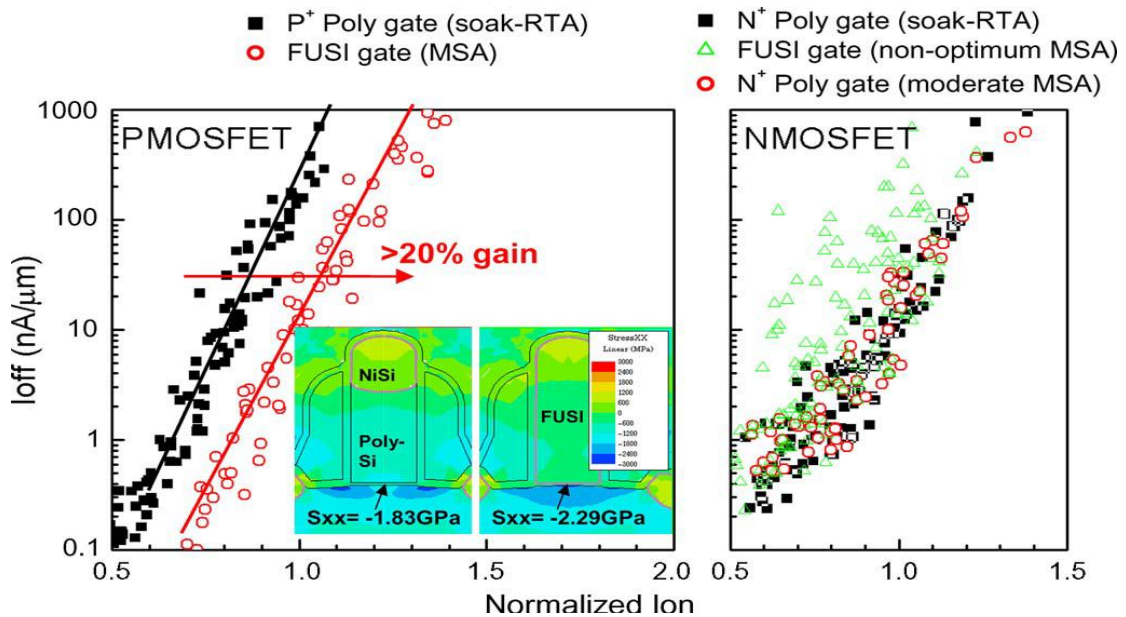


FUSI Gate Technology

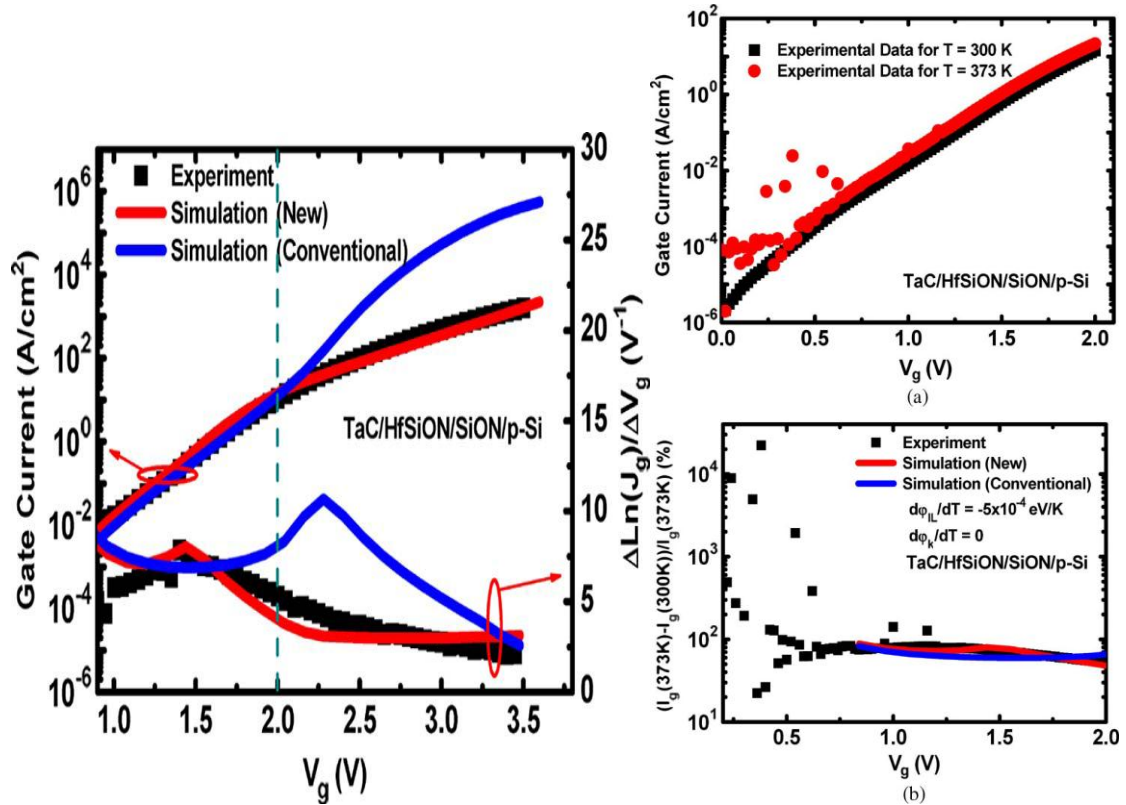
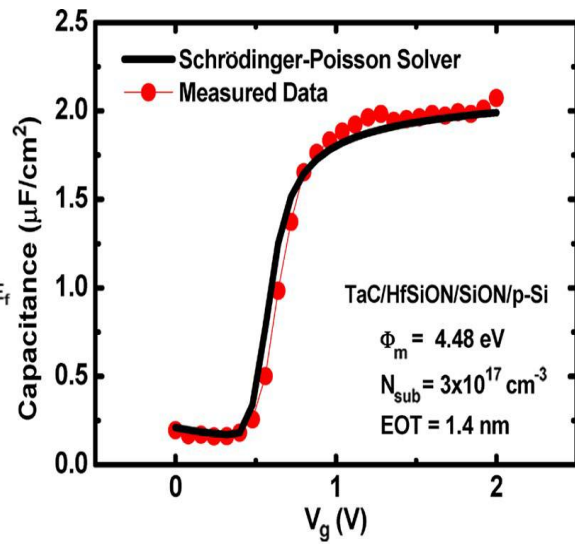
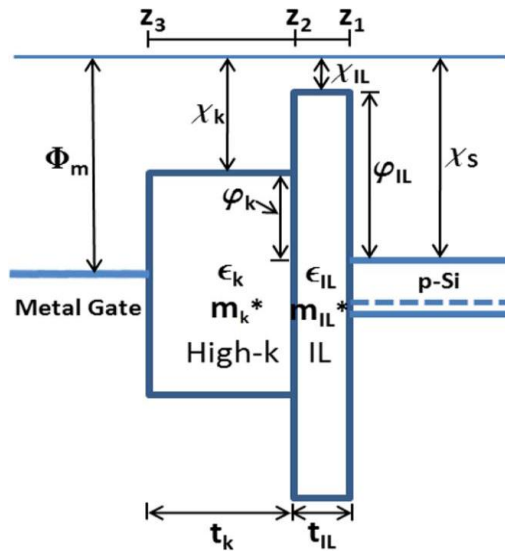
MSA Condition Anneal time ~1ms	Active region btw gates	Silicide on gate	
		NMOSFET	PMOSFET
Effective Temperature <900C	$R_s \approx 13 (\Omega/\square)$	$R_s \approx 11 (\Omega/\square)$	$R_s \approx 12 (\Omega/\square)$
	N ⁺ active $R_s \approx 22 (\Omega/\square)$	800Å	
	P_SiGe	Poly-Si gate	Poly-Si gate
Effective Temperature ~ 950C ~ 1050C	$R_s \approx 13 (\Omega/\square)$	$R_s \approx 11 (\Omega/\square)$	$R_s \approx 94 (\Omega/\square)$
	N ⁺ active $R_s \approx 16 (\Omega/\square)$	Poly-Si gate	FUSI gate
	P_SiGe	Poly-Si gate	FUSI gate
Effective Temperature >1100C	$R_s \approx 14 (\Omega/\square)$	$R_s \approx 17 (\Omega/\square)$	$R_s \approx 94 (\Omega/\square)$
	N ⁺ active $R_s \approx 16 (\Omega/\square)$	FUSI gate	FUSI gate
	P_SiGe	FUSI gate	FUSI gate



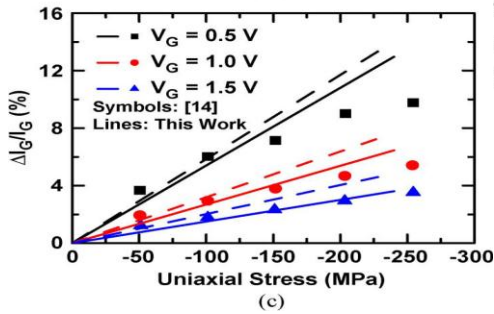
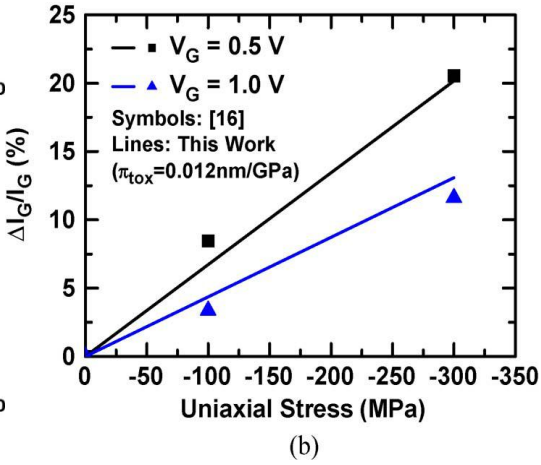
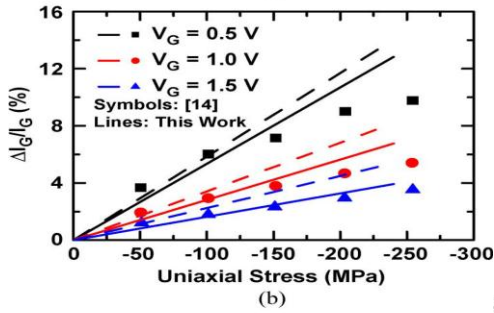
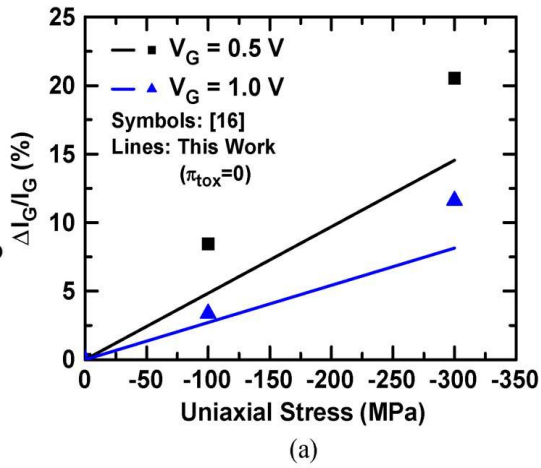
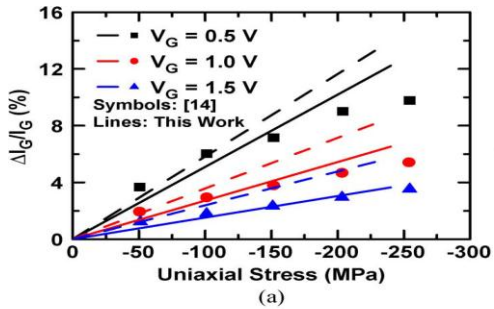
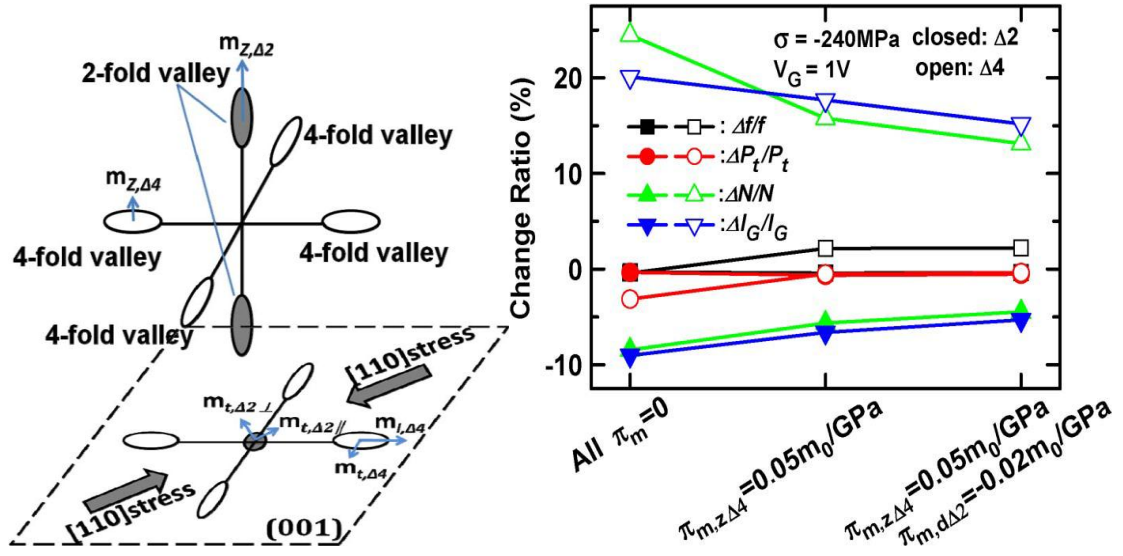
In N⁺ Poly-Si, total implanted Phosphorus dose $\geq 2E15 \text{ cm}^{-2}$
total implanted Nitrogen dose $\geq 5E14 \text{ cm}^{-2}$
In P⁺ Poly-Si, total Implanted Boron dose $\geq 2E15 \text{ cm}^{-2}$
no Nitrogen is implanted.



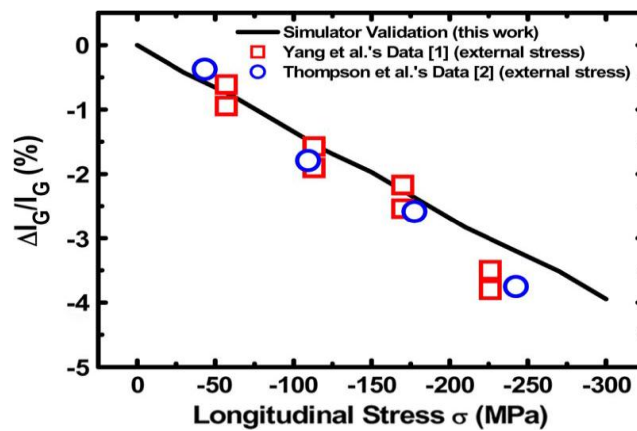
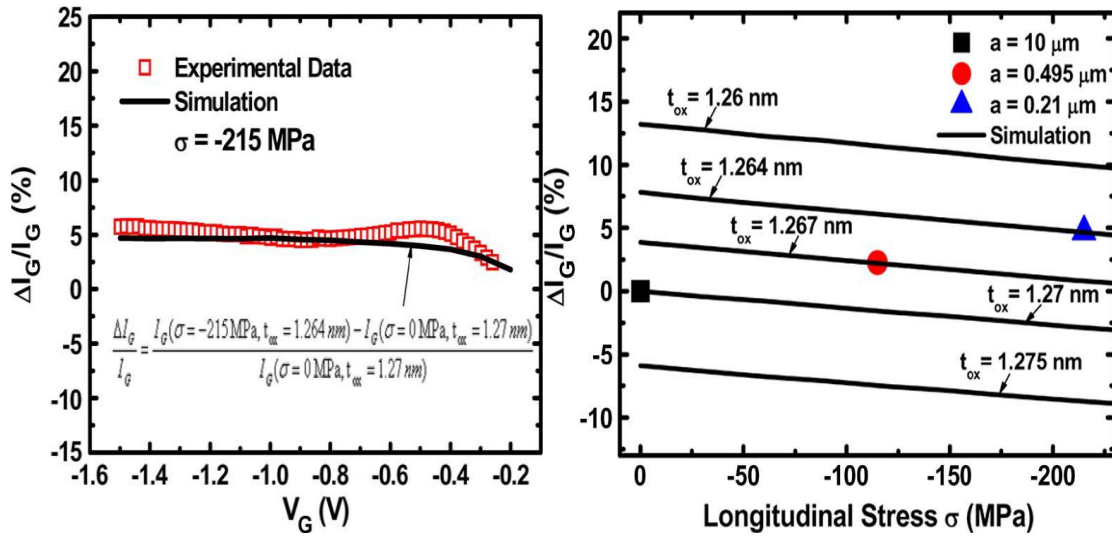
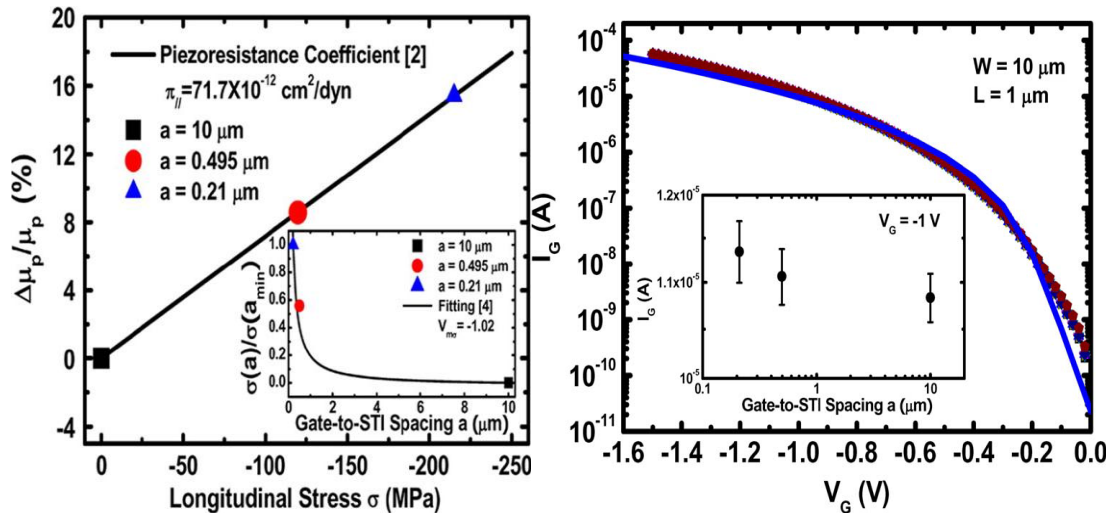
HKMG Parameter Extraction



Tunneling as Sensitive Monitor of Strain

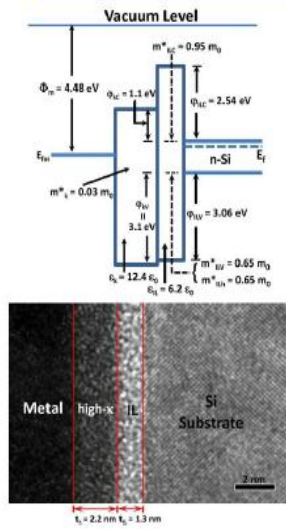


Strain Induced Oxidation Retardation



Published Results

● HKMG Stacks

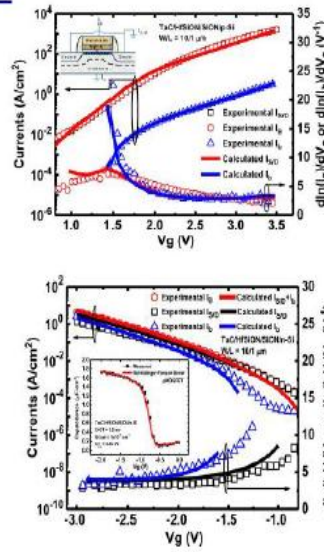


IEEE ELECTRON DEVICE LETTERS

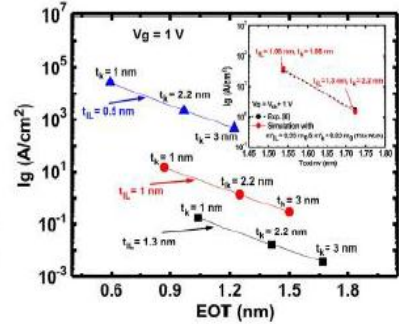
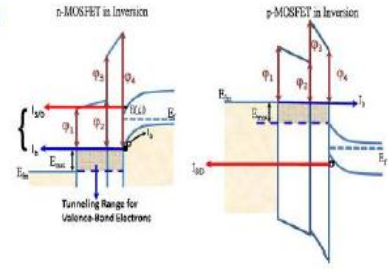
April 2012
EDL

Evidence for a Very Small Tunneling Effective Mass ($0.03m_0$) in MOSFET High- k (HfSiON) Gate Dielectrics

Ming-Jer Chen, Senior Member, IEEE, and Chih-Yu Hsu, Student Member, IEEE



IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 58, NO. 4, APRIL 2011



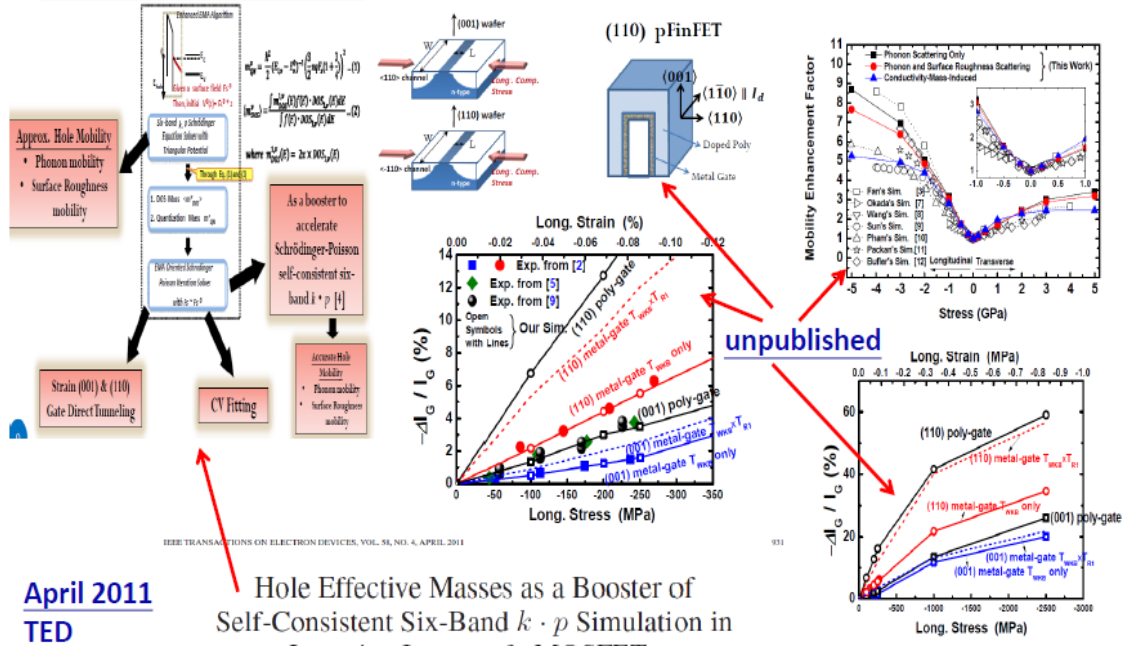
April 2011 EDL 951

A Method of Extracting Metal-Gate High- k Material Parameters Featuring Electron Gate Tunneling Current Transition

Chih-Yu Hsu, Student Member, IEEE, Hua-Gang Chang, and Ming-Jer Chen, Senior Member, IEEE

Published and Unpublished Results

● Hole Mobility Enhancement and Hole Gate Tunneling



IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 58, NO. 4, APRIL 2011

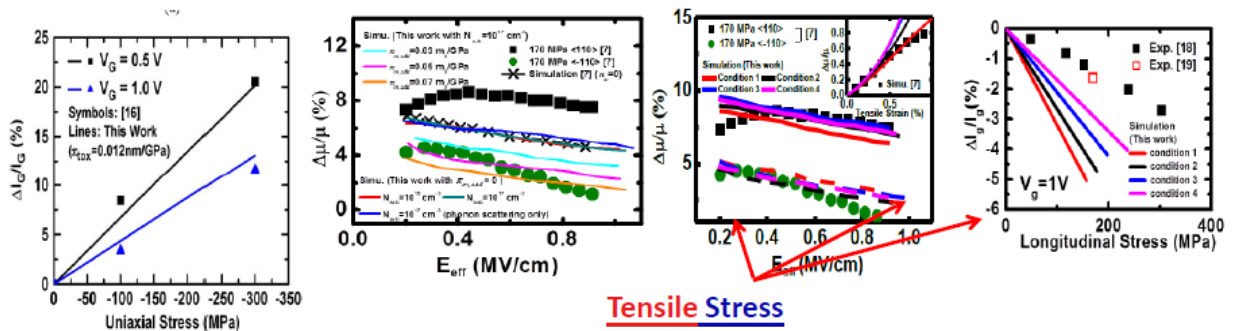
April 2011
TED

Hole Effective Masses as a Booster of Self-Consistent Six-Band $k \cdot p$ Simulation in Inversion Layers of pMOSFETs

Ming-Jer Chen, Senior Member, IEEE, Chien-Chih Lee, Student Member, IEEE, and Kuan-Hao Cheng

Published and Unpublished Results

● Electron Mobility Enhancement and Gate Tunneling



Tensile Stress

● We found that the widely-recognized band calculation methods might be invalid.

● Has just been accepted by EDL 2012

Jan. 2011 TED

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 58, NO. 1, JANUARY 2011

Gate Direct Tunneling Current in Uniaxially Compressive Strained nMOSFETs: A Sensitive Measure of Electron Piezo Effective Mass

Wei-Han Lee, Student Member, IEEE, and Ming-Jer Chen, Senior Member, IEEE

Evidence for the Fourfold-Valley Confinement Electron Piezo-Effective-Mass Coefficient in Inversion Layers of <110> Uniaxial Tensile Strained (001) nMOSFETs

Ming-Jer Chen, Senior Member, IEEE and Wei-Han Lee, Student Member, IEEE

Graduated Ph.D. and Master's (2011)

1. Dr. C. Y. Hsu 許智育
(TSMC 10-nm FinFETs RD)



2. Mr. K. H. Cheng 鄭寬豪
(TSMC 20-nm Integration RD)



3. Miss S. J. Kuang 光心君
(TSMC TCAD)



4. Mr. L. S. Pee 彭霖詳
(TSMC 20-nm Integration Platform RD)



Ph.D. and Master's to be Graduated (by end of 2012)

1. Dr. C. C. Lee 李建志 (Now in a German Top University,
on Graphene fabrication)
(TSMC 14-nm FinFETs RD)
2. Dr. W. H. Lee 李韋漢
(TSMC 10-nm FinFETs RD)
3. Mr. C. W. Lee 李致葳
(TSMC 20-nm RD Integration)
4. Mr. W. C. Chen 陳維志
(TSMC Production – Device Analysis)
5. Miss W. L. Chen, Miss T. H. Yeh, and Miss Y. H. Huang
(will join TSMC)

